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Item Type	Conference Paper
Authors	Alqahtani, Bashayr;Elatab, Nazek
Citation	Alqahtani, B., & El Atab, N. (2023). Optically Controlled Charge Trapping Memory Based on Spin Coated Hafnium Diselenide Flakes. 2023 IEEE 23rd International Conference on Nanotechnology (NANO). https://doi.org/10.1109/nano58406.2023.10231218
Eprint version	Post-print
DOI	10.1109/nano58406.2023.10231218
Publisher	IEEE
Rights	This is an accepted manuscript version of a paper before final publisher editing and formatting. Archived with thanks to IEEE.
Download date	2024-04-21 23:09:16
Link to Item	http://hdl.handle.net/10754/694015

Optically Controlled Charge Trapping Memory based on Spin Coated Hafnium Diselenide Flakes

Bashayr Alqahtani and Nazek Elatab

***Abstract*— This paper demonstrates the seamless fabrication of optoelectronic memory by integrating $HfSe_2$ as a charge-trapping layer in a MOS memory structure. Through a spin coating technique, solution-processable $HfSe_2$ flakes with average thicknesses of 2 nm were deposited between the tunneling and blocking oxide layers. The charge-trapping material distribution and thickness were explored by Atomic Force Microscopy and X-ray Diffraction Spectroscopy. The electrical characterization of MOS memory revealed a memory window of 5.5 Volts under ±16 Volts biasing. Furthermore, the memory endurance exceeds 10^4 electrical programming and erasing cycles. The retention test performed at room temperature showed that the memory device is expected to lose only 10% of the stored charges after 10 years. Under light stimuli (405nm wavelength and output power ~ 20 mW) with electrical readout voltage, the MOS memory showed an increase in the memory window from 5.5 Volts to 6.5 Volts.**

I. Introduction

Due to the limitation on further scaling down silicon-based non-volatile memories, the current interest is directed toward stacking multiple layers of memory cells vertically, integrating memories with other devices, and novel materials [1–3]. One form of downward scaling is the trend of "More than Moore" (MtM). It necessitates functional diversification in electronic devices where sensors can gather data, memories store it, and computing units process these information. The integration of optical sensing and data processing and storage in a device is greatly desired for efficient energy consumption and miniaturized electronic systems. Allowing light information to be stored with a low-voltage readout signal is advantageous for secure data storage and transformation. Meanwhile, combining light stimuli with electrical readout voltage contributes to improving memory capacity.

Emerging Two-dimensional (2D) materials for example, graphene, transition metal dichalcogenides (TMDCs), and black phosphorous, introduce a variety of physical and chemical properties that contribute to enhancing conventional memory devices. In addition, it inspires the next generation of affordable, flexible, and wearable flash memory. Due to the ultra-thin sheet thickness and low-temperature transfer technology of 2D materials, they can be heterogeneously combined with other systems of existing materials to produce remarkable light-matter interactions in optoelectronics. Embedding these nanosheets in memory devices presents fast switching speeds, multi-bit data storage, and high ON/OFF ratios, as well as broadband photoresponse and high photoresponsivity in optical sensors. The working mechanism of an optically controlled memory based on 2D materials is enabling charge-trapping sites for photo-generated charge carriers. In nonvolatile devices, the photo-generated electrons/holes are kept stored even after the removal of light stimuli. Many 2D materials have been studied in two/three terminals' memories but only a few of them were integrated with optical memories such as Molybdenum disulfide (MoS_2), black phosphorous (BP), Tungsten diselenide (WSe_2), and Boron nitride (BN) [4–7].

The layered hafnium diselenide ($HfSe_2$) is part of group IV (TMDCs) with a hexagonal lattice system as shown in figure 1(A) and maintains a moderate band gap in the 0.9- to 1.2-eV range down to monolayer thickness [8]. Although $HfSe_2$ has a band gap like silicon, it is compatible with desirable native high-k dielectric (HfO_2) which attracted many researchers' attention [8]. Furthermore, field effect transistors based on $HfSe_2$ are expected to have high carrier mobilities in the range of 3500 $cm^2V^{-1}s^{-1}$ owing to the weak electron-phonon interactions [9]. Lei et al. [10] fabricated ultrafast and ultrasensitive phototransistors, Au-contacted $HfSe_2$ phototransistors demonstrated high responsivity of up to 252 AW^{-1} with 7.8 ms response time. $HfSe_2$ is a potential material for device applications due to its aforementioned capabilities.

Recently, employing $HfSe_2$ in resistive-based memories has been investigated [11–13]. $HfSe_2$ based unipolar memristors showed steady resistive switching behavior during electrical characterization, a high switching ratio (>10^6), a relatively high temperature (106 °C), and long-term endurance (>10^4 s) [12]. Meanwhile, including $HfSe_2$ as a charge-trapping layer in flash memories and its performance under light illumination for programming and erasing cycles have not been studied yet. Here, we demonstrate the use of $HfSe_2$ flakes as a charge trapping layer (CTL) in a MOS memory structure by spine-coating the material solution to form the layer.

II. EXPERIMENTAL DETAILS

A. *MOS Memory Fabrication*

The memory devices are fabricated on a P+ Si substrate with resistivity in the range of 0.01-0.02 Ω-cm as the structure illustrated in figure 1(B). The samples were cleaned with an acetone/2-propanol (IPA) soak followed by BOE to etch the native oxide. Then, the tunneling oxide layer was deposited based on a (~7nm) thickness of Al_2O_3 using thermal Atomic Layer Deposition (ALD) at 250°C. After sonicating the $HfSe_2$ flakes in IPA solution for 3 minutes, the spin-coating technique is used to spread the

Research supported by King Abdullah University of Science and Technology.

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flakes uniformly. Therefore, the samples were heated at a temperature of 60°C on a hotplate to evaporate the IPA residuals. Blocking oxide layer (~21nm) thickness of Al_2O_3 was deposited afterward. Finally, the ITO layer (~150nm) thickness was deposited as top contact using a shadow mask with circular patterns with diameters ranging from 100µm to 400µm.

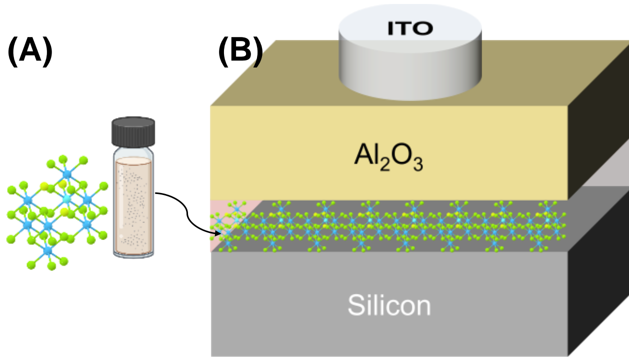

Figure 1: MOS Memory Device (A) 2D Material Lattice Formation, and (B) The Device Structure.

B. *Material and Device Characterization*

X-ray diffraction was performed at room temperature using a Bruker D8 Advance, aligned along the (400) plane of Si to confirm the material flakes. The electrical characterization was performed by B1500A Semiconductor Device Analyzer (SDA from Keysight, USA). The optical testing was done using a 405±0.5 nm blue laser in CW operation mode and output power ~ 20 mW from Shanghai Dream Lasers Technology.

III. Result and Discussion

Figure 2 shows the XRD pattern of the flakes deposited on the Si substrate, the peaks in the red color are related to material flakes which are in agreement with the previously reported in [14].

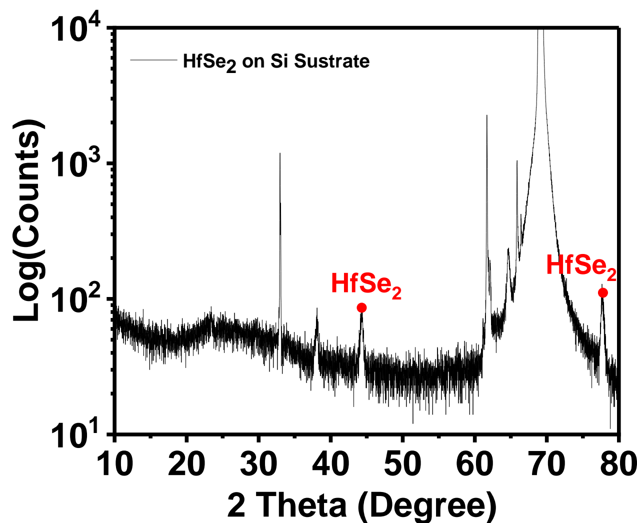

Figure 2: XRD pattern of HfSe2 on Si Substrate, highlighted points in red are regarding $HfSe_2$.

Regarding the electrical characterization, the Capacitance-Voltage (CV) curves were measured at a range of programming and erasing sweep voltages (P/E) from ±4 to ±22 Volts as presented in figure 3. To study the change of capacitance in different regions of the MOS memory, an AC signal of 50 mV amplitude and 80 kHz frequency was applied. The device is first programmed by sweeping the applied voltage from $-V_g$ to $+V_g$, then erased by sweeping the voltage back from $+V_g$ to $-V_g$. Furthermore, the increment in the memory window (V_t shift) is illustrated in figure 4. While increasing the P/E voltages, the increased electric field allows more charges to tunnel and be trapped in the CTL, and therefore a large memory window is obtained. At the electrical basing of ± 16 Volts, a memory window of 5.5 Volts was noticed which is acceptable considering the (~2nm) thicknesses of the flakes as CTL. It is slightly larger than employing RGO with similar thickness as CTL as reported in [15].

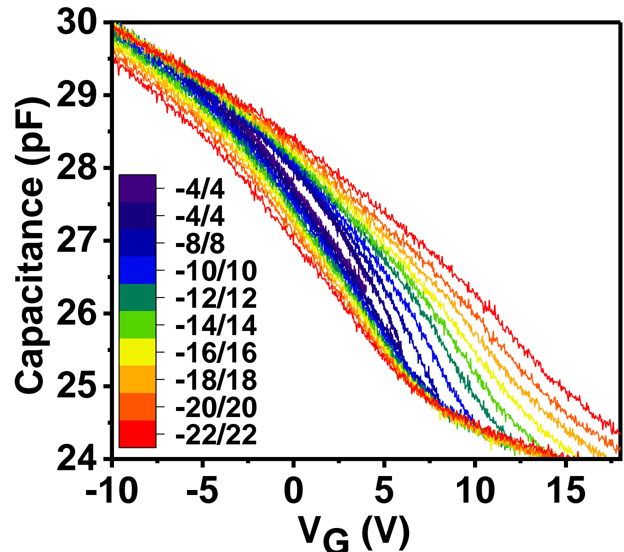

Figure 3: Capacitance-Voltage of MOS memory device at applying different voltage sweeps.

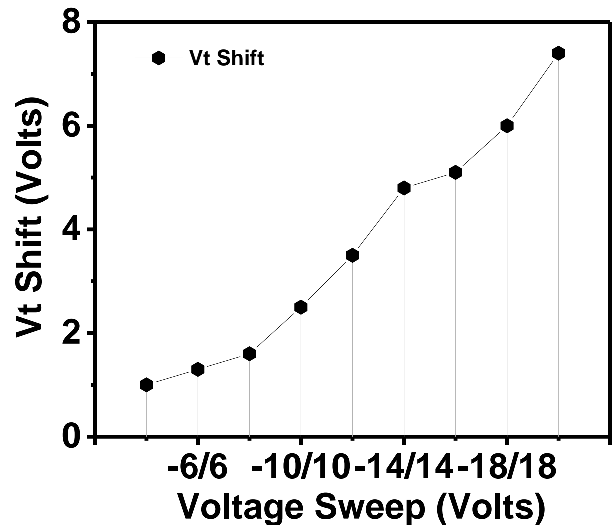

Figure 4: Vt Shift with increasing the sweeping voltages to ±20 Volts.

To further understand the charges trapping/de-trapping mechanism during P/E cycles, the energy band diagram in figure 5 of the memory shows $HfSe_2$ has an electron affinity of 4 eV [14]. The electron affinity of the ALD-grown aluminum oxide is 1.6 eV while the band gap is 6.5 eV [16], [17]. For silicon substrate, the electron affinity and the bandgap are 4.05 eV and 1.12 eV, respectively. The CTL has a bandgap and electron affinity similar to the Si, and the alumina oxide (tunneling layer) is contributing to barriers height for the electrons and the holes as 2.45eV and 2.93eV, respectively. Thus, electrons are preferable to tunnel through the oxide layer because of the shorter barrier height.

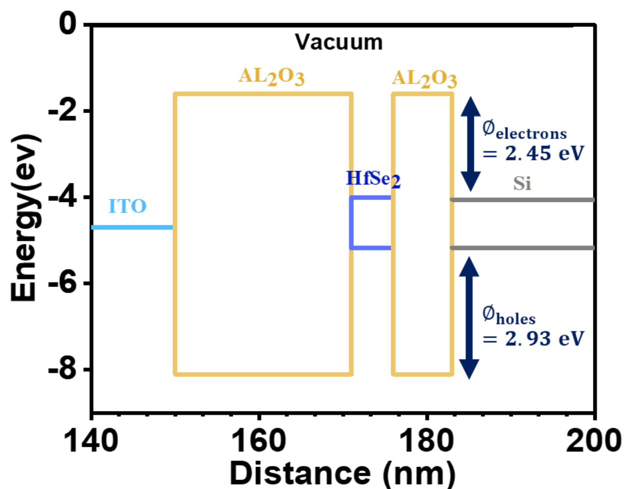

Figure 5: Bandgap diagram of the memory device showing the electrons and holes barrier height.

The device bandgap bending diagrams under applying positive and negative voltages are illustrated in figure 6 (A and B). During a positive biasing, the barrier for the minority carriers of the substrate (electrons) becomes thinner and consequently leading the electrons to tunnel through the oxide and get stored in the CTL. In contrast, the holes are anticipated to tunnel through the barrier at a negative gate biasing for the same reason.

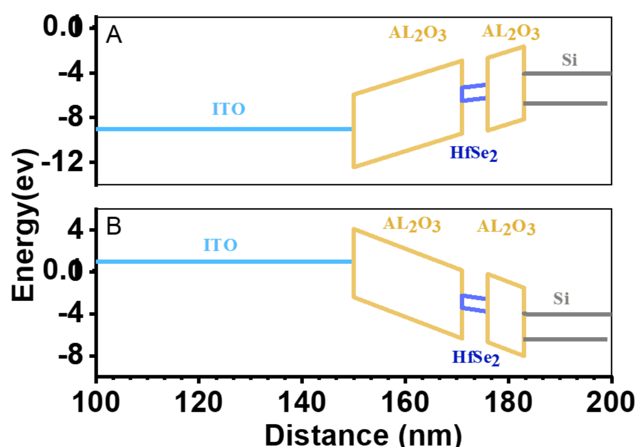

Figure 6: Band diagram under (A) positive voltage and (B) negative voltage applied.

Figure 7 depicts the measurement of a fresh memory cell's P/E signals at room temperature, the device showed good reliability and endurance under 10^4 cycles. Moreover, the slight decrease in Vt shift of around 8% demonstrates the memory's great endurance.

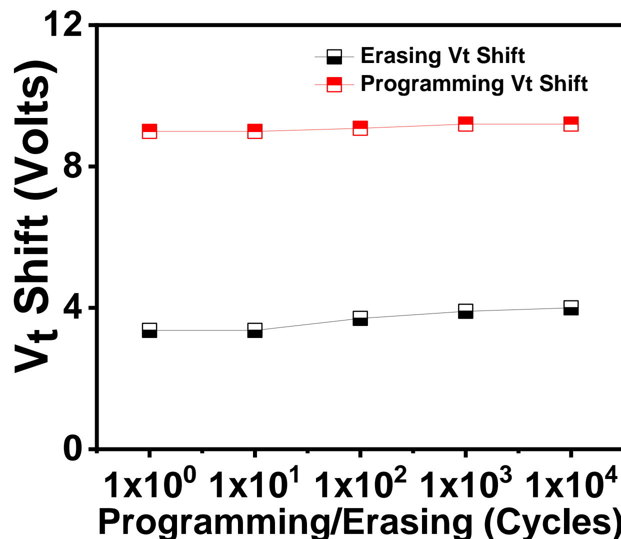

Figure 7: The MOS memory endurance at room temperature.

The effective lifetime of nonvolatile storage is the device retention time. The memory retention test was conducted at room temperature. According to measurements, a device would experience a charge loss of 10% after 10 years as plotted in figure 8.

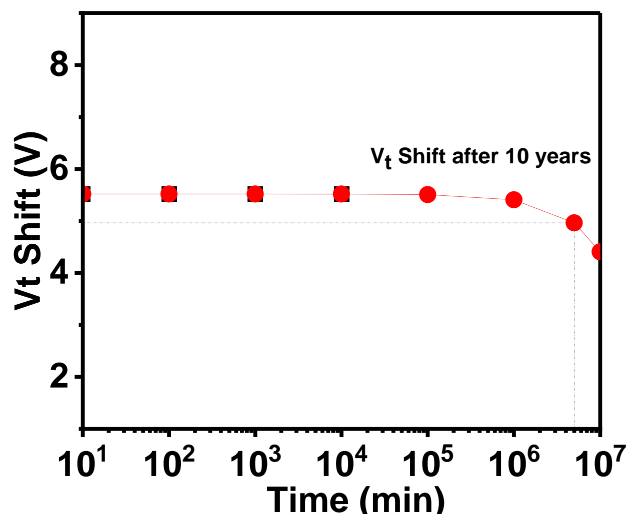

Figure 8: The device retention after 10 years with a memory window larger than 4 Volts.

Regarding the device's optical measurement, shining a laser light of 405nm wavelength and ~ 20 mW output power while biasing the device to record the change, an increase in the memory window was observed which is due to the shift of the programming signal towards the right side. Figure 9 illustrated the CV curve of P/E cycles under dark conditions and the corresponding optical programming curve.

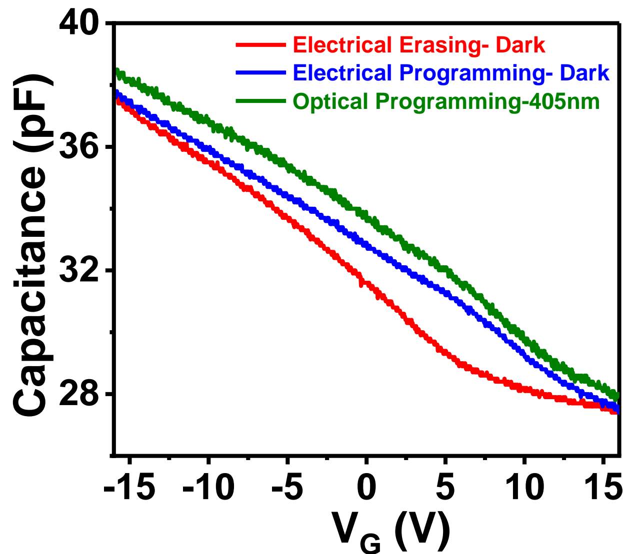

Figure 9: Behavior of the memory device under dark conditions biasing and light illumination.

IV. Conclusion

In conclusion, this work demonstrated embedding 2D material flakes in memory devices and their light interaction as a charge-trapping layer. The fabrication process used a MOS memory structure and solution-processable 2D material flakes, allowing for performing the study in straight forward approach. In dark conditions, the $HfSe_2$ flakes-based MOS memory exhibited a large memory window of 5.5 Volts at ±16 Volts basing which was enhanced further when including an optical programming signal to control the device. besides that, the endurance (>10^4cycles) and retention time (10% charge loss at room temperature after 10 years) measurements of the fabricated devices presented reliable and stable results.

Acknowledgment

This work was supported by the King Abdullah University of Science and Technology baseline fund.

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