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In-Solution Germanium Selenide Nanosheets as Charge Trapping Layer in Flash Memories

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Abstract — **Germanium selenide (GeSe) is a highly promising material with several attractive characteristics, particularly in the field of ferroelectric and phase-change memories due to its outstanding electronic behavior. However, the potential of GeSe as a charge-trapping layer in flash memory has received less attention. Herein, the fabrication of a nonvolatile MOS memory device using GeSe nanosheets as a charge-trapping layer was demonstrated and the materials flakes were examined extensively. The electrical performance of the memory device was investigated. Intriguingly, it exhibited an extraordinarily wide memory window of 9 V under ±10 V electrical biasing. Additionally, the devices presented high endurance of 10^4 programming and erasing cycles, and reliable charge storage of only 56% loss after 10 years.**

I. Introduction

Layered semiconductors, such as group-IV chalcogenides, that is, MX (M = Ge, Sn; X = S, Se), appear to attract less attention in the context of the tremendous interest in two-dimensional (2D) materials. Meanwhile, these chalcogenides have promising applications in electronic devices due to their fascinating properties of high carrier mobility and air stability. Monolayer GeSe is the only semiconductor among the four alternatives with a direct and small band gap of 1.1 eV[1]. Furthermore, the estimated carrier mobility of monolayer GeSe approaches 10^3 $cm^2V^{-1}s^{-1}$ [2]. Theoretically, GeSe has greater environmental stability than other 2D materials due to its surface's limited amount of dangling bonds.

The combination of ferroelectric and the ability to switch between amorphous and crystalline phases makes GeSe a genuinely unique and promising candidate for ferroelectric and phase-change memory technologies[3]. This study investigates embedding the in-solution GeSe flakes as a charge-trapping layer (CTL) in the MOS memory structure.

The device fabrication process is illustrated in Fig.1 in steps sequenced from 1 to 6. P+ Si wafer used as substrate and bottom contact. After soaking the samples in acetone and isopropanol (IPA) to clean them, the native oxide was etched using BOE. The thermal atomic layer deposition (ALD) was used to deposit the alumina oxide layers with thicknesses of 7 nm tunnelling and 21 nm blocking at 250°C. The GeSe nanosheets were deposited by a spin coating process on the top of the tunnelling oxide layer. Lastly, ITO sputtered as top contact by a shadow mask.

II. Result and discussion

The flakes distribution was investigated using Atomic Force Microscopy presented in Fig.2. Also, X-ray diffraction was performed at room temperature and the appeared peaks in Fig.3 aligned well with the previously reported[4]. Furthermore, GeSe nanosheets exhibit distinctive two peaks at B_{3g}^1 and A_g^1 and their Raman frequency shifts correspond to 149.8 cm^{-1} and 188 cm^{-1} as seen in Fig.4 and agrees with [5].

Capacitance–Voltage (CV) measurements were performed by B1500A Semiconductor Device Analyzer at different biasing voltages. The hysteresis curve revealed a remarkably large memory window of 9 V represented by the shift in threshold voltage of the two sweeps depicted in Fig.5 at ±10 V biasing voltage. Fig.6 displayed the memory window at different biasing which indicated the huge charge trapping in the GeSe flakes compared to the negligible memory window of the control devices (only 28 nm thickness of alumina oxide without CTL). The device expressed good endurance to 10^4 cycles and a long retention time with only 56% charge loss after 10 years.

In conclusion, this study highlights the potential of GeSe in the field of nonvolatile memory devices.

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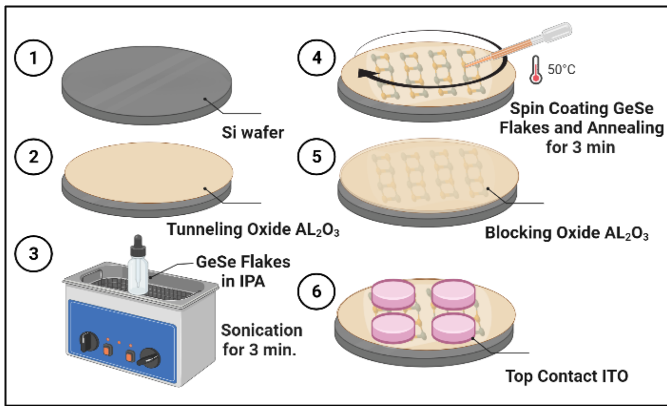

Figure 1: The MOS memory device fabrication process includes the spin coating technique of GeSe flakes in IPA to form a charge-trapping layer.

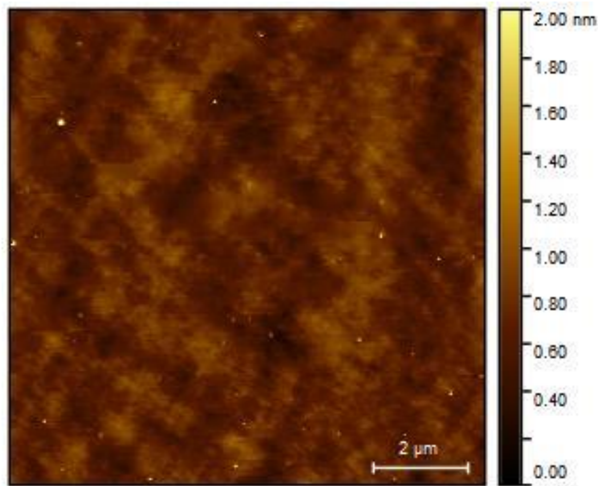

Figure 2: AFM scanning of the GeSe flakes spread on Si wafer.

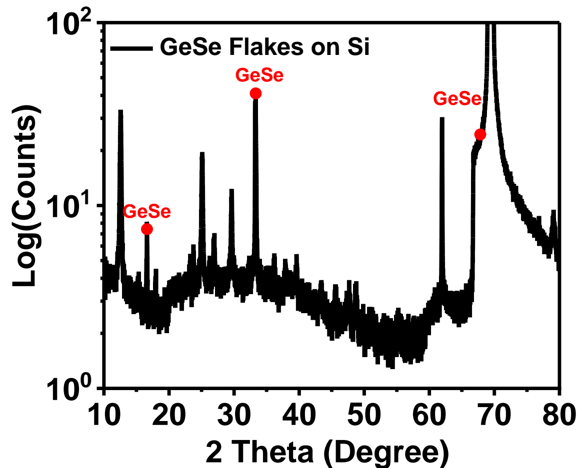

Figure 3: XRD pattern of GeSe flakes on Si wafer. The peaks highlighted in red correspond to the 2D material flakes.

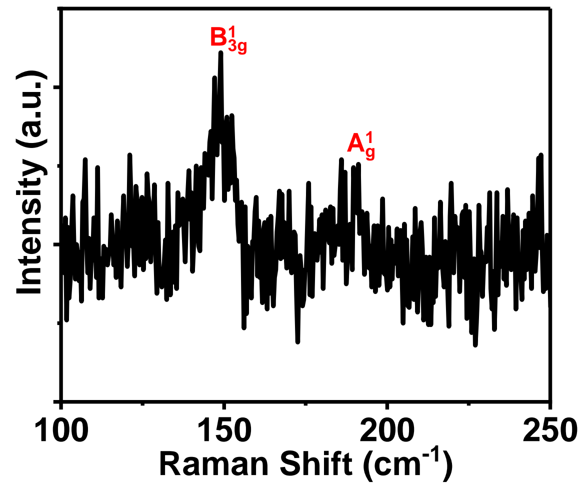

Figure 4: Raman peaks of GeSe nanosheet at 149.8 cm^{-1} and 188 cm^{-1}.

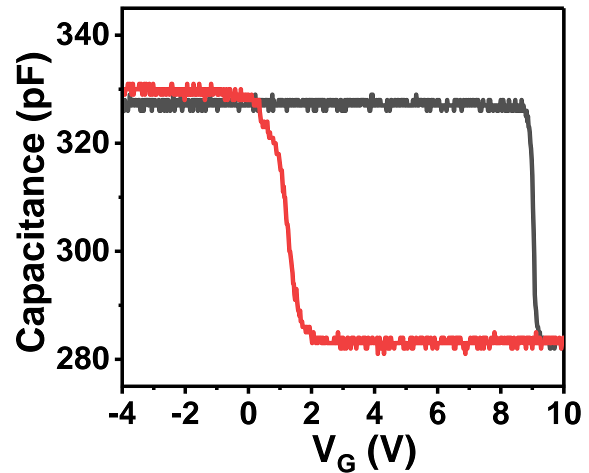

Figure 5: Capacitance-Voltage measurement of MOS memory device at biasing of ±10 V. The wide shift in threshold voltage indicates the 9V memory window.

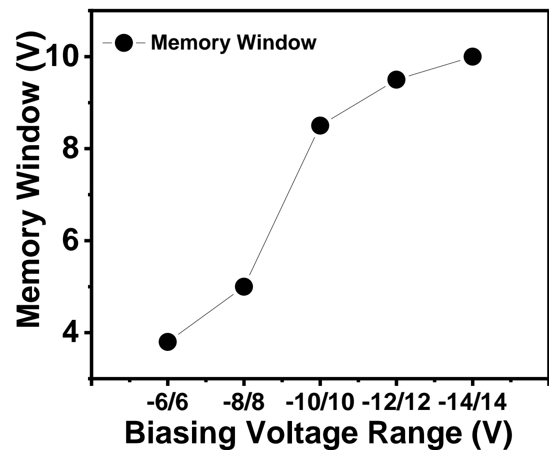

Figure 6: The increment of memory window capacity at different basing voltage.