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RF Performance Assessment of Sub-8nm GaN-SOI-FinFET Using Power Gain Parameters*

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***Abstract* – This work presents, a radio frequency (RF) performance evaluation of nanoscale gallium nitride-silicon-on-insulator fin field-effect transistor (GaN-SOI-FinFET). All the results have simultaneously been compared with conventional FinFET (Conv. FinFET). All the results show that the power gains have significantly improved in terms of Gma (maximum available power gain), Gms (maximum stable power gain), stern stability factor, G_{MT} (maximum transducer power gain), and an appreciable reduction in intrinsic delay as compared to conventional FinFET. Current gain unilateral power gain and have also been evaluated for the extraction of f_T (cut-off frequency) and f_{MAX} (maximum oscillator frequency) respectively. f_T and f_{MAX} enhance by 88.8% and 94.6% respectively. This analysis has been done at several THz frequencies. The implementation of GaN in the channel reduces the parasitic capacitance and paves the way for high-performance RF applications.**

Index Terms- Cut-off frequency, GaN-SOI-FinFET, Maximum oscillator frequency, Power Gains, RF.

I. Introduction

Continuous scaling of metal oxide semiconductor (MOS) devices is required for high speed, better performance, and higher power efficiency. Scaling leads to undesirable short channel effects (SCEs) and parasitic capacitances in a MOS device which make it unsuitable for RF application. To overcome these effects, 3D structures based on silicon such as FinFETs [1-3], gate-all-around FinFET and FETs [4-6], and other multi-gate FETs have been developed [7, 8]. In recent years different materials have been introduced in nanochannel transistors, which exhibit better performance. Such devices present near ideal subthreshold slope (SS) and lower leakage currents [9].

Among all the materials, Gallium Nitride (GaN) is the most promising material for high voltage and frequency operation owing to its larger bandgap, higher electron mobility, and ability to operate at very high temperatures without degrading its characteristics [10, 11]. The FinFETs based on GaN has better gate controllability due to the nonplanar 3D structure [12]. Very low thermal resistance has been observed in GaN material which makes it suitable for power transistors. Therefore, the self-heating effect has not been considered in this analysis. Many other properties make it a more desirable semiconductor for high frequency (THz) applications.

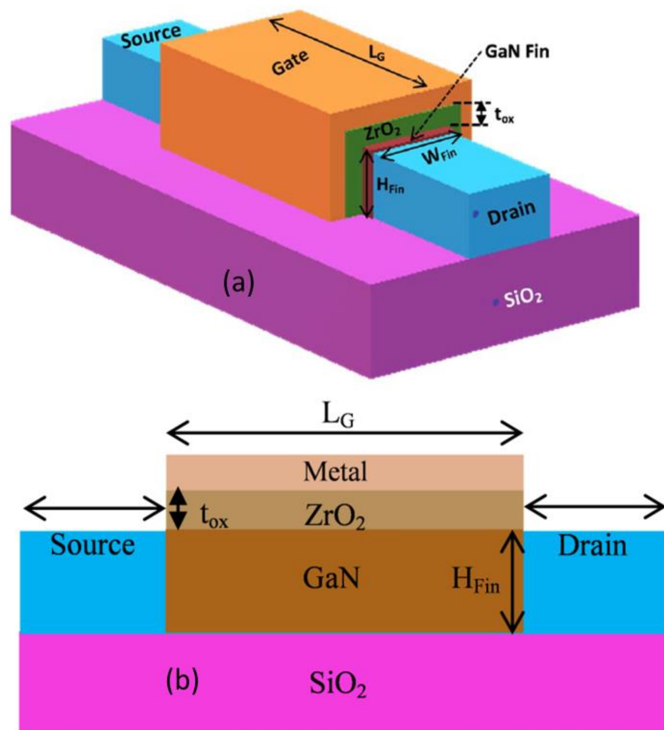

Fig. 1: (a) Three-dimensional and (b) Two-dimensional view of GaN-SOI-FinFET

II. Device Structure and Simulation Methodology

TABLE I: Device Parameters

Parameters	Dimensions
L_G	8 nm
L_S/L_D	10 nm
H_{Fin} (Fin Height)	8 nm
W_{Fin} (Fin Width)	4 nm
t_{OX} (Oxide Thickness)	1 nm
N_{Ch}	1.0 x 10^{16} cm^{-3}
$N_{S,D}$	1.0 x 10^{21} cm^{-3}

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Fig. 1 shows the three-dimensional and tow dimensional device design of the GaN-SOI- FinFET. For this work, 8 nm gate length (L_G) has considered along with the oxide thickness (t_{ox}) of 1 nm for on all three fin's sides. Width (W_{Fin}) and height (H_{Fin}) of the fin are 4 nm and 8 nm respectively. Low doping concentration (10^{16} cm^{-3}) has been considered in the channel region (N_{Ch}) uniformly however, very high (10^{21} cm^{-3}) uniform doping concentration has considered in the source/drain ($N_{S,D}$) regions. The gate electrode work function is 5.0 eV. We have used a TCAD device simulator for the performing the entire simulation [13]. We have performed the numerical simulation followed by device design in this work. Constant Voltage and Temperature (CVT) model has been considered for the numerical simulation of the device and this model is used to account for the mobility degradation and the ionized impurity scattering, caused due to surface roughness scattering, photon scattering, and field dependent mobility. Next, we have considered Shockley Read Hall model for recombination effects which useful for the leakage current simulation.

III. Result and Discussion

For the improve RF performance of the proposed device, various gain parameters have been evaluated. In order to evaluate power gains, first Gma and Gms have been evaluated for conventional FinFET and GaN-SOI-FinFET using Eq. (1) [14]. All the data for Gma and Gms have been plotted against frequency (in THz range) as reflected in Fig. 2. Fig. 2 reflects the improved performance of GaN-SOI-FinFET in comparison to conventional FinFET. Gma and Gms reflects the desirable maximum theoretical power gain of the device. For the defining the Gma a two-port network has been considered and defined as the retio of power available (maximum) at load to the power available (maximum) at the source. GaN-SOI-FinFET depicts substantial improvement in Gma and Gms due to the electrical properties of GaN as the larger value of Gma and Gms is desirable for high frequency applications.

$$G_{ma} = \frac{P_{load,\max}}{P_{source,\max}} \quad (1)$$

Low-noise amplifiers (LNA) designing is as important as power gains for RF amplifiers and in this way, stability is the key parameter. Amplifier's stability is also known as Stern stability factor (K), which has a value of K usually < 1 at low frequency and > 1 at high frequency [15, 16]. K can be defined by Eq. (2) [14, 17], as-

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2.|S_{12.} \cdot S_{21}|} \quad (2)$$

Here, reflection coefficients are denoted by S_{11} and S_{22} while transmission coefficients are denoted by S_{12} and $S_{21,}$ and Δ is defined as-

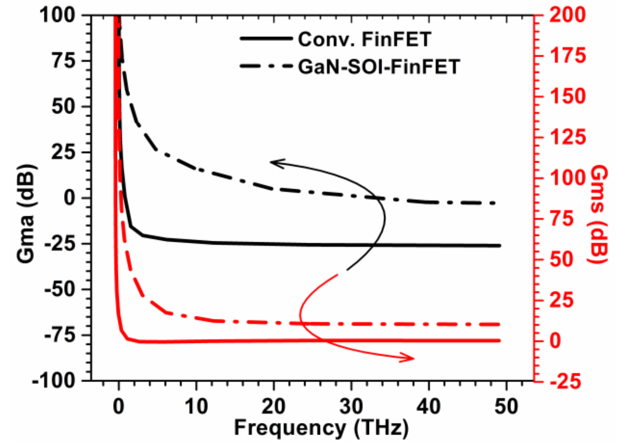

Fig. 2: Gma and Gms for Conv. FinFET and GaN-SOI-FinFET.

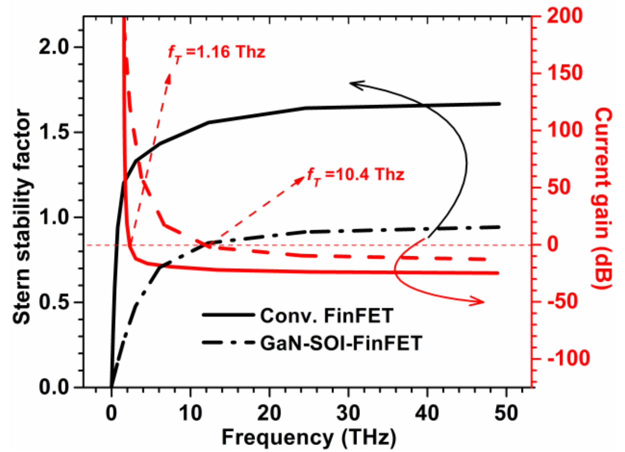

Fig. 3: Stern Stability Factor and Current Gain for Conv. FinFET and GaN-SOI-FinFET.

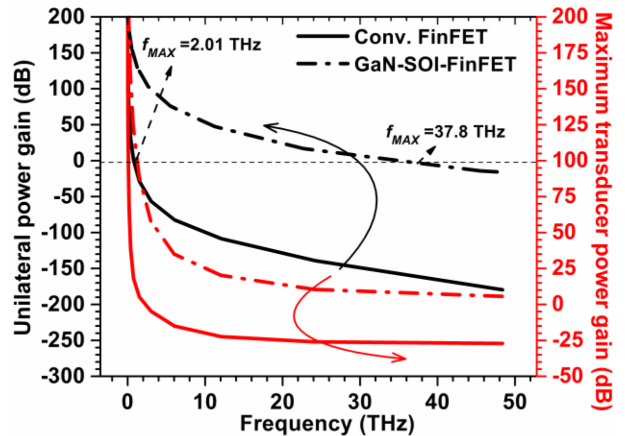

Fig. 4: Unilateral Power Gain and Maximum Transducer Power Gain for Conv. FinFET and GaN-SOI-FinFET..

$$\Delta = S_{11} \times S_{22} - S_{12} \times S_{21} \quad (3)$$

Stern stability factor for both the devices is shown in Fig. 3. From Fig. 3 it has been observed that K is greater than one at-

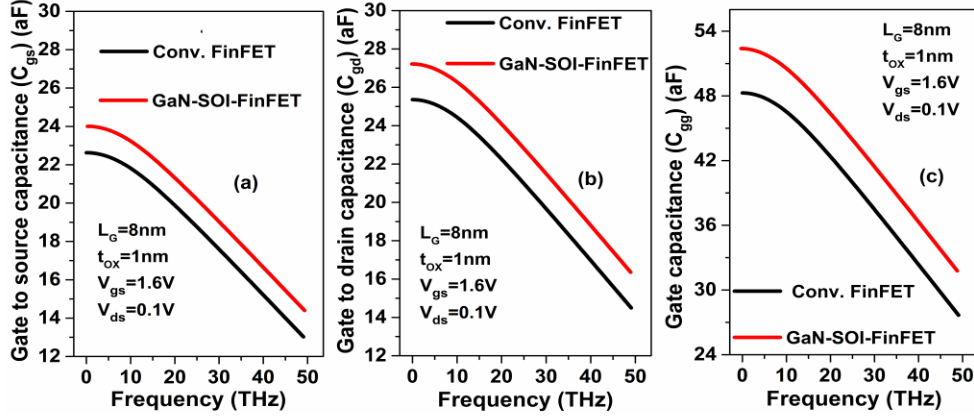

Fig. 5: Parasitic capacitances (a) C_{gs} (b) C_{gd} and (c) C_{gg}; as a function frequency for Conv. FinFET and GaN-SOI-FinFET

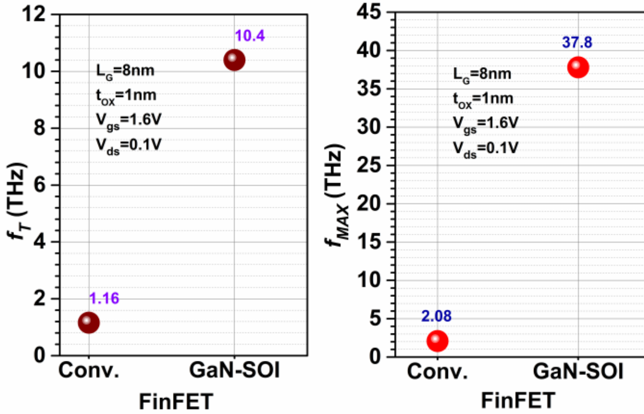

Fig. 6: (a) Cut-off frequency (f_T) and Maximum Oscillator Frequency and (b) (f_{MAX}) for for Conv. FinFET and GaN-SOI-FinFET

-high frequency for the conventional FinFET, and ~1 (slightly > 1 for the proposed device at a higher frequency and it is desirable for the designing of RF amplifiers.

Further, cut-off frequency (f_T) has been extracted from current gain plot at unity current gain [18] (shown in Fig. 3). f_T can be defined by Eq. (4) and it measures the swing and speed for high-speed digital applications [19-21]:

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{4}$$

where g_m is the transconductance and parasitic capacitances are denoted by gate to drain capacitance (C_{gd}) and gate to source capacitance (C_{gs}). These parasitic capacitances have also been evaluated and plotted aginst frequency as shown in Fig. 5. Result shows that f_T increases by 88.8% in GaN-SOI-FinFET as compared to conventional FinFET as shown in Fig. 6(a) due to reduced values of capacitances (shown in Fig. 6). Maximum oscillator frequency (f_{MAX}) has also been evaluated at the unity unilateral power gain [22] (shown in Fig. 4). f_{MAX} should be as high as possible for RF applications and can be calculated by Eq. (5) [18, 23]:

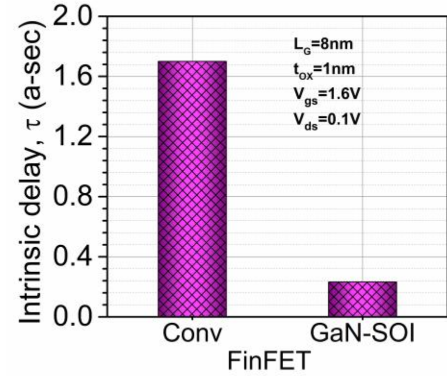

Fig. 7: Intrinsic delay for Conv. FinFET and GaN-SOI-FinFET.

$$f_{MAX} = \frac{f_T}{\sqrt{4R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)}} \tag{5}$$

Where g_{ds} is drain conductance, and R_g is gate resistance. Fig. 4 shows that f_{MAX} enhances by 94.6% in the proposed device as compared to conventional one and clearly reflected in Fig. 6(b). Fig. 4 also shows the RF performance of the device, and the efficacy of the two ports in terms of G_{MT} which is evaluation of the effectiveness of the two ports. G_{MT} is improved in the proposed device design as compared to conventional one as shown in Fig. 4 owing to GaN material in the channel region which made the device more suitable for RF applications. Thereafter, intrinsic delay (as shown in Fig. 7) has been calculated and plotted for both conventional FinFET and GaN-SOI-FinFET.

$$\tau = \frac{C_{gg}.V_d}{I_{ON}} \tag{6}$$

where applied drain bias voltage is denoted by V_d, C_{gg} is the gate capacitance evaluated and plotted in Fig. 5, and I_{ON} is the on-current of the device. Fig. 5 reflects very high reduction (85.29%) in intrinsic delay in the GaN-SOI device as

compared to conventional FinFET device due to the reduction of gate capacitances and higher current driving capability. Thus, GaN-SOI-FinFET proves to be a most promising candidate for RF applications.

IV. Conclusion

This work investigated the efficacy of GaN based SOI-FinFET device for improved RF performance. From the results it has been observed that GaN-SOI-FinFET enhanced gain metrices significantly in terms of Gma, Gms and G_{MT}. The parasitic capacitances have also been measured in terms of C_{gs}, C_{gd} and C_{gg} and it is observed that these capacitances are reduced significantly which enhances the cut-off frequency by ~9 times and f_{MAX} by ~18 times in the GaN based FinFET as compared to conv. FinFET. Intrinsic delay has also reduced by 6.8 times in GaN-SOI-FinFET as compared to conventional FinFET. Thus, all the results show that GaN based FinFET is a better solution for high-performance RF applications in sub 10nm regime.

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