Improved High Step-Up Cockcroft-Walton Magnetic Coupling Inverter

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Abstract—An improved dual winding magnetically coupled-inductors inverter based on a Cockcroft-Walton multiplier voltage cell is proposed in this paper. Compared with the conventional generalized Cockcroft-Walton multiplier voltage Z-source inverters, the proposed inverter attains higher voltage gain by decreasing the transformer’s turns number. As a result, lower cost, higher efficiency, higher voltage boost factor, and higher density can be realized in the proposed inverter. Furthermore, unlike conventional magnetically coupled impedance source inverters, the proposed topology offers a larger voltage boost factor for small shoot-through duty ratios with a smoother slope, which enhances the practical controllability of the inverter. Hence, a higher modulation ratio can be applied, which results in a better quality of the inverter’s waveforms. A clamping circuit is used to reduce the leakage inductance effects of the coupled inductors. As a result, the huge voltage spikes across the inverter bridge are eliminated. In addition, the proposed inverter draws a smooth and continuous input current from the input dc source, which is suitable for renewable energy sources. Detailed, theoretical analysis, simulation and experimental results are provided.

Index Terms—Clamping circuit, Cockcroft-Walton circuit, voltage multiplier, voltage overshoot.

I. INTRODUCTION

Recent advances in microgrids have created an expansion in the utilization of renewable energy sources (RES) and energy storage systems (ESS). Over the recent years, reliable and efficient high voltage gain power electronics converters have been instrumental in RES and ESS applications [1]. Magnetically coupled impedance source inverters have become noteworthy among researchers due to their distinguished features such as high voltage boost ability, high efficiency, low stress across the semiconductor switches, high controllability, high density, fewer number components, and high reliability, etc. [2]. In DC-AC conversion, magnetically coupled inductors can be utilized in the impedance networks to provide higher voltage step-up ability with a small shoot-through (ST) duty cycle and a high modulation ratio that causes low voltage stress on the inverter’s power switches and improvement in the output AC voltage quality [3].

The most popular magnetically coupled structures can be named Trans Z-source [4-6], A-source [7-8], Γ-source [9-10], and Y-source [11-12] networks. Despite all privileges of these topologies, they suffer from a major drawback; that is huge voltage spikes appear across the power switches because of the coupled inductors’ leakage inductances. As a result, the voltage rating of devices increases. In addition, efficiency and voltage gain decrease. Recently, several clamping circuits have been designed to remove DC-link voltage overshoots across the inverter bridge. An extra diode has been exploited in the modified Γ-source inverter, improved Σ-source inverter, and enhanced trans Z-source inverter to suppress voltage spikes on the power switches [13-15]. However, these inverters cannot offer higher voltage boost ability than their counterpart original topologies. In [16-18], passive components along with the diodes have been applied to the original topologies to provide high DC-link voltage with less switching voltage overshoots. However, similar to the existing magnetically coupled Z-source topologies, these inverters have a weak voltage boost ability at the low ST duty ratio ranges, which leads to impediments in the control of the converters. To overcome this drawback, switched coupled inductor impedance source converters have been presented in [19-25]. In addition, generalized Z-source and quasi-Z-source inverters based on Cockcroft-Walton multiplier voltage cells are proposed in [24].

In this paper, an improved magnetic coupling inverter based on the Cockcroft-Walton voltage multiplier cell is presented. Compared with the existing topologies proposed in [24], the proposed improved topology offers a higher voltage gain with the same parameters and the number of components. In addition, the proposed inverter has no voltage spikes problem. In section II, the operation principle and theoretical analysis of the proposed inverter are presented. In section III, detailed comparison is provided. In section IV, design of parameters is shown. Finally, in section V, detailed simulation and experimental results are reported.

II. Proposed Magnetic Coupling Inverter

The proposed magnetic coupling inverter is shown in Fig.1. It has one diode (D1), two capacitors (C1 and C3), an input inductor (L1) in series with the input source, a coupled-transformer with the turns ratio of N=N1/N2, a Cockcroft-Walton voltage multiplier cell which consists of two capacitors (C2 and C4) and two diodes (D2 and D3), and a three-phase inverter bridge. It can be seen that the proposed inverter has the same components as the generalized quasi-Z-source Cockcroft-Walton inverter. However, the different shape of the coupled inductor and improved structure of the component’s arrangement brings many advantages to the proposed inverter.
A. Operation principle

The proposed topology has two shoot-through (ST) and non-shoot-through (NST) modes similar to the existing impedance-source inverters. Fig. 2 (a) illustrates the equivalent circuit of the proposed inverter in the ST state. In this mode, the inverter bridge is equivalent to a short circuit, D2 in the Cockcroft-Walton cell is conducting, while D1 and D3 are reverse biased. In this state, the input inductor is charged by the input DC source, and coupled inductors are energized by capacitors C2, C3, and C4. In the NST state, the inverter bridge is equivalent to a current source, diodes D1 and D3 are turned ON, while diode D2 is blocking. In this mode, the saved energy in coupled inductors is released to the loads, and capacitors. Furthermore, the stored energy in the leakage inductance of winding N1 is absorbed by capacitors C1 and C3, and capacitors C2 and C4 absorb the saved energy in the leakage inductance of winding N2. Fig. 1 shows the high-frequency loop path of the proposed inverter. The loop includes bridge-D2-C2-C1-D1-C3-bridge. As a result, the DC-link voltage is clamped to V_{C2}+V_{C1}+V_{C3}, which results in voltage spikes elimination across the inverter bridge.

B. Voltage analysis

To simplify steady state analysis, the capacitors' equivalent series resistance (ESR) and the parasitic resistance of the inductors and coupled inductors are assumed insignificant. All switches are assumed ideal and the parasitic capacitance and ON resistance are not considered. Additionally, the coupling coefficient is defined as \eta = \frac{k}{\sqrt{L_m L_k}}, where L and Lm are the leakage and magnetizing inductances of the coupled transformer, respectively. Hence, the relation between the coupling coefficient and leakage inductance ratio is \eta = \frac{1-k}{k}.

In ST mode, by applying KVL to Fig. 2 (a), the following equations can be derived:

\[
\begin{align*}
V_{N1} &= V_{Lm} = NV_{N2} \\
V_{L1} &= V_{dc} + V_{C1} + V_{C2} + V_{C4} \\
V_{N2} &= \frac{N}{N+1} (1+\eta) \\
V_{N2} &= \frac{V_{C2} + V_{C4} + V_{C3}}{V_{N2}}
\end{align*}
\]

In NST state, by applying KVL to Fig. 2 (b), we can obtain:

\[
\begin{align*}
V_{L1} &= V_{dc} - V_{C3} \\
V_{N2} &= \frac{-V_{C1}}{N(1+\eta)} \\
V_{N2} &= \frac{V_{C2} - V_{C4} + V_{C3}}{V_{N2}}
\end{align*}
\]

By utilizing the volt-second balance principle to coupled and input inductors, we have:

\[
\begin{align*}
\int_{0}^{T_s} V_{L1} dt + \int_{0}^{T_s} V_{L1} dt = 0 \\
\int_{0}^{T_s} V_{N2} dt + \int_{0}^{T_s} V_{N2} dt = 0
\end{align*}
\]

(3)

In (3), D and T_s represent the ST duty ratio and switching period, respectively. By putting (1) and (2) in (3), the voltage stress across the capacitors can be derived as follows:

\[
\begin{align*}
V_{C1} &= \frac{ND(1+\eta)}{N(1+\eta) + D - 2ND(1+\eta) - 2} V_{dc} \\
V_{C2} &= \frac{N(1+\eta) + D - 2ND(1+\eta) - 2} {N(1+\eta) + D - 2ND(1+\eta) - 2} V_{dc} \\
V_{C3} &= \frac{N(1+\eta) + D - 2ND(1+\eta) - 2} {N(1+\eta) + D - 2ND(1+\eta) - 2} V_{dc} \\
V_{C4} &= \frac{N(1+\eta) + D - 2ND(1+\eta) - 2} {N(1+\eta) + D - 2ND(1+\eta) - 2} V_{dc}
\end{align*}
\]

Also, the peak dc-link voltage across the inverter bridge can be obtained as:

\[
V_i = \frac{N(1+\eta) - 1}{N(1+\eta) + D - 2ND(1+\eta) - 2} V_{dc}
\]

(5)

Since the value of the leakage inductance compared with the magnetizing inductance is very small, we can consider \eta = 0 or k=1. Thus we can rewrite the (5) as:

\[
V_i = \frac{N - 1}{N + D - 2ND - 2} V_{dc}
\]

(6)

Then, the voltage boost factor can be written as:

\[
B = \frac{N - 1}{N + D - 2ND - 2}
\]

(7)

From (7), B against D is plotted in Fig. 3. As shown in Fig. 3 (a) that the voltage boost factor of the proposed inverter increases by reducing the transformer turns numbers which can increase efficiency and reduce size.
In addition, from Fig. 3 (b), it can be clearly seen that the effect of the leakage inductance on the voltage gain of the proposed inverter is negligible. The peak ac phase voltage is given by (8), where $M$ presents the modulation index:

$$V_{ph} = \frac{M(N-1)}{2(N + D - 2ND - 2)} V_{dc}$$

It must be noted that the modulation index is the ratio of the peak value of the sine control waves to that of the peak value of the triangular carrier signal in the utilized simple boost control. According to the simple boost control, the relation between ST duty ratio and modulation index is given as $D=1-M$. Then, from (8), the voltage gain is calculated as in (9).

$$G = \frac{M(N-1)}{(-N - M + 2NM - 1)}$$  

### C. Current analysis

By applying KCL in ST state shown in Fig. 2(a) we have:

$$\begin{align*}
    i_{C1} &= -i_{dc} \\
    i_{C2} &= i_{Lm} - i_{N1} - i_{dc} + Ni_{N1} \\
    i_{C3} &= i_{Lm} - i_{N1} \\
    i_{C4} &= i_{Lm} - i_{N1} - i_{dc} \\
\end{align*}$$

Furthermore, in NST state we can get from Fig. 2 (b):

$$\begin{align*}
    i_{C1} &= i_{N1} - i_{Lm} - i_{l} \\
    i_{C2} &= Ni_{N1} - i_{l} \\
    i_{C3} &= i_{dc} - i_{l} \\
    i_{C4} &= -Ni_{N1} \\
\end{align*}$$

By applying current-ampere balance principle to capacitors, we have:

$$\int_0^T i_{cl} \, dt + \int_0^T i_{cl} \, dt = 0$$

Where $i=1,2,3,4$, represents the capacitors' indexes. By putting (10) and (11) in (12), we obtained:

$$\begin{align*}
    i_{N1} &= \frac{1 + 2D}{ND} i_{dc} \\
    i_{Lm} &= \frac{1 + 2D - ND}{ND} i_{dc} \\
\end{align*}$$

### D. Voltage stress across the semiconductors

From Fig.2 (a), the voltage stress across the diodes $D_1$ and $D_3$ can be obtained, and from Fig.2 (b), the voltage stress across $D_2$ can be attained:

$$\begin{align*}
    V_{D1} &= V_{N1} + V_{C1} = \frac{N}{N + D - 2ND - 2} V_{dc} \\
    V_{D2} &= V_{D3} = V_{C4} = \frac{1}{N + D - 2ND - 2} V_{dc} \\
\end{align*}$$

III. COMPARATIVE ANALYSIS

The proposed inverter features dc-link voltage clamping to reduce the effects of the coupled transformer’s leakage inductance. While in many of the original magnetically coupled impedance source inverters, voltage gain and efficiency are affected by the huge voltage spikes. Additionally, unlike topologies in [7], the proposed inverter provides a smooth continuous input current which is recommended for PV, fuel cell, and battery applications. Voltage boost ability, the voltage stress on switches, and input inductor current ripple are evaluated in the following sub-sections. For a fair comparison of the voltage boost ability, voltage gain, voltage stress across the power switches, and input current ripple, the transformer's turns ratio is assumed $N=N1/N2=100/35=2.85$ in the proposed inverter and the selected topologies, or 0.35 in [19] and [24].

### A. Voltage boost ability

Fig. 4(a) depicts the ST duty cycle versus voltage boost factor of the proposed and conventional coupled inductors impedance source converters for the same transformer's turns ratio. As shown, the proposed inverter offers higher voltage gain, especially at the low ST duty cycles, which is impossible in conventional impedance source converters. Furthermore, it is found that compared with the quasi Z-source Cockcroft-Walton topology, the proposed inverter offers a higher voltage boost ability with the same number of components. In addition, Fig. 4(b) shows that the proposed inverter provides a higher voltage gain for the same voltage modulation ratio when compared with the existing similar topologies. In other words, it attains the...
same voltage for a higher modulation index, which helps to obtain better output waveforms.

**B. Voltage stress across the power switches**

By substituting $N_f/N_i=100/35$ in (15), the voltage stress on the switches can be obtained as in (16). Note that $N_f/N_i=35/100$ is assumed for fair comparison as in [24].

$$V_{sw} = \frac{-1.85 + 4.7G}{3.85} V_{dc} \tag{16}$$

Fig. 4(c) compares the voltage stress across the power switches $V_{sw}$ for the proposed inverter and similar converters with various voltage gains. It can be found that the proposed inverter possesses lower voltages stress. Hence, the switches with lower power ratings can be employed in the proposed inverter, which results in lower power loss and cost.

**C. Current ripple of the input inductor**

The current ripple of the input inductor can be obtained as:

$$\Delta i_{L_1} = D T \frac{V_{L1}}{L_{1}} V_{dc} \tag{17}$$

During the ST mode, the voltage across the input inductor in the proposed inverter is equal to $(N/N-1)G V_{dc}$, while in the selected inverters, it is equal to $G V_{dc}$. The same value of input inductance, input dc-voltage, windings turns number, and switching period is assumed. As a result, the current ripple of the input inductor depends on the ST duty. In the case of the proposed inverter, the ST duty cycle is calculated as:

$$D = \frac{0.85G - 1.85}{4.7G - 1.85} \tag{18}$$

By substituting the ST duty cycle value from (18) into (17), considering the mentioned assumptions, and following the same way for the selected inverters, the normalized input current ripple versus the voltage gain can be plotted. Fig. 4(d) compares the input inductor currents ripples. The proposed inverter has a smaller input current ripple for the same voltage gain. Consequently, the proposed inverter can use a smaller inductor for the same current flow, which results in cost and size reduction. Finally, the table I provides a brief comparison between the proposed and conventional inverters.

**IV. PARAMETERS DESIGN OF THE PROPOSED INVERTER**

The magnetic parameters of the presented inverter are designed based on their maximum current ripple and voltage in ST interval. Accordingly, we can get the following equations where $%$ represents the maximum allowable current ripples of the inductors:

$$L_1 \geq \frac{V_{dc}^2 (-N D + N) D}{x%(N + D - 2N D - 2) P_o f_{sw}} \tag{19}$$

$$L_m \geq \frac{V_{dc}^2 (N - N D) N D^2}{x%(N + D - 2N D - 2)(1 + 2D - ND) P_o f_{sw}}$$

Additionally, the capacitive components of the proposed inverter are designed according to their maximum current, and voltage ripple in ST state. Hence, we have the following equations where $%$ presents the maximum allowable voltage ripples of the capacitors:

$$\frac{L_1}{L} \geq \frac{V_{dc}^2 (-N D + N) D}{x%(N + D - 2N D - 2) P_o f_{sw}}$$

$$L_m \geq \frac{V_{dc}^2 (N - N D) N D^2}{x%(N + D - 2N D - 2)(1 + 2D - ND) P_o f_{sw}}$$
\[
\begin{align*}
C_1 & \geq \frac{i_{C1}D}{\Delta V_{C1fsw}} = \frac{(N + D - 2ND - 2)P_0}{\gamma N V_{dc}^2 f_{sw}} \\
C_2 & \geq \frac{i_{C2}D}{\Delta V_{C2fsw}} = \frac{(N + D - 2ND - 2)P_0}{\gamma (1 - D)V_{dc}^2 f_{sw}} \\
C_3 & \geq \frac{i_{C3}D}{\Delta V_{C3fsw}} = \frac{(N + D - 2ND - 2)(1 - D)P_0}{\gamma (1 + D)V_{dc}^2 f_{sw}} \\
C_4 & \geq \frac{i_{C4}D}{\Delta V_{C4fsw}} = \frac{(N + D - 2ND - 2)2D P_0}{\gamma V_{dc}^2 f_{sw}} 
\end{align*}
\]

V. SIMULATION AND EXPERIMENTAL RESULTS

To validate the correctness of the proposed inverter, simulation results in MATLAB software, and experimental results attained from a 700 W laboratory prototype are provided. A picture of the hardware prototype of the proposed inverter is shown in Fig. 5. Particularly, the simple boost control is implemented by using the digital signal processor (DSP-TMS320F28335). The simulation and setup parameters are selected as follows: \(V_{in} = 100 \text{V}, C_1 = 120 \mu \text{F}, C_2 = 47 \mu \text{F}, C_3 = 330 \mu \text{F}, C_4 = 47 \mu \text{F}, L_1 = 300 \mu \text{H}, L_2 = 440 \mu \text{H}, L_3 = 100 \mu \text{H}, N_1 = 100/35, D = 0.1, M = 0.9, f_{sw} = 10 \text{kHz}, \) and \(f_{fs} = 60 \text{Hz} \). Diodes STBR3008WY and VS-150EBU04, and switches FGAF40N60UF are employed for the three-phase inverter. Figs. 5 and 6 show the simulation and experimental waveforms of the proposed topology, respectively. From the theoretical equations, simulation, and experimental results, the peak value of the dc-link voltage and phase output voltages of the proposed inverter are 486 V and 218 V as shown in Figs. 6(a), 6(b), and 7(a). Whereas for the same M and D values, the conventional counterpart inverter in [18] generates a dc link voltage of 382 V and output phase voltage of 171 V as shown in Figs. 6(a) and 6(b).

Fig. 5. Hardware prototype picture of the proposed inverter.
capacitors C1, C2, C3, and C4 are about 75 V, 237 V, 175 V, and 263 V, respectively, which has been proved through simulation and experimental results in Fig. 6(f), Fig. 7(b), and Fig. 7(c).

VI. POWER LOSSES ANALYSIS

The efficiency analysis of the proposed inverter is presented in this section. The principal power losses of the proposed inverter are generated by semiconductors, magnetic components, and ESR of the capacitors. The loss of the power switches comes from switching and conduction losses. From [26], the turn-off and turn-on switching power losses of the IGBTs can be gained as:

$$P_{\text{turn-off}} = P_{\text{turn-on}} = \frac{1}{2} c_{\text{CEO}} f_{\text{sw}} V_{\text{sw}}^2$$

(21)

Hence, the switching power loss of the IGBTs can be obtained as:

$$P_{\text{sw}} = P_{\text{turn-off}} + P_{\text{turn-on}} = \frac{3}{2} c_{\text{CEO}} f_{\text{sw}} V_{\text{sw}}^2$$

(22)

Since the $V_{\text{dc}}$ is the same as the dc-link voltage $V_i$, we can get:

$$P_{\text{sw}} = \frac{3}{2} c_{\text{CEO}} f_{\text{sw}} (V_i)^2 = \frac{3}{2} c_{\text{CEO}} f_{\text{sw}} \left(\frac{P_{\text{max}}}{K_f}\right)^2$$

(23)

Where $c_{\text{CEO}}$, $P_0$ and $I_0$ present the IGBTs junction capacitance, the output power and output dc-current of the proposed converter, respectively. From (10-13), the shoot-through current of the proposed converter is expressed by:

$$i_{\text{ST}} = \begin{cases} \frac{1 - D}{N D (1 - 2D)} I_i & 0 < t \leq DT \\ 0 & DT < t \leq T \end{cases}$$

(24)

Hence, the RMS value of the shoot-through current can be obtained as:

$$i_{\text{ST-rms}} = \frac{1}{T} \int_0^T i_{\text{ST}}^2 dt = \frac{1 - D}{N (1 - 2D) \sqrt{N}} I_i$$

(25)

The conduction loss of the IGBTs can be calculated from (26), where $R_s$ represents the ON-resistance of the power switches:

$$P_{\text{con}} = 6 R_s \left(\frac{i_{\text{ST-rms}}}{3}\right)^2 = \frac{2}{3} R_s \left\{\frac{(1 - D)^2 P_0^2}{N^2 (1 - 2D)^2 V_i^2}\right\}$$

(26)

From [26], the total power losses of the switches in inverter bridge can be obtained as:

$$P_{\text{S-tot}} = \frac{P_{\text{sw}}}{2} + P_{\text{con}} = \frac{3}{2} c_{\text{CEO}} f_{\text{sw}} \left(\frac{P_0}{K_f}\right)^2 + \frac{2}{3} R_s \left\{\frac{(1 - D)^2 P_0^2}{N^2 (1 - 2D)^2 V_i^2}\right\}$$

(27)

The loss of the diodes because of their forward voltage drop ($V_{\text{fD}}$) is attained as:

$$P_{\text{VD}} = \sum_{i=1}^3 V_{\text{fD}} I_{\text{Di}}$$

(28)

Where $I_D$ presents the diodes average currents. Additionally, the diodes power losses from their parasitic resistances can be gained as:

$$P_{\text{RD}} = \sum_{i=1}^3 R_{\text{rd}} I_{\text{Di-rms}}^2$$

(29)

Where $R_{\text{rd}}$ is the diodes' parasitic resistance. Likewise, the loss of the diodes' reverse recovery can be gained as:

$$P_{\text{RRD}} = \sum_{i=1}^3 Q_{\text{rr}} f_{\text{SW}} V_{\text{rrDi}}$$

(30)

In (30), $Q_{\text{rr}}$ and $V_{\text{rrD}}$ are the diodes reverse recovery charge and voltage, respectively. Hence, the total power losses of the diodes can be derived:

$$P_{D-tot} = P_{\text{VD}} + P_{\text{RD}} + P_{\text{RRD}}$$

$$= \sum_{i=1}^3 V_F I_{\text{Di}} + \sum_{i=1}^3 R_{\text{rd}} I_{\text{Di-rms}}^2 + \sum_{i=1}^3 Q_{\text{rr}} f_{\text{SW}} V_{\text{rrDi}}$$

(31)

Core losses, copper losses, and ESR losses from the inductors cause magnetic power losses. From [27], the input inductor and coupled transformer copper losses are obtained as follows:

$$P_{\text{cu-Li}} = \frac{\mu L_{\text{c}} W_A}{K_w W_A}$$

$$P_{\text{cu-T}} = \frac{\mu L_{\text{c}} (N_1^2 + N_2^2)}{K_w W_A}$$

(32)

(33)

Where $\mu$, $L_{\text{c}}$, $W_A$ are mean length per turns, wire effective resistivity, input inductor's RMS current, the primary winding turns number, secondary winding turns number, RMS current of primary winding, RMS current of the secondary winding, winding fill factor, and core window area, respectively. Moreover, the core loss of the coupled transformer is derived from (34):

$$P_{\text{fe}} = K_{\text{fe}} \cdot I_m \cdot A_c \cdot B_{\text{max}}^\beta$$

(34)

Where $K_{\text{fe}}$, $I_m$, $A_c$, $B_{\text{max}}$, and $\beta$ are core loss coefficient, mean magnetic path length, core cross-sectional area, peak ac flux density, and core loss exponent, respectively. Likewise, the ESRs of the magnetic components produce the power losses, which can be calculated from (35):

$$P_{\text{ESR-L}} = r_{\text{l1}} l_{\text{c-dc-rms}}^2 + r_{\text{n1}} I_{\text{n1-rms}}^2 + r_{\text{n2}} I_{\text{n2-rms}}^2$$

(35)

Hence, the total power losses of the magnetic components are derived as:

$$P_{\text{M-tot}} = P_{\text{cu-L1}} + P_{\text{cu-T}} + P_{\text{fe}} + P_{\text{ESR-L}}$$

(36)

Also, the power losses of the capacitors come from their ESRs:

$$P_{\text{C-tot}} = P_{\text{ESR-C}} = \sum_{i=1}^3 r_{\text{ci}} I_{\text{ci-rms}}^2$$

(37)

Finally, the total power losses of the proposed inverter can be obtained from (38):
\[ P_{\text{Loss-tot}} = P_{S-\text{tot}} + P_{D-\text{tot}} + P_{M-\text{tot}} + P_{C-\text{tot}} \] (38)

According to the theoretical equations, used components' datasheets, simulation values, and magnetic components' practical design, the efficiency of the proposed inverter can be measured. Furthermore, \( C_{CE}, F_{L1}, F_{N1}, F_{N2}, \) and \( F_{C} \) are assumed about 10 nF, 0.5 Ω, 0.4 Ω, 0.13 Ω, and 0.05 Ω, respectively. Fig. 8 shows an efficiency comparison between the proposed inverter and the conventional topologies in [19] and [24] at the various output powers. For a fair comparison, the same voltage boost factor \( (B= 4.86) \) with the equal ST duty ratio and modulation index are considered. It can be clearly found that the proposed inverter provides a higher efficiency, which is rooted in the fact that it employs a less number of windings turns. Positively, the proposed inverter can give higher efficiency with the same voltage gain, and equal windings turns number at the different ST duty ratios and modulation indexes. In this case, the proposed inverter offers lower conduction and switching losses due to the utilization of the much smaller ST duty cycle and higher modulation ratio. Fig. 9 shows the power loss distribution of the proposed inverter at \( P_{IN}=700 \) W. The power loss of switches, diodes, capacitors, and magnetic components are calculated about 28 W, 13 W, 8 W, and 42 W respectively. Thus, the total power loss is about 91 W and the efficiency is \( \eta=700/(700+91) = 88.5\% \).

![Fig. 8. Measured efficiency comparison.](image)

![Fig. 9. Power loss distribution in the proposed inverter at P_in=700W.](image)

**VII. CONCLUSION**

In this study, a modified three-phase inverter has been presented. The proposed inverter has a high voltage boost ability suitable for RES and ESS applications. It employs a Cockcroft-walton voltage multiplier cell along with the coupled inductors to obtain high voltage gain. Additionally, the proposed inverter offered the following properties.

- It draws a smooth input current with low ripple from the dc source, making it a good choice for PV systems. Likewise, the input inrush current is not huge, and the input LC filter is not required.
- Compared with the similar transformer-based inverters, it operates in the higher voltage operation range with the same turns number, lower switch voltage stress, and lower input current ripple.
- In the proposed inverter, a small ST duty cycle and high modulation ratio can be applied for the high voltage application. Hence, the output voltage quality can be improved in comparison with similar topologies.
- Due to the coupled inductors structure, higher voltage gain can be achieved by reducing the transformer turns number. Thus, the proposed inverter acquires the advantages in terms of cost, efficiency, voltage boost factor, and density points.
- A clamping circuit has been considered to absorb the leakage inductance energies of the coupled transformer. As a result, the dc-link voltage is clamped, and the voltage spikes across the power switches can be reduced.

To prove the effectiveness of the proposed inverter, simulation results have been presented. Moreover, a 700 W laboratory prototype has been implemented to verify the inverter's performance.

**REFERENCES**


