Cascaded Inverters Increasing the Number of Levels and Effective Switching Frequency in Output Using Coupled Inductors

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Abstract—In this paper, a new coupled-inductor based modular multilevel cascaded inverter using a new phase-shift control is presented. The proposed inverter can generate a high output ac voltage using standard low voltage rating devices. The number of levels in the output pulse width modulation (PWM) voltage and the effective switching frequency of the output filter are increased using coupled inductors and phase-shift control. The switching signals of the cascaded units in the proposed inverter are phase-shifted by $360/4n$, where $n$ is the number of cascaded units. The proposed phase-shift control results in $(4n+1)$ levels in the output PWM voltage of the proposed inverter and increases the effective switching frequency of the output filter by $4n$ times of the actual switching frequency $f_{sw}$. As a result, the output waveforms can be generated with better quality and less distortion. In addition, the output filter can be decreased dramatically in size. Besides, fewer coupled inductors are used to reduce the footprints, the number of inductors, and magnetic volume. Moreover, the proposed inverter is exceptionally reliable due to no short-circuit risk in the circuit.

Index Terms—Cascaded inverter, fewer coupled inductors, high reliability, multilevel, phase-shift.

I. INTRODUCTION

The two-level inverters are preferred in low voltage and low power applications. In high voltage and high-power applications [1], such as HVDC transmission [2], large motor drive [3], locomotive [4], solid-state transformers [5], pipeline pumps [6], water pumps [7], steel rolling mills [8], reactive power compensation [9, 10], and renewable energy [11] the multilevel inverters are preferred. A multilevel inverter synthesizes a staircase sinusoidal output voltage from several discrete voltage levels. The number of steps in the output voltage waveform increases with the number of discrete voltage levels. The higher the number of levels in the output voltage, the lower is the harmonic distortion. Thus, an output waveform with zero harmonic distortion can be synthesized by an infinite number of levels. The multilevel inverters increase the effective switching frequency of the output filter without increasing the actual switching frequency of the semiconductor devices. As a result, the output filter can be decreased in size. Besides, high efficiency, low electromagnetic noise, and low switching losses are the main benefits of multilevel inverters.

However, the maximum number of voltage levels in the output PWM waveform is limited due to the number of semiconductor devices, control, voltage imbalance issues, circuit layout, etc.

The famous multilevel inverters are the diode-clamp neutral point clamp (NPC) [12], flying-capacitors [13], and cascaded inverters with isolated dc sources [14-15]. An $n$-level diode-clamp inverter has $n-1$ dc-link capacitors and generates an output waveform with $n$-levels. It can increase the effective switching frequency of the output filter by $n$-times the actual switching frequency $f_{sw}$. In an $n$-level diode-clamp inverter with an input dc voltage $V_{dc}$, each capacitor has a voltage of $V_{dc}/(n-1)$. It has 2n-2 active switches and each switch blocks $V_{dc}/(n-1)$ voltage. The clamping diodes block unequal voltages, i.e., some diodes block high voltage and others block lower voltage. A five-level diode-clamp NPC inverter is shown in Fig. 1(a). It has eight switches $S_1-S_8$, and four dc-link capacitors $C_1-C_4$. The voltage across each capacitor is $V_{dc}/4$, and the voltage across each switch is limited to a capacitor voltage $V_{dc}/4$. The diodes $D_2$ and $D_4$ block $3V_{dc}/4$, $D_3$ and $D_5$ block $V_{dc}/2$, and $D_1$ and $D_6$ block $V_{dc}/4$. However, the diode clamp inverter is not modular and requires more components to generate the required number of levels in the output voltage.

An $n$-level flying-capacitor inverter has $n-1$ dc-link capacitors, $2n-2$ switches and generates an output PWM waveform with $n$-levels. It can increase the effective switching frequency of the output filter by $n$-times the actual switching frequency. Besides, it requires $(n-1)(n-2)/2$ flying capacitors of the same voltage stress. In an $n$-level flying-capacitor inverter with an input dc voltage $V_{dc}$ has voltage $V_{dc}/(n-1)$ across each capacitor. Each switch blocks $V_{dc}/(n-1)$ voltage. A five-level flying-capacitor inverter is shown in Fig. 1(b). It has eight switches $S_1-S_8$, four main dc-link capacitors $C_1-C_4$, and six flying capacitors $C_5-C_{10}$. The voltage across each capacitor is $V_{dc}/4$, and the voltage across each switch is limited to a capacitor voltage $V_{dc}/4$.

The H-bridge cascaded inverter [14-15] connects many H-bridge inverters in series as shown in Fig. 1(c). It is highly modular and has simple control. An $n$-level cascaded inverter with unipolar control has $2n-2$ switches and requires $(n-1)/2$ dc bus capacitors. It can be operated with phase-shifted bipolar or unipolar PWM control. In phase-shift bipolar control, the switching signals are phase-sifted by $360\degree/n$, and in phase-shift unipolar control, the switching signals are phase-sifted by $360\degree/2n$. An $n$-unit cascaded inverter using bipolar PWM generates an output PWM voltage with $n+1$ level.
the effective switching frequency of the output filter by \( n \) times the actual switching frequency. On the other hand, an \( n \)-unit cascaded inverter with unipolar PWM control generates an output PWM voltage with \( 2n+1 \) level. It increases the effective switching frequency of the output filter by \( 2n \) times the actual switching frequency. Therefore, the unipolar PWM results in lower power loss, smaller output filter, and high-power density. However, the H-bridge cascaded inverter requires more active switches to generate the required number of levels in the output voltage.

In the literature, many interesting multilevel inverter topologies have been presented to overcome the drawbacks of conventional multilevel inverters. In [16]-[21], switched-capacitor multilevel inverters are proposed, to decrease the number of required isolated sources. However, they require many circuit components which negatively affect the efficiency, cost, and power density. In [22], a level doubling inverter topology is presented which is a combination of an H-bridge inverter, half-bridge inverter and bidirectional switches. However, it has many switches, and switches withstand high voltage stress. In [23], a nine-level inverter with two DC sources, two flying capacitors, and eight switches is presented. However, it requires complex control techniques to balance the voltage of flying capacitors. In [24], another nine-level inverter derived from the H-bridge inverter is proposed. It has a simple structure, but the switches withstand high voltage stress. In [16], a thirteen-level inverter called a K-type inverter is presented. This inverter requires 14 switches, four DC sources and two flying capacitors. In [25], another thirteen-level inverter called E-type inverter is presented which has eight switches and four DC sources. The main drawback of this inverter is the use of many circuit components. Similarly, asymmetrical cascaded H-bridge inverter topologies [26], [27] and hybrid topologies [28-30] having different power cell configurations are developed. They decrease the number of isolated sources, but they are less modular than the conventional cascaded H-bridge inverters.

In all the aforementioned traditional inverters, the maximum number of levels in the output voltage is limited due to the number of semiconductor devices, control, voltage imbalance issues, circuit layout, etc. Besides, they have a common problem of short-circuit which results in lower reliability. To decrease the risk of short-circuit, the dead time is used in the switching signals. However, dead time decreases the achievable voltage gain and distorts the output waveforms. Therefore, the dual-buck single-phase [31-33], three-phase [34], cascaded inverters [35], and couple-inductor inductor-based inverters [36-38] have been developed.

![Fig. 1. Multilevel inverters. (a) Five-level diode-clamp NPC inverter. (b) Five-level flying-capacitor inverter. (c) n-unit cascaded inverter using the proposed phase-shift control and fewer coupled inductors.](image)

![Fig. 2. Block diagram for the gate signals generation of the proposed 2-unit couple-inductor cascaded inverter.](image)

![Fig. 3. Gate signals generation of the proposed 2-unit cascaded inverter.](image)

The dual-buck cascaded inverter in [35] has no short-circuit risk. However, an \( n \)-unit cascaded dual-buck inverter same as the H-bridge cascaded inverter generates only \( n+1 \) levels in output voltage, and its effective switching frequency of the output filter is \( n f_{SW} \). In [39], a hybrid coupled-inductor and cascaded H-bridge multilevel inverter is proposed. It could increase the number of levels in output, however it suffers from short-circuit issues, required dead-time in the switching signals and can cause reverse recovery issues of MOSFET body diodes.

An H-bridge inverter with phase-shift unipolar control results in a three-level output PWM voltage. To increase the number of levels in the output PWM voltage without increasing the number of active switches, coupled inductor inverters have been developed in [36-38]. However, they require two coupled inductors per unit which increases the magnetic volume. Also, they are suitable for low power as the semiconductor devices must withstand a high input voltage to generate a high output ac voltage.

In this paper, a new cascaded inverter is presented. Also, a new phase-shift control is developed for its proper operation. The proposed \( n \)-unit cascaded inverter has the following advantages:

1. **Higher Voltage Gain:**
   - Each unit generates a higher voltage level compared to the previous one.
   - The total voltage level is the sum of the individual levels.

2. **Reduced Number of Devices:**
   - Fewer semiconductor devices are required compared to the number of levels.
   - Lower cost and complexity.

3. **Improved Efficiency:**
   - Lower power loss due to reduced switching frequency.
   - Better current sharing among the units.

4. **Robustness:**
   - Increased reliability due to the modular structure.
   -容错能力增强

5. **Modularity:**
   - Easy scalability by adding or removing units.

These advantages make the proposed cascaded inverter suitable for various applications requiring multilevel voltage output.
Fig. 4. Operation modes of the proposed 2-unit cascaded inverter. (a) $v_{an} = 0$. (b) $v_{an} = 0.5V_{dc}$. (c) $v_{an} = V_{dc}$. (d) $v_{an} = 1.5V_{dc}$. (e) $v_{an} = 2V_{dc}$. (f) $v_{an} = -0.5V_{dc}$. (g) $v_{an} = -V_{dc}$. (h) $v_{an} = -1.5V_{dc}$. (i) $v_{an} = -2V_{dc}$.

Fig. 5. Comparison of the output filter inductor ($L_f$) voltages of the 2-unit phase-shifted cascaded inverters. (a) Traditional inverter with bipolar PWM control. (b) Traditional inverter with unipolar PWM control. (c) Proposed inverter with the proposed phase-shift control.

Fig. 6. Comparison of the output PWM voltage ($v_{an}$) of the 2-unit phase-shifted cascaded inverters. (a) Traditional inverter with bipolar PWM control. (b) Traditional inverter with unipolar PWM control. (c) Proposed inverter with the proposed phase-shift control.

1. It generates the most levels in output voltage waveform with the lowest number of switches. It generates a $4n+1$ level in the output voltage waveform.
2. It increases the effective switching frequency of the output filter by $4n$ times the actual switching frequency of the semiconductor devices. Besides, it decreases the voltage across the output filter inductor. As a result, the output filter can be decreased dramatically in size.
3. It has no short-circuit risk in the circuit. As a result, an exceptionally reliable inverter can be obtained.
4. The current freewheels through the external diodes, which can decrease the overall power loss.
5. Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) can be used without reverse recovery issues.

II. PROPOSED INVERTER AND ITS PHASE-SHIFTED CONTROL

The proposed $n$-unit cascaded inverter is shown in Fig. 1(d). It connects $n$ units in series. The coupled inductors are shared between the units to decrease the number of coupled inductors, magnetic volume, footprints, soldering connections, conduction...
losses and cost. The total number of coupled inductors in the proposed inverter is \( n+1 \). The proposed inverter requires \( n-1 \) fewer coupled inductors than the cascaded inverter based on the inverter in [36–38].

The proposed inverter can obtain peak output voltage \( \sum_{i=1}^{n} V_{dc i} \) where \( V_{dc 1} \cdot V_{dc 2} \cdot \ldots \cdot V_{dc n} \) are the input dc voltages of the unit 1, 2, \ldots, and \( n \), respectively. As shown in each phase leg an active switch is connected in series with an external diode. Therefore, the proposed inverter is free of short-circuiting. The current freewheels through the external diodes, which can decrease the reverse recovery loss and related issues.

A new phase-shifted PWM control scheme is developed for the proposed inverter in which the switching signals of the back-to-back cascaded units are phase-shifted by \( 360^\circ/4n \). The phase-shift of the carrier or switching signals can be obtained through the following generalized relations.

\[
\begin{align*}
S_{4N-3} &= 360^\circ \times \frac{N-1}{4n}, N \leq n \\
S_{4N-2} &= 360^\circ \times \frac{N+2n-1}{4n}, N \leq n \\
S_{4N-1} &= 360^\circ \times \frac{N+3n-1}{4n}, N \leq n \\
S_{4N-4} &= 360^\circ \times \frac{N+n-1}{4n}, N \leq n
\end{align*}
\]

where \( n \) is the total number of units, and \( N \) is the number of unit under consideration in the proposed cascaded inverter. For example, for a 3-unit cascaded inverter, \( n = 3 \), and \( N \) is 1, 2, and 3 for \( 1^\text{st} \), \( 2^\text{nd} \) and \( 3^\text{rd} \) unit, respectively. The block diagram of the generation of the switching signal for the proposed 2-unit cascaded inverter is shown in Fig. 2. The switching signals of switch \( S_1 \), \( S_2 \), \( S_3 \), \( S_4 \), \( S_5 \), \( S_6 \), \( S_7 \), and \( S_8 \) are obtained by comparing \( v_{\text{ref}} \) with carrier signals \( v_{\text{tr1}}, v_{\text{tr2}}, v_{\text{tr3}}, v_{\text{tr4}}, v_{\text{tr5}}, v_{\text{tr6}}, v_{\text{tr7}}, \) and \( v_{\text{tr8}} \), respectively as shown in Fig. 2. Note that the reference and carrier signals are in 1st quadrant. The signals \( v_{\text{tr2}}, v_{\text{tr3}}, v_{\text{tr4}}, v_{\text{tr5}}, v_{\text{tr6}}, v_{\text{tr7}}, \) and \( v_{\text{tr8}} \) are phase-shifted by \( 180^\circ, 270^\circ, 90^\circ, 45^\circ, 225^\circ, 315^\circ, \) and \( 135^\circ \), respectively. The switching signals of the 2-unit cascaded inverter are given in Fig. 3. The operation modes of the proposed 2-unit cascaded inverter with nine levels in the output voltage are shown in Fig. 4. The switching states and output voltage levels for the operation modes in Fig. 4 are given in Table I.

### III. COMPARISON OF THE PROPOSED AND CONVENTIONAL CASCAD INVERTERS

In this section, the proposed and conventional 2-unit cascaded inverters are compared. The conventional inverter is operated with phase-shift bipolar and unipolar PWM controls. In the phase-shift bipolar and unipolar PWM controls, the switching signals of the back-to-back connected units are phase-shifted by 180° and 90°, respectively. The switching signals of the back-to-back connected units in the proposed inverter are phase-shifted by 45°.

#### A. Comparison of the Output Inductor Voltage

Fig. 5 compares the voltage (\( v_L \)) of the output filter inductor (\( L_f \)) in the proposed and conventional inverters. Fig. 5(a) shows the voltage across the output inductor \( L_f \) in the conventional inverter with the bipolar control, where \( v_o \) is the output voltage after the filter, and \( V_{dc} \) is the input voltage of each unit. The inductor voltage has three discrete levels \( 2V_{dc} - v_o, -v_o, \) and \(-2V_{dc} - v_o \). The voltage swing across the inductor is \( 2V_{dc} \). Fig. 5(b) shows the voltage across the output inductor \( L_f \) in the conventional inverter with the unipolar control. The inductor voltage has five discrete levels \(-v_o, V_{dc} - v_o, 2V_{dc} - v_o, -V_{dc} - v_o, \) and \(-2V_{dc} - v_o \). The voltage swing across the inductor is \(-V_{dc} \). Fig. 5(c) shows the voltage across the output inductor \( L_f \) in the proposed cascaded inverter. The inductor voltage has nine discrete levels \(-v_o, 0.5V_{dc} - v_o, V_{dc} - v_o, 1.5V_{dc} - v_o, 2V_{dc} - v_o, -0.5V_{dc} - v_o, -V_{dc} - v_o, -1.5V_{dc} - v_o, \) and \(-2V_{dc} - v_o \). The voltage swing across the inductor in the proposed inverter is 0.5\( V_{dc} \).

#### B. Comparison of the Output PWM Voltage

Fig. 6 compares the output PWM voltage waveforms. The output voltage of the conventional inverter with bipolar PWM control has three discrete levels \( 2V_{dc}, 0 \) and \(-2V_{dc} \) and with unipolar PWM control has five discrete levels \( 2V_{dc}, V_{dc}, 0, -V_{dc}, \) and \(-2V_{dc} \). The output voltage of the proposed inverter with the proposed control has nine discrete levels \( 2V_{dc}, 1.5V_{dc}, V_{dc}, 0.5V_{dc}, 0, -0.5V_{dc}, -V_{dc}, 1.5V_{dc}, \) and \(-2V_{dc} \). The number of levels in the output voltage of the conventional H-bridge and proposed inverters are given in (6)-(7) and plotted in Fig. 7(a).

\[
\begin{align*}
V_{\text{conv.bipolar}} &= n + 1 \\
V_{\text{conv.unipolar}} &= 2n + 1 \\
V_{\text{proposed}} &= 4n + 1
\end{align*}
\]

For the same number of cascaded units, the proposed inverter produces a lot more levels. For example, for a 10-unit cascaded inverter, the conventional inverter produces 11 and 21 levels with the bipolar and unipolar PWM controls, respectively. On the other hand, the proposed inverter produces 41 levels in the output voltage.

![Fig. 7. (a) Comparison of the levels in the output PWM voltages. (b) Comparison of the effective switching frequencies of the output filter.](https://www.ieee.org/publications/rights/index.html for more information.)
C. Comparison of the Effective Switching Frequency of the Output Filter Inductor

The effective switching frequencies of the output filter in the conventional inverter with bipolar and unipolar phase-shift PWM controls are \( n_{f_{sw}} \) and \( 2n_{f_{sw}} \), respectively. Whereas the effective switching frequency of the output filter in the proposed inverter is \( 4n_{f_{sw}} \). Fig. 7(b) compares the effective switching frequencies of the output filter inductor. As shown the effective switching frequency of the output filter in the proposed inverter is higher than the conventional inverter. For example, for a 10-unit cascaded inverter, the effective switching frequency of the output filter inductor in the proposed inverter is \( 40f_{sw} \), whereas for the conventional inverter, it is \( 10f_{sw} \) and \( 20f_{sw} \) with bipolar and unipolar control, respectively. Thus, due to the higher effective switching frequency and the lower voltage of the output inductor in the proposed inverter, it can be designed much smaller in size.

IV. ANALYSIS AND COMPARISON OF THE OUTPUT INDUCTOR CURRENT RIPPLES

The current ripple analysis is carried out for the positive half-cycle of the output current. A similar analysis can be done for the negative half-cycle of the output current.

A. Conventional Cascaded Inverter Using Bipolar PWM Control

The current ripple of the conventional 2-unit cascaded inverter using phase-shift bipolar control can be obtained as

\[
\Delta i_{L_{Con,bi}} = \frac{(2V_{dc} - v_o)(D - \frac{1}{2})T_s}{L}, 0.5 \leq D \leq 1 \tag{8}
\]

where \( T_s = 1/f_{sw} \) is the switching time period. The duty ratio \( D \) of the inverter is derived in (9).

\[
D = \frac{\sin(\omega t) + 1}{2} \tag{9}
\]

The output voltage of the 2-unit cascaded inverter is

\[
v_o = 2M \sin(\omega t) \tag{10}
\]

where \( M \) is the modulation index. By putting (9) and (10) in (8) and rearranging we obtained

\[
\Delta i_{L_{Con,bi}} = \frac{V_{dc}T_s}{L}(\sin(\omega t) - M\sin^2(\omega t)), 0 \leq \omega t \leq \pi \tag{11}
\]

B. Conventional Cascaded Inverter Using Unipolar PWM Control

The current ripples of the conventional inverter using phase-shift unipolar control is expressed in (12).

\[
\begin{aligned}
\Delta i_{L_{Con,up}} &= \frac{(V_{dc} - v_o)(D - \frac{1}{2})T_s}{L}, & 1/2 \leq D \leq 3/4 \tag{12} \\
\Delta i_{L_{Con,up}} &= \frac{(2V_{dc} - v_o)(D - \frac{3}{4})T_s}{L}, & 3/4 \leq D \leq 1
\end{aligned}
\]

By putting (9) and (10) in (12) and rearranging we obtained (13).

C. Proposed Cascaded Inverter

The inductor current ripples of the proposed inverter are derived as given in (14). Putting (9) and (10) in (14) and rearranging we obtained (15). The inductor current ripples of the conventional and proposed inverters from (11), (13), and (15) are normalized to \( V_{dc}T_s/L \) and plotted in Fig. 8(a).

As shown the current ripple of the proposed inverter is dramatically smaller than the conventional inverter. The ratios of the inductor ripples from (11), (13), and (15) are given in (16) and (17) and plotted in Fig. 8(b). As shown the inductor current ripples of the conventional inverter are much larger than the proposed inverter.

For example, for \( D=0.6 \), the inductor current ripple of the conventional inverter with bipolar and unipolar PWM controls are 90 and 40 times larger than the proposed inverter.

D. Comparison of the Simulated Output Inductor Current Ripples

Fig. 9 compares the PSIM simulated output inductor currents. The input voltage \( V_{dc} \) of each unit is 330 V, the output voltage is 420 Vrms, switching frequency is 50 kHz, output power is 4 kW, line-frequency is 60 Hz and inductance of the output inductor is 50 \( \mu \)H. The peak current ripple of the conventional inverter with bipolar and unipolar control is 28 A and 12 A, respectively. Whereas the peak inductor current ripple of the proposed inverter is only 0.5 A.
Design of Coupled Inductors

The four possible switching states of a switching cell in a switching cycle are shown in Fig. 10. In state 1 shown in Fig. 10(a), \( S_1 \) is ON, \( S_2 \) is OFF, \( D_1 \) is ON, and \( D_2 \) is OFF. In state 2 shown in Fig. 10(b), \( S_1 \) and \( S_2 \) are OFF, \( D_1 \) and \( D_2 \) are ON. In state 3 shown in Fig. 10(c), \( S_1 \) is OFF, \( S_2 \) is ON, \( D_1 \) is OFF, and \( D_2 \) is ON. In state 4 shown in Fig. 10(d), \( S_1 \) and \( S_2 \) are ON, \( D_1 \) and \( D_2 \) are OFF. As shown by the red colour in Fig. 10, a circulating \( i_{\text{circ}} \) is produced. The coupled inductor protects the circulating current. The coupled inductor model is shown in Fig. 11. The leakage inductance of the primary and secondary windings are given by \( L_{\text{IR1}} \) and \( L_{\text{IR2}} \), and the magnetizing inductance is shown by \( L_{\text{cm}} \). As shown in Fig. 11, the circulating current \( i_{\text{cm}} \) is opposed by \( L_{\text{IR1}} \), \( L_{\text{IR2}} \), and \( 4L_m \). Therefore the circulating current ripple can be obtained as

\[
\frac{di_{\text{circ}}}{dt} = \frac{V_{dc}}{L_{\text{IR1}} + L_{\text{IR2}} + 4L_m} = \frac{V_{dc}}{4L_o}
\]  

For \( L_{\text{IR1}} = L_{\text{IR2}} \), the magnetizing inductance \( (L_m) \) is same as the self-inductance \( (L_o) \). Fig. 12 shows the design of a coupled inductor with EE and PQ cores. The leakage inductance does not affect the inverter.

\[
\begin{align*}
\Delta i_{\text{L_con,up}} &= \frac{V_{dc}T_s}{L} \left( 0.5 \sin(\omega t) - M \sin^2(\omega t) \right), \quad 0 \leq \omega t \leq 3.141 \\
\Delta i_{\text{L_con,up}} &= \frac{V_{dc}T_s}{L} \left( \sin(\omega t) + 0.5M \sin(\omega t) - M \sin^2(\omega t) - 0.5 \right), \quad 0.523 \leq \omega t \leq 3.141 \\
\Delta i_{\text{L1}} &= \frac{V_{dc}T_s}{L} \left( \frac{1}{4} - M \sin(\omega t) \right) \sin \left( \omega t - \frac{1}{4} \right), \quad 0 \leq \omega t < 0.252 \\
\Delta i_{\text{L2}} &= \frac{V_{dc}T_s}{L} \left( \frac{1}{4} - M \sin(\omega t) \right) \sin \left( \omega t - \frac{1}{4} \right), \quad 0.252 \leq \omega t < 0.523 \\
\Delta i_{\text{L3}} &= \frac{V_{dc}T_s}{L} \left( \frac{3}{4} - M \sin(\omega t) \right) \sin \left( \omega t - \frac{1}{2} \right), \quad 0.523 \leq \omega t < 0.848 \\
\Delta i_{\text{L4}} &= \frac{V_{dc}T_s}{L} \left( \frac{3}{4} - M \sin(\omega t) \right) \sin \left( \omega t - \frac{3}{4} \right), \quad 0.848 \leq \omega t < 1.57
\end{align*}
\]

\[
\begin{align*}
\Delta i_{\text{L_con,bp}} &= \frac{1}{4} - M \sin(\omega t), \quad 0 \leq \omega t < 0.252 \\
\Delta i_{\text{L1}} &= \frac{1}{4} - M \sin(\omega t), \quad 0 \leq \omega t < 0.252 \\
\Delta i_{\text{L2}} &= \frac{1}{4} - M \sin(\omega t), \quad 0 \leq \omega t < 0.252 \\
\Delta i_{\text{L3}} &= \frac{1}{4} - M \sin(\omega t), \quad 0 \leq \omega t < 0.252 \\
\Delta i_{\text{L4}} &= \frac{1}{4} - M \sin(\omega t), \quad 0 \leq \omega t < 0.252 \\
\Delta i_{\text{L_con,bp}} &= \frac{1}{4} - M \sin(\omega t), \quad 0 \leq \omega t < 0.848 \\
\Delta i_{\text{L1}} &= \frac{1}{4} - M \sin(\omega t), \quad 0 \leq \omega t < 0.252 \\
\Delta i_{\text{L2}} &= \frac{1}{4} - M \sin(\omega t), \quad 0 \leq \omega t < 0.252 \\
\Delta i_{\text{L3}} &= \frac{1}{4} - M \sin(\omega t), \quad 0 \leq \omega t < 0.252 \\
\Delta i_{\text{L4}} &= \frac{1}{4} - M \sin(\omega t), \quad 0 \leq \omega t < 0.252 \\
\end{align*}
\]
Fig. 12. Design of the coupled inductor. (a) EE cores. (b) PQ cores.

performance. However, the leakage inductance can be well decreased by tightly winding the coils as shown in Fig. 12. The air gap ($l_{g}$) is inserted in the cores to avoid core saturation due to current. In PQ core air gap is in the central leg, and there is no airgap in the external legs. The core area of the central leg is ($A_{c}$) and that of the external legs is ($A_{e}/2$). Where as in the EE core, the air gap ($l_{g}$) is divided into ($l_{g} / N_{p}$) and inserted in both external legs. The core area is $A_{e}$. A coupled inductor has two windings, primary with turns ($N_{p}$) and secondary with turns ($N_{s}$). In PQ core, both windings are placed on the central leg as shown in Fig. 12(b). The magnetic flux produced by $N_{p}$ is shown by $\varphi_{1}$ and the flux produced by $N_{s}$ is shown by $\varphi_{2}$.

In EE core, $N_{p}$ is placed on the leftmost leg and $N_{s}$ is placed on the rightmost leg. In both cores the fluxes of the primary and
secondary turns are getting added. By assuming \( N_p = N_s \), the self inductance is given by the following equation

\[
L = \frac{\mu_o N^2 A_e}{l_g}
\]

where \( \mu_o \) is the permeability of free space and its value is \( 4\pi \times 10^{-7} \). For a given ripple of circulating current, the self inductance from (18) is obtained 0.2 mH. The air gap \( (l_g) \) in the magnetic core can be calculated from the following equation

\[
I_{L,sat} = \frac{B_{max} l_g}{\mu_o N}
\]

where \( I_{L,sat} \) is the inductor saturation current, and \( B_{max} \) is the maximum flux density of magnetic core. For \( \text{PQ5050} \), \( A_e = 332 \text{ mm}^2 \) and \( B_{max} \approx 0.2\sim0.4 \). For \( N=27 \), \( l_g = 1.5 \text{ mm} \), \( A_e = 332 \text{ mm}^2 \) and \( \mu_o = 4\pi \times 10^{-7} \), \( L \) is obtained around 0.2 mH. Similarly, the inductor can be designed with the EE cores. The leakage inductance can be extremely small with the PQ cores by winding both coils on the centre leg as shown in Fig. 12(b).

The proposed cascaded inverter is also extended into a three-phase cascaded inverter as shown in Fig. 13. It can generate a three-phase output voltage. Fig. 14 shows the simulation results of the proposed three-phase cascaded inverter for the same specifications as in Table II except the output power and voltage. The output power for the three-phase inverter is 12 kW, input dc voltage is 330 V and the output voltage is 440 Vrms. Fig. 14(a) shows the output three-phase voltages \( (v_{oa}, v_{ob}, \text{and } v_{oc}) \) and input voltage \( (V_{dc}) \). Fig. 14(b) shows the output three-phase currents \( (i_{oa}, i_{ob}, \text{and } i_{oc}) \). Fig. 14(c) shows the output three-phase PWM voltages \( (v_{an}, v_{bn}, \text{and } v_{cn}) \) before the filter. Fig. 14(d) shows the expanded results of Fig. 14(c).

### Table II. Parameters of the Experimental Prototype

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-bus voltage</td>
<td>( V_{dc} )</td>
<td>330 V</td>
</tr>
<tr>
<td>Coupled inductors</td>
<td>( L_L )</td>
<td>0.2 mH</td>
</tr>
<tr>
<td>Output main inductor</td>
<td>( L_f )</td>
<td>0.05 mH</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>( f_{sw} )</td>
<td>50 kHz</td>
</tr>
<tr>
<td>Line-frequency</td>
<td>( f )</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Rated output voltage</td>
<td>( V_o )</td>
<td>420 Vrms</td>
</tr>
<tr>
<td>MOSFETS</td>
<td>( S_1 - S_8 )</td>
<td>47N60CFD</td>
</tr>
<tr>
<td>Output capacitor</td>
<td>( C_f )</td>
<td>0.47 ( \mu F )</td>
</tr>
<tr>
<td>Diodes</td>
<td>( D_1 - D_8 )</td>
<td>RHRRG3060</td>
</tr>
<tr>
<td>Controller</td>
<td></td>
<td>TMS320F28335</td>
</tr>
<tr>
<td>Gate driver</td>
<td></td>
<td>VLAB502-01</td>
</tr>
<tr>
<td>Rated output power</td>
<td>( P_o )</td>
<td>4 kW</td>
</tr>
</tbody>
</table>

### Table III

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power MOSFET S1-S4</td>
<td>47N60CFD</td>
<td></td>
</tr>
<tr>
<td>Power Diode D1-D4</td>
<td>RHRRG3060</td>
<td></td>
</tr>
<tr>
<td>Output inductor</td>
<td>( L_f )</td>
<td>CM400060</td>
</tr>
<tr>
<td>Coupled inductors</td>
<td>( L_L )</td>
<td>PQ5050</td>
</tr>
<tr>
<td>Conduction resistance of output inductor</td>
<td>30 m( \Omega )</td>
<td></td>
</tr>
<tr>
<td>Conduction resistance of each winding of coupled inductor</td>
<td>47 m( \Omega )</td>
<td></td>
</tr>
<tr>
<td>RMS current of output inductor</td>
<td>9.67 A</td>
<td></td>
</tr>
<tr>
<td>RMS current of each winding of coupled inductor</td>
<td>4.9 A</td>
<td></td>
</tr>
</tbody>
</table>

The power loss breakdown of the proposed 2-unit cascaded inverter is conducted in the thermal module of the PSIM as shown in Fig. 15. The circuit components are first modelled in the thermal module using data from the data sheets and experiments. The parameters for power loss distribution is shown in Table III. The body diodes loss is zero because no current flow through the body diodes. Finally, a comparison of the proposed and conventional inverters is given in Table IV. The efficiency of the proposed inverter is higher for the following reasons.

- In the proposed inverter, body diodes do not conduct, therefore the reverse recovery loss and issues of body diodes are eliminated. The external freewheeling diodes

![Fig. 13. Proposed coupled-inductor three-phase inverter.](image)

![Fig. 14. Simulation results of the proposed 2-unit cascaded three-phase inverter.](image)

![Fig. 15. Power loss breakdown of the proposed 2-unit cascaded inverter for input dc voltage 330 V, output voltage 420 Vrms and output power 4 kW.](image)
conduct in the proposed inverter, which has negligible reverse recovery issues and low forward voltage drop. Whereas in the conventional MLIs, the body diodes of switches conduct, which has higher reverse recovery issues and power loss.

- The conventional inverters require finite dead time (1 μs is used in PSIM simulations for efficiency estimation), which decreases the output voltage. In order to obtain the same voltage as the proposed inverter, the input voltage for the conventional inverters is increased which increases the power loss due to higher voltage and current stresses of components in the conventional inverters. On the other hand the proposed inverter do not have delays in switching signals (equivalent to dead time in conventional MLIs).
- The proposed inverter can use MOSFETs without reverse recovery issues, whereas the conventional MLIs causes higher reverse recovery issues of MOSFET body diodes.

The THD of the proposed inverter is higher compared to the conventional MLIs. Because, the conventional inverters require finite dead time (1 μs is used in PSIM simulations for efficiency estimation), which causes distortion in the output voltage. During the dead-time energy does not transfer to output. On the other hand the proposed inverter do not have delays in switching signals (equivalent to dead time in conventional MLIs).

V. EXPERIMENTAL RESULTS

A 4-kW hardware prototype of the proposed 2-unit cascaded inverter is fabricated and tested as shown in Fig. 16. The electrical specifications are given in Table II. The switching signals are phase-shifted by 45° as given in Figs. 2 and 3. The gatesource switching signals \(v_{GS1}, v_{GS2}, v_{GS5},\) and \(v_{GS6}\) of the switch \(S_1, S_2, S_5\) and \(S_6\), respectively are shown in Fig. 17(a). The zoom-in waveforms of Fig. 17(a) are shown in Fig. 17(b). The control signal of switch \(S_5\) is shifted by 45° to the control signal of \(S_1\). The control signal of switch \(S_6\) is shifted by 45° to the control signal of \(S_2\). It can also be seen that the switch \(S_1\) and \(S_2\) are working with four states in a switching cycle. State 1 (\(S_5\) is ON, \(S_6\) is OFF), state 2 (\(S_5\) and \(S_6\) both are ON), state 3 (\(S_1\) is ON, \(S_5\) is OFF), and state 4 (\(S_5\) and \(S_6\) both are OFF).

Fig. 18(a) shows the experimental results of the output inductor current \(i_f\), and drain-source voltage \(v_{DS1}\) and \(v_{DS2}\) of switch \(S_1\) and \(S_2\), respectively. Fig. 18(b) shows the expanded waveforms of the results in Fig. 18(a). As shown the output inductor current increases and decreases eight times in a switching cycle of the semiconductor switches, which confirms that the effective switching frequency of the output inductor in the proposed 2-unit cascaded inverter is eight times (400 kHz) the actual switching frequency (50 kHz). The results in Fig. 18 also confirmed that the proposed inverter works well without short-circuiting issues even when all the switches in the same phase leg are turned on.
Fig. 20. Experimental results of the winding currents of the coupled inductors.

Fig. 19(a) shows the experimental results of the input voltage $V_{dc}$ and output voltage before the filter $v_{an}$ and after the filter $v_o$. As shown the output voltage before the filter $v_{an}$ has nine-levels which confirms the previous analysis in section IV. The output voltage after the filter $v_o$ has less distortion due to no delays in the switching signals. Fig. 19(b) shows the experimental results of the output voltage $v_o$, output current $i_o$, and drain-source voltage $v_{DS7}$ and $v_{DS8}$ of switch $S7$ and $S8$ with a partially inductive load for power factor 0.81. The results in Fig. 19(b) confirms that the proposed inverter can provide reactive power. Fig. 20 shows the currents of the coupled inductor. It has no negative current which confirms that the body diodes of the MOSFETs are OFF. Fig. 21 shows the voltage and current of the output filter inductor. As shown the inductor voltage is much lower.

Fig. 22 shows the dynamic experimental results of the proposed inverter for a sudden change in output voltage. At the time instant $t0$, the output voltage drops from 420 Vrms to 210 Vrms, and at the instant $t1$, the output voltage rises from 210 Vrms to 420 Vrms. As shown the proposed inverter works well with a change in output voltage.

Fig. 23 compares the output PWM voltage of the proposed and conventional inverters. As shown the conventional 2-unit cascaded H-bridge inverter with unipolar PWM control generates five levels in output voltage, whereas the proposed inverter generates nine levels in output PWM voltage. Fig. 24(a) compares the total harmonic distortion (THD) of the proposed and conventional inverters. The THD of the conventional cascaded H-bridge inverter is much higher because of 1 us dead time in its switching signals. The THD of the proposed inverter is much lower because the proposed inverter has no delays (equivalent to dead time) in the control signals. The measured efficiency of the proposed inverter is shown in Fig. 24(b). Its peak efficiency is 97.8%.

VI. CONCLUSION

In this paper, a new cascaded inverter is proposed to increase the number of levels in the output using coupled inductors and a new type of phase-shift control. The proposed inverter inherits the benefits of the conventional cascaded inverters such as high modularity and generating a higher output ac voltage using low voltage rating devices. In addition, the proposed inverter has the following main features.

1. It generates the most levels in output voltage with the lowest number of switches. The proposed $n$-unit cascaded inverter generates a $4n+1$ level in the output voltage waveform.
2. It increases the effective switching frequency of the output filter by $4n$ times the actual switching frequency of the semiconductor devices. Besides, it decreases the voltage
across the output filter inductor. As a result, the output filter can be decreased dramatically in size.

3. It has no short-circuit risk in the circuit.

4. In the proposed inverter, delays in the switching signals can be eliminated to improve the quality of output waveforms.

5. In the proposed inverter, the body diodes of the switches do not conduct, therefore MOSFETs can be used without reverse recovery issues of the body diodes.

To validate the benefits of the proposed inverter, a 4 kW hardware prototype of the proposed 2-unit cascaded inverter is constructed and tested using various loads for 330 V input voltage and 420 Vrms/60 Hz output voltage. It is verified that the proposed 2-unit cascaded inverter generates a nine-level output voltage and increases the effective switching frequency of the output filter by eight times the actual switching frequency of 50 kHz. The output voltage has been obtained with less total harmonic distortion of about 1%. Peak efficiency of 97.8% is obtained with the proposed inverter.

In future work, the proposed three-phase cascaded inverters will be analyzed and designed. In addition, the magnetic components will be integrated to reduce the magnetic volume.

REFERENCES


