Supporting Information

Ultrafast and ultralow power voltage-dominated magnetic logic

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S1. Design of magnetic components and voltage-dominated negative differential resistance

For our magnetic components, a perpendicular magnetically anisotropic\textsuperscript{[22]} multilayer of Ta/CoFeB/MgO was used. In magnetic materials, a Hall voltage perpendicular to the applied current is associated with magnetization because of the anomalous Hall effect, which results in an imbalance of the left voltage and right voltage in our three-terminal device (Figure S1a). However, the voltage imbalance caused by the anomalous Hall voltage\textsuperscript{[23]} is only \(~0.4\%\) (Figure S1b). Magnetic components helped to realize reconfigurable logic operations via the anomalous Hall effect and offered non-volatile memory stored in the magnetization direction of up or down. Therefore, our magnetic components served as both magnetic input and output bits, realizing logic operations and magnetic storage. The magnetization should be stable in the logic operations for magnetic input bits, while the magnetization should be switched via spin-orbit torque in the magnetic storage for magnetic output bits. The current flowed from left to right electrodes and was co-linear with the longitudinal magnetic field in both logic operations and magnetic storage. As the current inside the magnetic input is not used to switch the magnetic output directly, this current can be much smaller than the critical current, so that the spin-orbit torque effect is not useable in logic operations. On the other hand, the output current was controlled by the MOSFET, and was larger than the critical current, resulting in magnetic switching.

To improve the output ratio, voltage-controlled N-type negative differential resistance (NDR) was introduced into the magnetic component. This phenomenon can be observed in many solid-state devices, such as resonant tunneling diodes\textsuperscript{[24]} (RTDs), IMPact ionization Avalanche Transit-Time (IMPATT) diodes\textsuperscript{[25]}, Gunn diodes\textsuperscript{[26]}, and circuits consisting of bipolar junction transistors (BJTs), or junction-gate field-effect transistors (JFET) or metal-oxide-semiconductor field-effect transistors (MOSFETs)\textsuperscript{[15]}. For the results reported in the main text, in order to investigate the minimum switching time of our magnetic logic device a resonant tunneling diode (TD261 produced by New Jersey Semi-conductor Products, Inc) was chosen for the basic logic operations (Figure S2a). For simplicity and stability, we chose circuits consisting of two complementary junction-gate field-effect transistors (2SK170 and 2SJ74 produced by Toshiba Electronic Devices & Storage Corporation) in our XOR
gate and the full adder. It should be noted that for miniaturization, the circuit consisting of MOSFET might be a good choice in industry since it can be scaled down.

**S2. Description of N-type NDR-enhanced magnetic transport**

In the main text, N-type NDR helped to form two magnetism-controlled voltage levels and offered a fundamental demonstration of the reliable output in logic operations. Due to the linear current-voltage relationship of the magnetic film, our three-terminal magnetic component can be regarded as a Δ-type resistor network, as shown in Figure S3.

This phenomenon can be qualitatively illustrated by the load line method\[27\] (Figure S4). With magnetization up, the resistance of the right side \(R_{\text{Right}}\) was larger than that of the left side \(R_{\text{Left}}\) and the slope of the load line of the right side \(I_{\text{Right}}\) was smaller than that of the left side \(I_{\text{Left}}\) (Figure S4b ~ f). When the applied voltage was small, both \(I_{\text{Right}}\) and \(I_{\text{Left}}\) intersected at the first positive resistance region, and the voltage difference of two sides was small (Stage 1). With increasing applied voltage, \(I_{\text{Right}}\) firstly intersects at the negative resistance region, and the voltage of the right side \(V_{\text{Right}}\) increases while the voltage of the left side \(V_{\text{Left}}\) decreases, leading to the appearance of voltage bifurcation (Stage 2). With further increase of applied voltage, \(V_{\text{Left}}\) increases from the first positive region (Stage 3) to a negative resistance region (Stage 4). When the applied voltage was large, both \(I_{\text{Right}}\) and \(I_{\text{Left}}\) intersected at the second positive resistance region (Stage 5). The voltage difference of the two sides became small and the voltage bifurcation disappears. With magnetization down, \(R_{\text{Right}} < R_{\text{Left}}\), and the right and left side are at a low voltage state and high voltage state in the voltage bifurcation region, respectively.

To explain the five stages mentioned above, we can deduce the \(I-V\) curve of the total device with the following equations, according to Kirchhoff’s law:

\[
V = V_{\text{Left}} + V_{\text{Right}} \tag{S1}
\]

\[
I_{\text{top}} = \frac{V_{\text{Left}}}{R_{\text{Left}}} + I_{\text{NDR}}(V_{\text{Left}}) = \frac{V_{\text{Right}}}{R_{\text{Right}}} + I_{\text{NDR}}(V_{\text{Right}}) \tag{S2}
\]

where \(V\), \(I_{\text{NDR}}\), and \(I_{\text{top}}\) represent the total applied voltage, the voltage on the N-type NDR components, and the current of the top channel in the Δ-type resistor network of the three-terminal magnetic component (Figure S3b). With magnetization up, \(R_{\text{Right}} < R_{\text{Left}}\). The solution of equations S1 and S2 can be illustrated by the load line method (Figure S5). With increasing current \(I_{\text{top}}\) of the top channel, the load line of the right side, with slope of \(1/R_{\text{Right}}\), crosses the \(I-V\) curve of the N-type NDR at point R, while the load line of left channel, with slope of \(1/R_{\text{Left}}\), crosses the \(I-V\) curve of the N-type NDR at point L. According to geometric relations, points L and R satisfy Equation S2. Accordingly, we can add \(V_{\text{Right}}\) and \(V_{\text{Left}}\) to get \(V\) at \(I_{\text{top}}\) (point P).
Using this method, we can draw the whole trace of the $I$-$V_o$ curve, as shown in Figure S5b. The first positive resistance region, negative resistance region and the second positive resistance region of the N-type NDR $I$-$V$ curve are labelled as the $\alpha$, $\beta$ and $\gamma$ branches, respectively (Figure S5b). The situation of the left side at $X$ ($X=\alpha$, $\beta$, $\gamma$) branch and right side at $Y$ ($Y=\alpha$, $\beta$, $\gamma$) branch are labelled as the $X$-$Y$ branches. As the N-type NDR components have nonlinear transport properties, our magnetic logic device has several solutions for a special applied voltage. With the applied voltage $V_{\text{applied}}$, there were three possible solutions of the right-left sides in the $\alpha$-$\beta$, $\beta$-$\alpha$ and $\beta$-$\beta$ branches (Figure S5b). With magnetization up, when $V < V_1$, the right and left sides were both at the $\alpha$ branch and the difference of voltage of two sides was small, corresponding to stage 1 in Figure S4b. When the applied voltage increased above $V_1$, because the difference of $R_{\text{right}}$ and $R_{\text{left}}$ opened a gap between the $\alpha$-$\alpha$ and $\alpha$-$\beta$-$\beta$ branches around the applied voltage $V_1$, the stations of the left and right sides evolve only from the $\alpha$-$\alpha$ to the $\beta$-$\alpha$ branch and cannot enter the $\alpha$-$\beta$ or $\beta$-$\beta$ branches. For the situation of the $\beta$-$\alpha$ branch, the right side was at the $\beta$ branch and the voltage of this side was high. At the same time the left side was at the $\alpha$ branch and the voltage of this side was low, leading to the appearance of voltage bifurcation with high $V_{\text{right}}$ and low $V_{\text{left}}$, which corresponds to stage 2. With the further increase of the applied voltage, the voltage of the right-left side enters the $\gamma$-$\alpha$ and $\gamma$-$\beta$ branches, corresponding to stage 3 and 4, respectively. For the $\gamma$-$\alpha$ and $\gamma$-$\beta$ branches, the right and left sides were at different branches and the difference of the voltage of the two sides was large. When $V > V_4$, the left and right sides were both at the $\gamma$ branch and the difference of the voltage of two sides became small, leading to the disappearance of voltage bifurcation, which corresponds to stage 5. Therefore, with the increase of applied voltage from zero, the right-left side can move in the branches of $\alpha$-$\alpha$, $\beta$-$\alpha$, $\gamma$-$\alpha$, $\beta$-$\gamma$ and cannot enter the branches of $\alpha$-$\beta$, $\alpha$-$\gamma$, $\beta$-$\beta$ and $\beta$-$\gamma$ due to the gap induced by the anomalous Hall effect.

An extremely large magnetism-controlled voltage bifurcation was observed in our magnetic device (Figure S4a), which could be used for reconfigurable logic operations. Three magnetic components (two as logic input bits (a, b) and one as the control bit (c)) were connected in parallel (Figure 1b in main text). Because of the anomalous Hall effect, the relationship of effective resistances for the left channel ($R_{\text{eff, left}}$) and right channel ($R_{\text{eff, right}}$) varied with the magnetization configuration of the three magnetic bits (Figure S6a). When $c = “0”$, $R_{\text{eff, left}} < R_{\text{eff, right}}$ only for logic inputs $(1, 1)$ and $R_{\text{eff, left}} > R_{\text{eff, right}}$ for all other logic inputs. When $c = “1”$, $R_{\text{eff, left}} < R_{\text{eff, right}}$ only for logic input $(0, 0)$ and $R_{\text{eff, left}} > R_{\text{eff, right}}$ for all other logic inputs. Hence, enlarged by the N-type NDR, left voltage $V_{O1}$ was at high voltage state (logic output “1”) only for logic input $(1,1)$ and at low voltage state (logic output “0”) for the other logic inputs, which is the logic operation of AND. At the same time, the right voltage $V_{O2}$ realized the logic operation of NAND. The left voltage $V_{O1}$ and right voltage $V_{O2}$ satisfied the logic operations of OR and NOR, respectively (Figure S6 b).

S3. Measurement of switching time of magnetic device and N type NDR
As the switching time of the logic operations in our magnetic logic device is determined by the switching time of the N-type NDR, we firstly measured the switching time of the N-type NDR with an electrical method\textsuperscript{[16]} (Figure S7). For the resonant tunneling diode, voltage pulses of 10 ns in width were applied, with voltage varied from 0.1 V to 0.4 V. The switching time was obtained from the input and output signals, and the power consumption was obtained from $IVt$, where $I$ is the current, $V$ is the voltage pulse amplitude, and $t$ is the switching time, as shown in Table S1 and Figure 1c in main text.

The measured switching time of the current-driven magnetic logic device was determined as ~10 ns\textsuperscript{[10]}, much larger than that of complementary metal-oxide-semiconductor (CMOS) logic circuits. However, for resonant tunneling diodes, the measured switching time can achieve values as low as ~300 ps, which is much shorter than that of CMOS logic and other magnetic logic devices with the same scale. Furthermore, compared with current-driven magnetic logic and magnetic domain-wall logic, the power consumption of our magnetic logic device was much lower because of the lower working currents in the logic operations.

For our magnetic logic device, the switching time in magnetic storage process is determined by the spin-orbit torque in the Ta/CoFeB/MgO multilayer. By measuring the transverse voltage of the three-terminal magnetic component before and after the triggering current pulse, the switching time of spin-orbit torque switching can also be measured using an electrical method\textsuperscript{[16]}, as shown in Figure S8b. Additionally, we used the magneto-optical Kerr effect (MOKE)\textsuperscript{[28]} to measure the switching time of the spin-orbit torque, as shown in Figure S8, where magnetic switching can also be observed after applying a current pulse with 1 ns width. Spin-orbit torque switching in our magnetic layer with voltage pulses down to ~1 ns has been observed, demonstrating that the switching time of spin-orbit torque in our devices was < 1ns.

**S4. Fabrication of an XOR gate and full adder by cascading**

The logic outputs of our device are voltage signals with large output ratios, which can trigger the MOSFET (RUM003N02 produced by Rohm Semiconductor) directly. Therefore, several magnetic logic gates can be cascaded via MOSFET and intermediate magnetic bits. As examples, we present an exclusive-OR (XOR) gate by cascading two NOR magnetic logic gates and two MOSFETs (Figure S9), and show also the capability for full adder operation by cascading four NOR magnetic logic gates with control circuits (Figure 3 in the main text). Here, we give a more detailed discussion of the XOR gate and the full adder. The N-type NDR used in the XOR gate and the full adder were components consisting of complementary junction field transistors.

The XOR logic operations can be expressed as follows:

$$a \text{ XOR } b = (a \text{ NOR } b) \text{ NOR } (\overline{a} \text{ NOR } \overline{b})$$

(S3)
where $\overline{a}$ and $\overline{b}$ represent NOT $a$ and NOT $b$. This was achieved by flowing write currents through bit $a$ (bit $b$) and bit $\overline{a}$ (bit $\overline{b}$) in opposite directions (indicated by green lines in Figure S9a).

For the magnetic logic gate A (Figure S9a) consisting of bit $a$, bit $b$, and the bit $c_1$, the gate voltage $V_{OI}$ satisfied the NOR operation between bit $a$ and bit $b$, realizing “$a$ NOR $b$” in equation S3. For the magnetic logic gate B (Figure S9a) consisting of bit $\overline{a}$, bit $\overline{b}$, and bit $c_1$, the gate voltage $V_{OII}$ satisfied the NOR operation between bit $\overline{a}$ and bit $\overline{b}$, realizing “$\overline{a}$ NOR $\overline{b}$” in equation S3. For the two parallel connected MOSFETs, the output current $I_O$ was low only when both the gate voltage $V_{OI}$ and $V_{OII}$ were low, and it was high for all other situations (Figure S10). The output magnetic bit $d$ was preset as logic “1” (magnetization up), and it was switched to logic “0” via spin-orbit torque for high output currents and remained logic “1” for low output currents. The magnetization of output bit $d$ satisfies the NOR operation between gate voltage $V_{OI}$ and $V_{OII}$, thereby realizing “($a$ NOT $b$) NOR ($\overline{a}$ NOT $\overline{b}$)” in equation S3. Therefore, the XOR operation of bit $a$ and bit $b$ was realized.

The Sum operation of the full adder can be expressed as follows:

$$S_i = \text{SUM} (A_i, B_i, C_{i-1}) = (A_i \text{ XOR } B_i) \text{ XOR } C_{i-1} \quad (S4)$$

Based on the XOR gate, the Sum operation of the full adder can be achieved by our device in two steps via intermediate bits $I_i$ and $\tilde{I}_i$ (Figure S11). In the first step, the XOR operation of bit $A_i$ and bit $B_i$ is performed by the XOR gate (Figure S11) and the results written into intermediate bits $I_i$ and $\tilde{I}_i$. In the second step, the XOR operation of bit $I_i$ and bit $C_{i-1}$ is performed and the result written into bit $S_i$, realizing the Sum operation ($A_i \text{ XOR } B_i) \text{ XOR } C_{i-1}$ in equation S4). Moreover, control circuits with a sequence pulse generator (Figure S12), were also applied, so that the first and the second steps could be processed automatically.

In the first step, the voltage pulse $Q_1$ was triggered, the blue MOSFETs were “on” and the yellow MOSFETs were “off” (Figure 4 in the main text). Hence, the magnetic bits and N-type NDR were connected (Figure S11a). The XOR operation of $A_i$ and $B_i$ was performed and the results were written into intermediate bits $I_i$ and $\tilde{I}_i$, realizing $I_i = A_i \text{ XOR } B_i$. In the second step, the voltage pulse $Q_2$ was triggered after $Q_1$, and the blue MOSFETs were “off” and the yellow MOSFETs were “on” (Figure 3 in the main text). Hence, the XOR operation of $I_i$ and $C_{i-1}$ was performed, and the result was written into bit $S_i$ (Figure S11b), realizing $S_i = I_i \text{ XOR } C_{i-1} = (A_i \text{ XOR } B_i) \text{ XOR } C_{i-1}$. The Sum operation of the full adder was therefore realized.

S5. Industrial implementation potential of the logic-memory device
In the main text, the industrial implementation potential of our device was briefly illuminated from the aspects of miniaturization capability and cascade. Here, we give a more detailed discussion about miniaturization capability, switching time, power consumption, and reproducibility, as well as some perspectives on cascading.

S5.1. Miniaturization capability, switching time and power consumption

Firstly, the N-type NDR components used in our experiment were resonant tunneling diodes and circuits consisting of complementary junction-gate field-effect transistors. For resonant tunneling diodes, the switching time is related to the semiconducting materials used (e.g., ~55 ps for GaN/AlN, and ~21 ps for InGaAs/AlAs\(^{22}\)) and switching times can achieve ~1.7 ps. Hence, by using resonant tunneling diodes, our magnetic logic device can work at extremely high frequencies (~THz)\(^{29}\). Circuits consisting of complementary MOSFETs could also be used, and are compatible with current semiconductor technology and can be scaled down. The switching time of MOSFET can decrease dramatically when scaled down (30 ps for fin field-effect transistor of 32 nm in size\(^{18}\)). Therefore, the working frequency of our device could achieve ~GHz if circuits consisting of MOSFETs are used, which is good enough for conventional logic application.

Secondly, the magnetic components can be scaled down to ~20 nm with a stable perpendicular magnetic anisotropy property\(^{20}\). Because magnetic logic output bits can be switched by an all-electric method via spin-orbit torque, the writing process is determined by the switching time of the spin-orbit torque in magnetic components, which can achieve < 180 ps\(^{19}\). If the Ta/CoFeB/MgO multilayers used in our experiment are replaced by Pt/Ta/Cu/Co/Pt/Ta magnetic multilayers, the switching time of spin-orbit torque can be as low as ~6 ps\(^{30}\).

Finally, we estimated the potential power consumption per logic operation of our logic-memory device. Considering the magnetic components are of ~20 nm in size, the working current must be smaller than switching current, which is estimated at ~2 μA. The working voltage can be estimated to be ~0.4 V according to the working voltage of the resonant tunneling diode. Hence, one logic operation will consume an energy of < 0.08 fJ with duration time of ~100 ps for our logic-memory device, which is much lower than that for spin-transfer torque magnetic tunnel junction logic (~50 fJ for 20 nm in size\(^{31}\)) and that for spin-orbit torque magnetic tunnel junction logic (49.6 fJ for 40 nm in size\(^{9}\)). If a resonant tunneling diode with lower working voltage is adopted, the power consumption can be further reduced. Furthermore, our logic-memory device can perform non-volatile logic operations and information storage in one step, which saves the energy consumed by standby power, as well as data refreshing, transferring and transformation in conventional processors. These are the major superiorities of our logic-memory device in power consumption compared with conventional CMOS logic.

S5.2. Reproducibility

In the magnetic logic gate (Figure 1b in the main text), we continuously switched three magnetic bits of two logic input bits and one control bit in the sequence of (111)
and repeated application of this sequence 1000 times, with the output voltage was measured. Part of the results are shown in Figure S13a. We also performed a magnetism-controlled reconfigurable logic operation $8 \times 10^3$ times reliably for testing of the device’s reproducibility. The endurance of our device in logic operation is determined by the endurance of the N-type NDR used. The measured endurance of the resonant tunneling diode$^{32}$ and MOSFET circuits$^{33}$ were $>10^9$ and $10^{16}$. The endurance of the memory parts is determined by the spin-orbit torque switching$^{34}$, which was measured to be $> 10^{14}$.

The measurement of logic operation reproducibility (Figure S13b) indicates that the probability distribution of the logic output “1” (High voltage state) and the logic output “0” (Low voltage state) satisfies a normal distribution:

$$f_{HVS}(V) = \frac{1}{\sqrt{2\pi} \times 4.4287 \times 10^{-5}} \exp\left\{ -\frac{(V - 0.38095)}{2(4.4287 \times 10^{-5})^2} \right\}$$  \hspace{1cm} (S5)$$

$$f_{LVS}(V) = \frac{1}{\sqrt{2\pi} \times 4.0809 \times 10^{-5}} \exp\left\{ -\frac{(V - 0.03891)}{2(4.0809 \times 10^{-5})^2} \right\}$$  \hspace{1cm} (S6)$$

In our magnetic logic-memory device, the output voltage is converted to writing current $I_O$ by a MOSFET (Figure S14a). The output voltage and the writing current satisfy:

$$I_O = f_{mosfet}(V_O) = I_{DS} \left( \frac{V_O}{V_{GS(th)}} - 1 \right)^2$$  \hspace{1cm} (S7)$$

where $V_{GS(th)}$ represents the threshold gate voltage of the MOSFET, and $I_{DS}$ represents the writing current when $V_O = 2V_{GS(th)}$.

As the magnetization of output bit $d$ is switched by the writing current $I_O$ via the SOT effect, the switching possibility is related to the current density through the magnetic device, which can be expressed as follows$^{35}$ (Figure S14b):

$$P_{switch} = 1 - \exp\left\{ 1 - \frac{r_p}{r_0} \exp\left\{ -\Delta \left( 1 - \frac{J}{J_c} \right) \right\} \right\}$$  \hspace{1cm} (S8)$$

where $r_p$ is the width of the applied pulse, $r_0$ is the switching speed (1 ns in our experiment), $\Delta$ the is thermal stability (58.3 for our magnetic films), $J$ is the applied writing current density, and $J_c$ is the critical current density ($10^6$ A/cm$^2$ in our experiment). From equations S5, S6, S7, and S8, the logic operation error rate of our magnetic logic-memory device can be calculated as $10^{-7}$, which is comparable with that of CMOS logic$^{13}$.

Furthermore, we can enhance the anomalous Hall effect-induced voltage imbalance of the three-terminal magnetic components by choosing magnetic materials with large anomalous Hall angles, such as magnetic semiconductors ($\rho_{xy}/\rho_{xx} \sim 0.15$)$^{36}$ and magnetic topological insulators ($\rho_{xy}/\rho_{xx} \sim 100$)$^{37}$), both of which are much larger than that of the magnetic material used in our experiment ($\rho_{xy}/\rho_{xx} \sim 0.02$).
By use of a material with a larger anomalous Hall effect, the device-to-device reproducibility will be improved and will satisfy the requirement of large-scale industrial implementation. Therefore, our logic-memory device with these perspectives has a good potential for device-to-device reproducibility.

S5.3. Perspective of cascading

As our logic-memory device can perform reconfigurable logic and non-volatile memory simultaneously, we designed a magnetic logic-memory architecture that is simpler than CMOS logic, as shown in Figure S15.

There are two main layers in this architecture: the semiconductor layer and the magnetic layer. The semiconductor layer contains an array of N-type NDR components, MOSFETs, and the control unit circuit, while the magnetic layer contains an array of magnetic components. It is not necessary to place two N-type NDR components around every magnetic bit. Instead, the control unit circuit is fabricated with standard CMOS technology, and can address magnetic bits, select N-type NDR pairs and connect them with magnetic bits. Hence, the number of N-type NDR pairs is determined by the requirement of parallel computing logic operations and is much smaller than the number of magnetic bits. The working process of this architecture is: (1) the control unit selects target N-type NDR pairs and magnetic bits, and magnetic output bits are pre-set, (2) magnetic input bits, output bits and N-type NDR pairs are connected via MOSFET to form a magnetic logic gate, (3) the logic operation is performed and the results are written into the magnetic output bits in one clock cycle.

In complex logic operations, such as the XOR gate and the full adder, both N-type NDR components and magnetic bits can be “shared” with this architecture. For example, the magnetic bits used in the first step can also be used in the second step under the control of the control unit, which will further reduce the chip area. Moreover, without a requirement for data transfer and transformation between logic processors and memory, a large number of logic-memory processes can be executed in parallel, enhancing the computational efficiency significantly. Meanwhile, both input data and output data are stored in magnetic bits at run time of the logic operation, resulting in “instant-on” performance after resumption from being powered off.
Fig. S1 a) Schematic of the anomalous Hall effect of magnetization down (left) and up (right). b) AHE-induced voltage imbalance of a MgO/CoFeB/Ta multilayer film at an applied voltage of 1 V. The inset is the measurement circuit.
**Fig. S2** N-type NDR $I$-$V$ curves of (a) a resonant tunneling diode and (b) circuits consisting of two complementary junction-gate field-effect transistors. The differential resistance was $\sim 170$ $\Omega$ in the negative resistance region of RTD, and 800 $\Omega$ in the circuits consisting of junction-gate field-effect transistors.
Fig. S3 a) Schematic of our magnetic device structure. b) The equivalent Δ-type resistor network of the three-terminal magnetic component.
Fig. S4 Mechanism of NDR-induced current bifurcation. a) The phenomenon of voltage bifurcation for the case of magnetization up. The applied voltage can be divided into five stages. For stages 1 to 5, the changing trend of the right side are increase, increase, increase, decrease, and increase, while that of the left side are increase, decrease, increase, increase, and increase. b) ~ f) The situations of load lines on the $I$ - $V$ curves at different stages. The red and blue dashed lines show the load line of the right and left sides for magnetization up, respectively. The red and blue arrows indicate the variation trend of the voltage of the right and left sides with increasing applied voltage.
Fig. S5 a) Schematic of the load line method with N-type NDR components. b) Traces of the $I_{top}$-$V$ curve for magnetization up (labels $\alpha, \beta, \gamma$ are referenced in the text of S2).
Fig. S6  a) Voltage imbalance directly induced by the anomalous Hall effect with different magnetization configurations of the three magnetic bits. b) Output voltages $V_{O1}$ and $V_{O2}$ of different magnetization configurations of the three magnetic bits with an applied voltage of 0.4 V.
Fig. S7 (a) Electrical set-up for the time-resolved measurements of the voltage-dominated NDR. The capacitors $C_1$, $C_2$, and inductance $L$ are used to eliminate direct voltage in the circuit. (b) The input and output signals of the NDR.
Fig. S8 (a) Optical detection of the three-terminal magnetic logic device under nanosecond electrical pulses. (b) The transverse voltage of three-terminal magnetic component before and after applying a current pulse with 1 ns width. Repeated experiments were performed to eliminate thermal and electrical noise.
Fig. S9 Schematic of an XOR magnetic logic gate based on our device. The green lines represent the write line of the logic input bits. Since the write currents through bit $a$ and bit $\bar{a}$, bit $b$ and bit $\bar{b}$ are opposite, the magnetization of bit $a$ and bit $\bar{a}$, bit $b$ and bit $\bar{b}$ are reversed, driven by spin-orbit torque. b) Current through the output bit $d$ with various logic inputs. c) Truth table for the magnetic logic XOR device.
Fig. S10 a) Two MOSFETs in parallel connected with output bit $d$. b) The relationship between the magnetization of output bit $d$ and the gate voltages $V_{OI}$ and $V_{OII}$ of the MOSFETs.
Fig. S11 a) The equivalent circuit of the first step of the operation of a full adder. b) The equivalent circuit of the second step of the operation of a full adder.
Fig. 12 a) Schematic of a sequence pulse generator (SPG). b) The voltage pulses generated by the SPG, where voltage pulse $Q_2$ is generated after voltage pulse $Q_1$. 
Fig. S13  a) Measurement of logic operation reproducibility, and b) probability distribution of output logic “0” (Low voltage state, left) and output logic “1” (High voltage state, right).
**Fig. 14** a) Schematic showing magnetic switching controlled by output voltage via a MOSFET. b) Switching probability as a function of applied current.
Fig. 15 Schematic of logic-memory architecture based on our logic-memory device. The magnetic layer of magnetic bit arrays is fabricated on the semiconductor layer, and the magnetic layer can contain several layers of magnetic bit arrays. Conducting metal wires can be filled between the semiconductor layer and the magnetic layer. The dashed lines indicate how three magnetic input bits, one magnetic output bit and N-type NDR pairs construct one magnetic logic gate. The inset in the red dashed box shows the basic unit of our logic-memory device.
Table S1. The measured switching time, power, and power consumption of a resonant tunneling diode.

<table>
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<tr>
<th>Input voltage (V)</th>
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<th>0.2</th>
<th>0.3</th>
<th>0.4</th>
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<td>Switching time (ns)</td>
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<td>0.439</td>
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<td>0.298</td>
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<td>Power consumption (pJ)</td>
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<td>0.161</td>
<td>0.117</td>
<td>0.152</td>
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</table>
References


