High-Yield Ti$_3$C$_2$Tx MXene-MoS$_2$ Integrated Circuits

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Abstract: It is very challenging to employ solution-processed conducting films in large-area ultrathin nanoelectronics. In this manuscript, spray-coated Ti$_3$C$_2$Tx MXene films as metal contacts are successfully integrated into sub-10 nm gate oxide two-dimensional (2D) MoS$_2$ transistor circuits. The Ti$_3$C$_2$Tx films are prepared on glass substrates by a spray coating process followed by vacuum annealing. Compared to the as-prepared sample, the films after a vacuum annealing exhibit a higher conductivity (~11,000 S/cm) and a lower work function (~4.5 eV). Besides, the annealed Ti$_3$C$_2$Tx film can be patterned through a standard cleanroom process without peeling-off. The annealed Ti$_3$C$_2$Tx film shows a better band alignment for n-type transport in MoS$_2$ channel with small work function mismatch of 0.06 eV. The MoS$_2$ film can be uniformly transferred on the patterned Ti$_3$C$_2$Tx surface and then readily processed through the cleanroom process. A large-area array of Ti$_3$C$_2$Tx MXene-MoS$_2$ transistors is fabricated using different dielectric thicknesses and semiconducting channel sizes. We demonstrate high yield and stable performance for these transistor arrays even with an 8 nm thick dielectric layer. Besides, several circuits are demonstrated, including rectifiers, NMOS inverters, and voltage-shift NMOS inverters. Overall, this work indicates the tremendous potential for solution-processed Ti$_3$C$_2$Tx MXene films in large-area 2D nanoelectronics.
1. Introduction

MXenes, atomic-thin early transitional metal carbides or nitrides, are a fast-growing family of 2D materials with attractive physical and chemical properties.\(^1\)-\(^4\) They have a general formula \(\text{M}_n\text{X}_n\text{T}_x\), where M represents a transitional metal element, X represents carbon or nitrogen element, and T represents surface groups including -F, -OH, -O.\(^5\)-\(^7\) They are derived from their precursor MAX phase (A represents Al, Ga, or Si), usually through chemical etching A element using hydrofluoric acid solution,\(^6,8\) mixture of fluoride salts and hydrochloric acid,\(^9,10\) alkali solution\(^11\) or molten salt.\(^12,13\) They hold the unique combination of several excellent properties, such as metallic conductivity,\(^14\) surface plasmons,\(^15\) hydrophilicity,\(^16\) tunable surface groups and work function (theoretically in between 2 and 8 eV),\(^12,17\)-\(^20\) and good water dispersibility without surfactant.\(^7,21,22\) These are enabling MXenes many promising applications in energy storage,\(^23\)-\(^26\) catalyst,\(^27\)-\(^29\) electromagnetic shielding,\(^30\)-\(^32\) strain sensing,\(^33\)-\(^35\) bio-sensing,\(^36,37\) (photo) thermoelectric,\(^18,38,39\) optoelectronics\(^15,40\)-\(^42\) and electronics.\(^19,20,43\)-\(^45\) Especially in the electronic applications, the representative \(\text{Ti}_3\text{C}_2\text{T}_x\) MXene is raising great interests and playing impact-growing roles as contact electrodes in transistors because of its excellent conductivity up to 24,000 S/cm,\(^46\) good chemical and mechanical stability\(^47\)-\(^50\) and low-cost surfactant-free solution process.\(^4,21\)

So far, \(\text{Ti}_3\text{C}_2\text{T}_x\) film has been used as transistor contact electrodes with semiconducting oxide,\(^43\) organic semiconductors,\(^20,51\) and quantum dots,\(^44\) which have demonstrated its potential in microelectronics. However, there have been no attempts to integrate large-area \(\text{Ti}_3\text{C}_2\text{T}_x\) metal electrodes with wafer-scale 2D semiconducting films. Besides, there have been no previous reports using sub-10 nm high-k gate oxide for solution processing of thin film transistors. The reason is that the too rough surface, particle residues, non-layered stacking defects in the solution-processed conducting films would cause serious leakage issues in the device operation. These are typical concerns for most of the solution-processed conductive films as the transistor contact electrode, including silver nanowire,\(^52\)-\(^54\) carbon nanotube,\(^55,56\) and graphene.\(^57\) Thus, almost all the solution-
processed transistor fabrication techniques utilize a very thick dielectric layer to avoid the current leakage issue, as listed in Table S1. Nevertheless, this manuscript found that the Ti$_3$C$_2$Tx film prepared by our homemade automatic spray system showed excellent reliability in large-area Ti$_3$C$_2$Tx-MoS$_2$ transistor arrays. When using high-k dielectric bilayer HfO$_2$/Al$_2$O$_3$ (short name: Hf/Al) with thickness above 10 nm (such as Hf/Al: 16 nm and 27 nm), we evidenced ~96% yield with narrow device performance variation. Even though we reduced the Hf/Al layer thickness to less than 10 nm (~8 nm), we could still achieve about 80%-yield in transistor devices with leakage current less than few nanoamps. Besides, we investigated devices with different dimensions (channel length and width), and we could consistently achieve high-yield transistor arrays. We also fabricated and characterized different circuits such as rectifiers, NMOS inverters, and voltage-shift NMOS inverters to confirm the device reliability further. Therefore, we conclude that the solution-processed Ti$_3$C$_2$Tx MXene film has a great potential in large-area ultrathin nanoelectronics.

2. Results and Discussions

2.1. Device fabrication process
Figure 1. The schematic of Ti$_3$C$_2$Tx MXene-MoS$_2$ device array fabrication process. a) Spray-coated Ti$_3$C$_2$Tx film on glass. b) The lattice model of hexagonal Ti$_3$C$_2$Tx structure with vdW gaps. c) The 2-inch bilayer MoS$_2$/c-cut sapphire wafer grown by epitaxial phase conversion process. d) The lattice model of the 2H-MoS$_2$ structure with vdW gaps. e) The MoS$_2$ film transferred on the lithography-processed Ti$_3$C$_2$Tx pattern surface. f) The Ti$_3$C$_2$Tx-MoS$_2$ transistor arrays fabrication schematic through the standard cleanroom photolithography process. Micro-optical graphs of g) the Ti$_3$C$_2$Tx film patterning as source/drain (S/D) electrodes, h) the transferred MoS$_2$ film patterning as the semiconducting channel, i) the ALD HfO$_2$ film as the dielectric layer (400 cycles), j) the spray-coated Ti$_3$C$_2$Tx film and k) corresponding patterning as the top gate (TG) electrode. (Scale bar: c - 0.5 inch; e - 1 cm; g - 350 µm; h, i, j, k - 500 µm)

Figure 1 provides the process flow used to fabricate the Ti$_3$C$_2$Tx-MoS$_2$ transistor array. Before starting the cleanroom fabrication process, the metallic Ti$_3$C$_2$Tx and semiconducting MoS$_2$ films were individually prepared. The Ti$_3$C$_2$Tx films were coated on a glass substrate (Figure 1a) by our homemade automatic spray system, as shown in Video S1. To achieve reliable electronic-grade Ti$_3$C$_2$Tx films, Ti$_3$C$_2$Tx flake water suspension and the spray coating process need to be carefully...
optimized. Before starting the spray coating, a UV-ozone treatment is also essential to make the glass surface hydrophilic.\textsuperscript{[21]} However, the as-sprayed Ti$_3$C$_2$Tx film cannot directly go through the cleanroom patterning process because liquid chemicals involved in the lithography have a high chance to destroy the film by re-dispersing the as-stacked flakes. Therefore, we performed a vacuum annealing process at 400 °C for 1 h to enhance the flake stack adhesion on the glass substrate.\textsuperscript{[58]} Three semitransparent Ti$_3$C$_2$Tx MXene films with different thickness are displayed in Figure 1a. The 2D layered structure of Ti$_3$C$_2$Tx is reflected by the lattice model in Figure 1b. One vdW layer has seven layers of covalently bonded atoms. Two layers of carbon atoms (brown spheres) are in-between three titanium layers (blue spheres); the two outside layers (red spheres) are chemically bonded surface groups (including -F, -OH, =O). In addition, the 2-inch MoS$_2$ film (Figure 1c) was grown on a c-cut sapphire substrate by the epitaxial phase conversion process developed in our lab.\textsuperscript{[59, 63]} The high-quality, large-area uniformity and continuity have been well confirmed in our previous reports.\textsuperscript{[59, 63]} The MoS$_2$ 2H phase with vdW layered structure is displayed in Figure 1d. The MoS$_2$ film was transferred on the patterned Ti$_3$C$_2$Tx with few wrinkles (see Figure 1e) through a wet transfer process. The cleanroom device fabrication process is shown in Figure 1f. The annealed Ti$_3$C$_2$Tx film went through a photolithography patterning process followed by a dry etching process to generate the Ti$_3$C$_2$Tx source/drain (S/D) electrode array. The clean and uniformly patterned Ti$_3$C$_2$Tx array is shown in Figure 1g, where no peeling off phenomena occurred during the patterning process. Then, we transferred the large-area MoS$_2$ film uniformly on top of this S/D array patterning. A photolithography patterning and dry etching process was used to form the MoS$_2$ channels, which were well-aligned to the Ti$_3$C$_2$Tx S/D electrode array, as indicated in Figure 1h. Subsequently, the dielectric layer HfO$_2$ (or Al$_2$O$_3$) was grown by an atomic layer deposition (ALD) system. Dielectric layers including HfO$_2$ with 400 or 200 cycles and HfO$_2$/Al$_2$O$_3$ bilayer with 180/20, 100/20, or 50/10 cycles were deposited. The photograph in Figure 1i shows the device array after depositing 400-cycle HfO$_2$, with a noticeable color change compared to Figure 1h. After that, dielectric via holes were opened to access the S/D contact pads using photolithography combined with a dry etching process. The top
gate Ti$_3$C$_2$T$_x$ layer coating and patterning was processed in the same way as the S/D Ti$_3$C$_2$T$_x$ layer. The uniform Ti$_3$C$_2$T$_x$ film coating and clean patterning can be confirmed in Figures 1j and 1k, respectively. Before testing, the fabricated devices were annealed at 200 °C for 1 h in H$_2$ atmosphere for improving contact among adjacent layers.

2.2. Film characterization

**Figure 2.** Characterizations of Ti$_3$C$_2$T$_x$ and MoS$_2$ films. a) AFM height images (Scale bar: 1 µm) b) Raman c) XRD and d) electrical conductivity vs. temperature curves of both fresh-sprayed Ti$_3$C$_2$T$_x$ film (fresh-Ti$_3$C$_2$) and 400 °C vacuum-annealed Ti$_3$C$_2$T$_x$ film (400-Ti$_3$C$_2$). Ti 2p XPS spectra of e) fresh-Ti$_3$C$_2$ and f) 400-Ti$_3$C$_2$ films. C 1s XPS spectra of g) fresh-Ti$_3$C$_2$ and h) 400-Ti$_3$C$_2$ films. i) Optical image, j) AFM image (with line scan across the edge), and k) Raman spectrum of the large-area MoS$_2$ film. (Scale bar: i - 250 µm; j - 4 µm). l) UPS spectra of fresh-Ti$_3$C$_2$, 400-Ti$_3$C$_2$, and MoS$_2$ films.

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Basic characterization of Ti$_3$C$_2$T$_x$ and MoS$_2$ films is shown in Figure 2. Using atomic force microscopy (AFM), we confirmed that both the 400 °C vacuum-annealed (upper image) and as-prepared (lower image) Ti$_3$C$_2$T$_x$ film are formed by excellent lateral stacking of 2D flakes as shown in Figure 2a. The structure, conductivity, and surface chemistry of both fresh Ti$_3$C$_2$T$_x$ (fresh-Ti$_3$C$_2$, black curves) and 400 °C vacuum-annealed Ti$_3$C$_2$T$_x$ (400-Ti$_3$C$_2$, red curves) films are discussed in Figure 2b-h. Raman spectra of both fresh-Ti$_3$C$_2$ and 400-Ti$_3$C$_2$ in Figure 2b display characteristic peaks at 127, 207, 383, 577, 717, and 723 cm$^{-1}$, consistent with previous reports. No peak position shift is observed after annealing at 400 °C. However, one small bulge at 163 cm$^{-1}$ is observed in fresh-Ti$_3$C$_2$, probably because of a small amount of oxidization induced by the Raman laser irradiation in air. In contrast, the bulge at 163 cm$^{-1}$ is not observed in the 400-Ti$_3$C$_2$ Raman spectrum, implying its better stability. In the X-ray diffraction (XRD) spectra in Figure 2c, both fresh-Ti$_3$C$_2$ and 400-Ti$_3$C$_2$ have only (0002) family of diffraction peaks observed, further confirming their near-perfect layer stacking. However, we noticed an obvious peak shift between the fresh-Ti$_3$C$_2$ and 400-Ti$_3$C$_2$, especially the 0002 peak shifts from 6.1° (in black) to 7.9° (in red). We used the Bragg’s Law and calculated the lattice parameter in c-LP to be 28.2 Å for fresh-Ti$_3$C$_2$ and 22.4 Å for 400-Ti$_3$C$_2$. The shrinking interlayer spacing results from the removal of water molecules intercalated in-between Ti$_3$C$_2$T$_x$ layers after thermal treatment. We also compared their electrical conductivity in Figure 2d. Their metallic nature is confirmed as the electrical conductivity of both samples decreases with increasing temperature. However, the 400-Ti$_3$C$_2$ sample shows a higher conductivity value (about 11,000 S/cm at 32 °C) than the fresh-Ti$_3$C$_2$ sample (about 6,300 S/cm at 32 °C). The elimination of water molecules after vacuum annealing results in closer inter-flake stacking and thus lower contact resistance. Conductive AFM characterization (Figure S1a-d) further fact confirmed the 400-Ti$_3$C$_2$ has higher conductivity, more negative surface charge, and stronger surface adhesion force. Those improved properties after MXene annealing in a vacuum helped to achieve better contact between Ti$_3$C$_2$T$_x$ MXene and MoS$_2$ during patterning, as shown in Figure S1e. Moreover, the 400-Ti$_3$C$_2$ film was found
to be more stable during the standard cleanroom patterning process than the fresh-Ti$_3$C$_2$, as shown in Figure S2 and Video S2-3. X-ray photoelectron spectroscopy (XPS) characterization was performed to figure out the change in the Ti$_3$C$_2$T$_x$ surface state after vacuum annealing at 400 °C. Detailed XPS spectra of the Ti 2p and C 1s for both fresh-Ti$_3$C$_2$ and 400-Ti$_3$C$_2$ samples are shown in Figure 2e-f and g-h, respectively. Lorentzian-Gaussian fitting on all relevant XPS spectra was performed. We can figure out that some sub-peaks related to special chemical bonding show an obvious drop after annealing, such as C-O and O-C=O in C 1s. This result means that surface contaminations were effectively removed or modified after the vacuum-assisted thermal treatment. However, other sub-peaks related to Ti-C and Ti-(O or F) bounding have no observable change, which means both the flake crystal quality and the surface groups change very little after this vacuum annealing. Corresponding F 1s and O 1s XPS spectra are shown in Figure S3.

We also characterized the large-area few-layer MoS$_2$ film used as the channel layer in the transistor. This MoS$_2$ film was grown by the epitaxial phase conversion method developed previously by our group.$^{[59,63]}$ The optical image of the MoS$_2$ film transferred on the SiO$_2$ (300 nm)/Si$^{++}$ substrate is displayed in Figure 2l, confirming its considerable area uniformity and continuity. The AFM image inserted with a line-scale profile is shown in Figure 2j, confirming the layer thickness of about 1.69 nm (2 ~ 3 layers). The Raman spectrum of the MoS$_2$ film in Figure 2k shows peak difference of about 23 cm$^{-1}$ between $E_{2g}$ and $A_{1g}$ modes. We also compared the work function difference among MoS$_2$, fresh-Ti$_3$C$_2$, and 400-Ti$_3$C$_2$ by ultraviolet photoelectron spectroscopy (UPS) as shown in Figure 2l. It shows 400-Ti$_3$C$_2$ has a lower work function value of ~4.50 eV compared to the fresh Ti$_3$C$_2$ (~4.60 eV). The reduced work function value was further confirmed by Kelvin probe force microscope (KPFM) measurement (see Figure S4). Since MoS$_2$ has a work function value of ~4.44 eV (see the blue curve in Figure 2l) and a conduction band minimum (CBM) reported about 4.25 eV,$^{[64]}$ it means 400-Ti$_3$C$_2$ has less contact barrier to MoS$_2$ than the fresh-Ti$_3$C$_2$. This has been further indicated in the band offset diagram in Figure S4c-d. Therefore, we confirmed that the Ti$_3$C$_2$T$_x$ film after 400 °C vacuum
annealing shows better compatibility as a metal contact in the MoS$_2$ transistor in terms of conductivity, contact barrier, and device fabrication durability.

### 2.3. Transistor performance using different dielectric layers

**Figure 3.** Ti$_3$C$_2$T$_x$-MoS$_2$ transistors performance with different dielectric layer thickness ($t_{\text{Diel}}$) and interface, all transistors have fixed channel width/length ($W/L=250/25$ $\mu$m/$\mu$m) to facilitate the comparison. Dual scan of transfer curves in logarithmic & linear scale, and leakage current of transistors with dielectric layers of a) Hf200 b) Hf180/Al20 c) Hf50/Al10, fixing $V_{DS}$ at 0.1V. d-f) Their corresponding output curves, respectively, range of $V_{GS}$ change is indicated in the relevant plots. Transistor performance changes under different dielectric layers: g) $I_{ON}/I_{OFF}$ ratio and $I_{GS}$, h) forward threshold voltage ($V_{thF}$) and hysteresis ($\Delta V_{th}$), and i) field-effect mobility ($\mu_{FE}$) and subthreshold swing ($SS$). j) Yield counted by randomly testing many devices at different locations. ($t_{\text{Hf400}}$: 55 nm; $t_{\text{Hf200}}$: 27.5 nm; $t_{\text{Hf180/Al20}}$: 24.8/2.4 nm; $t_{\text{Hf100/Al20}}$: 13.7/2.4 nm; $t_{\text{Hf50/Al10}}$: 6.8/1.2 nm. The Al$_2$O$_3$ layer was deposited on the MoS$_2$ layer before the HfO$_2$ deposition to improve the semiconductor/dielectric interface.)

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As demonstrated above, the Ti$_3$C$_2$Tx film exhibits excellent electrical conductivity, low band offset with MoS$_2$, and good compatibility with the cleanroom patterning process. Therefore, we were motivated to make transistor devices using Ti$_3$C$_2$Tx as contact electrodes (including S/D and TG) and MoS$_2$ as the semiconducting channel layer. Different dielectric layers were used, including 55 nm HfO$_2$, 27.5 nm HfO$_2$, 24.8/2.4 nm HfO$_2$/Al$_2$O$_3$, 13.7/2.4 nm HfO$_2$/Al$_2$O$_3$, and 6.8/1.2 nm HfO$_2$/Al$_2$O$_3$ layers all grown by ALD using 400 (Hf400), 200 (Hf200), 180/20 (Hf180/Al20), 100/20 (Hf100/Al20), and 50/10 (Hf50/Al10) deposition cycles, respectively. We compared three representative transistor transfer curves in logarithmic and linear scale and the corresponding leakage current in logarithmic scale in Figure 3a-c. Using Hf200 as the dielectric layer in Figure 3a, we confirmed that Ti$_3$C$_2$Tx-MoS$_2$ transistors could work appropriately with the S/D current on/off ratio ($I_{on}/I_{off}$) of about 10$^5$, the gate to source leakage current ($I_{gs}$) less than 10$^{-10}$ A. Its corresponding output curves are shown in Figure 3d. The dual sweep transfer curves in both the logarithmic and linear scale show a relatively large hysteresis, which might result from the charge traps at the MoS$_2$/HfO$_2$ interface.$^{[65]}$ Using the Hf180/Al20 dielectric layer, the typical transistor with the MoS$_2$/Al$_2$O$_3$ interface formed has a similar dielectric layer thickness to the transistor with the MoS$_2$/HfO$_2$ interface. Its transfer and leakage current curves (Figure 3b) display similar $I_{on}/I_{off}$, $I_{gs}$ levels, $V_{gs}$ operation range (-3 to 6 V), while offering lower hysteresis. The output curves of the transistor using the Hf180/Al20 dielectric layer are shown in Figure 3e. We further tried the thinner dielectric Hf50/Al10 layer of about 8 nm, which has been rarely reported for transistor devices using solution-processed electrodes. Amazingly, the Ti$_3$C$_2$Tx-MoS$_2$ transistor achieving a similar $I_{on}/I_{off}$ still exhibits a low leakage current of 10$^{-10}$ A, as shown in Figure 3c. The reason for this substantially reduced gate leakage could be that the thinner dielectric layer causes the larger capacitance so it can regulate the $I_{ds}$ with a smaller $V_{gs}$ range (-1 to 2 V). The smaller voltage operation range is also reflected in its output curve in Figure 3f. Notably, almost all kinds of solution-processed conducting films have very rough surfaces, prohibiting their applications in ultrathin nanoelectronics. They need a thick dielectric layer to fabricate transistor...
devices to avoid current leakage, as listed in Table S1. The successful demonstration here using the sub-10 nm dielectric layer opens a window for solution-processed ultrathin nanoelectronics.

Next, we tested many devices with the same transistor W/L size using all five dielectric layers. Their logarithmic-scale transfer and $I_{GS}$ leakage curves are shown in Figure S5, and representative output curves are provided in Figure S6. The statistical analysis plots of transistor performance parameters are illustrated in Figure 3g-j. We first confirmed that all the transistors have very low gate leakage, as shown in the Figure 3g orange curve. Even though the dielectric layer thickness is reduced from 55 nm (Hf400) to 8 nm (Hf50Al10), the leakage current is always below $10^{-9}$ A. Furthermore, most $I_{ON}/I_{OFF}$ ratios are above $10^5$, as seen in the Figure 3g black curve. Notably, when the dielectric layer is ~16 nm (Hf100/Al20), the $I_{ON}/I_{OFF}$ ratio could reach $10^8$. In Figure 3h, we can see that both forward threshold voltage ($V_{thF}$, black curve) and hysteresis ($\Delta V_{th}$, orange curve) become smaller when the dielectric layer thickness is reduced. In addition, the MoS$_2$/dielectric interface has a minor influence on the $V_{thF}$, but noticeable change is observed in hysteresis ($\Delta V_{th}$) when comparing the dielectrics Hf200 and Hf180/Al20. The dielectric layer thickness also heavily influenced the subthreshold swing (SS) value, where the thinnest dielectric layer (8 nm of Hf50/Al10) resulted in SS of only 224 mV·dec$^{-1}$. Further, negligible changes of SS values were observed when changing the transistor from MoS$_2$/HfO$_2$ to MoS$_2$/Al$_2$O$_3$, but this interface change improved the field-effect mobility ($\mu_{FE}$). However, the dielectric layer thickness has little influence on the mobility value. Figure 3j illustrates that 100% transistor can be achieved when using thicker dielectric layers of 27.2 nm (Hf180/Al20) and 16.1 nm (Hf100/Al20). Further, 80% yield was achieved even with a sub-10 nm thin dielectric layer (Hf50/Al10).

2.4. Characterization on the sub-10 nm gate oxide transistor
Figure 4. Characterization on the layer stacking structure of a Ti₃C₂Tₓ-MoS₂ transistor with sub-10 nm Hf50/Al10 dielectric layer. a) The optical image of the transistor with W/L = 250/25 µm/µm, the blue-marked area is for the cross-sectional TEM sample preparation. b) The three-dimensional device schematic, all layers are labeled. Cross-sectional STEM images c) in low magnification and d) in high resolution from the orange-marked area in Figure c. (Scale bar: c - 20 nm, d - 5 nm) e) Intensity profile from the orange-line scan in Figure d. f) The optical image (upper) and cross-sectional schematic (bottom) of Ti₃C₂Tₓ/(Hf50/Al10)/Ti₃C₂Tₓ metal/insulator/metal (MIM) capacitor (diameter: 200 µm). g) Curves of capacitance density vs. bias under different frequencies.

We further characterized the transistors that use the Hf50/Al10 gate dielectric layer and MXene contacts (Figure 4). The optical image of one typical transistor with the size of W/L=250/25 µm/µm is shown in Figure 4a. The blue-marked area is selected for the cross-sectional TEM sample preparation using the focused ion beam (FIB) technique. The TG transistor structure is schematically displayed in Figure 4b, where Ti₃C₂Tₓ MXene is used as both bottom S/D contact and TG electrodes and MoS₂ as the semiconducting channel stacked on the top of S/D electrodes. The blue-rectangle marked area in Figure 4b shows the cross-section of the stacking structure, which was visualized using transmission electron microscopy (TEM). The low magnification TEM image in Figure 4c displays the layered nature of Ti₃C₂Tₓ at the top and bottom dark area and the Hf50/Al10 layer at the bright area in the middle. We found that the ALD Hf50/Al10 layer could uniformly cover all the
device area even though the bottom S/D Ti$_3$C$_2$Tx layers have a considerable thickness fluctuation between 12.1 nm and 45.1 nm (see the TEM image and relevant intensity line scan plots in Figure S7). The high-resolution TEM image in Figure 4d could resolve the bilayer MoS$_2$ channel legibly. The intensity line scan in Figure 4e, plotted along the orange vertical dashed line in Figure 4d, indicates relevant vdW layer gaps and dielectric layer thickness. The vdW gap in-between Ti$_3$C$_2$Tx layers is about 11.03 Å, which is consistent with the XRD result. The vdW gap in the MoS$_2$ layer is about 7.1 Å, similar to previous reports.\[^{[63]}\] The vdW gap between Ti$_3$C$_2$Tx and MoS$_2$ is relatively large, about 19.3 Å, which might increase contact resistance. Also, the dielectric layer (Hf$_{50}$/Al$_{10}$) was confirmed to have a thickness of about 8 nm. A Ti$_3$C$_2$Tx/Dielectric layer/Ti$_3$C$_2$Tx (metal/insulator/metal or MIM) capacitor was fabricated to test the capacitance under different voltages and frequencies. Figure 4f displays a representative MIM capacitor with an overlap area diameter of 200 µm; an optical image of the device is shown in the upper part and the MIM capacitor schematic is in the lower part of the figure. Capacitance density vs. voltage curves measured at different AC field frequencies are shown in Figure 3g for a Ti$_3$C$_2$Tx/Hf$_{50}$/Al$_{10}$/Ti$_3$C$_2$Tx MIM capacitor. We can observe that the capacitance value of about $1.15 \times 10^{-6}$ F·cm$^{-2}$ for this Ti$_3$C$_2$Tx/Hf$_{50}$/Al$_{10}$/Ti$_3$C$_2$Tx MIM capacitor, which hardly changes with frequency. Capacitors using other dielectric layers were also fabricated and tested as illustrated in Figure S8 and Table S2. It is observed that using the same dielectric layer (Hf$_{400}$), the capacitance value is slightly lower than values for capacitors using Au/Ti or AZO oxide as contacts,\[^{[63, 69]}\] but capacitance stability with frequency is comparable.

2.5. Transistor performance with different channel sizes
Figure 5. MXene-MoS₂ transistors performance with different channel $W/L$ using dielectric layer Hf100/Al20. a) The photograph of a 1-inch glass wafer with transistor arrays. b) The microscopic optical image of a transistor array with different channel dimensions. c) The yield and d) Dual sweep logarithmic-scale transfer curves collected by randomly testing many devices at different locations. Statistical analysis data in Figure 5d for transistor parameters e) $I_{GSmax}$ f) $\Delta V_{th}$ g) $\mu_{FE}$ h) $I_{ON}/I_{OFF}$ and i) $SS$, both forward and reverse scans have been considered. In Figure g-i: the data in blue corresponding to forward scan curves, the data in red corresponding to reverse scan curves. (Scale bar: b - 250 µm)

We fabricated transistor arrays with different $W/L$ on the 1-inch glass substrate to further explore the device reliability and area uniformity. The device was fabricated using the dielectric layer Hf100/Al20, and its image is shown in Figure 5a. The microscopic optical image of the transistor array is provided in Figure 5b, which shows devices with different channel sizes. We tested many devices from the randomly selected area across the glass wafer and found a very high yield of workable transistors with a very low leakage current level. The yield of transistors with different $W/L$ is shown in Figure 5c. Remarkably, their yields in any channel size are higher than 90%, and the total...
yield counting 123 devices with different sizes could reach even 96%. Figure 5d shows plots of logarithmic-scale $I_{DS}$ transfer and $I_{OS}$ curves of many devices, obtained from six channel $W/L$ sizes, as marked in the figure. These curves show the excellent area uniformity of the devices. Corresponding output curves of representative transistors are shown in Figure S9. Quantitative analysis parameters of these transistors further confirmed the performance reliability and uniformity. Figure 5e indicates that most devices with the maximum gate leakage current level are below $10^{-10}$ A for any $W/L$ size. Figure 5f demonstrates that all devices exhibit voltage hysteresis in between 0.2 to 0.9 V. Particularly, devices with $W/L$ of 100/25 $\mu$m/$\mu$m have hysteresis in a very narrow range (0.68 ~ 0.88 V). In Figure 5g, field-effect mobility (blue) calculated from forward sweep transfer curves changes between 1 and 3 $\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$, while the reverse-sweep mobility (red) fluctuates between 1 and 6 $\text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$. The reason for the higher mobility in reverse-sweep curves might result from the interface charge trapping in the semiconductor/dielectric interface.\(^{[66]}\) The highest mobility was obtained from the device with $W/L$ 100/50 $\mu$m/$\mu$m. In addition, $I_{ON}/I_{OFF}$ ratios of most devices varied in the range of $10^6$ to $10^8$ (blue) for forward sweep and $10^5$ to $10^6$ (red) for the reverse sweep, as seen in Figure 5h. The $SS$ values change between 200 and 600 mV-dec$^{-1}$ for dual-sweep, as shown in Figure 5i. Therefore, we confirmed that both the solution-processed $\text{Ti}_3\text{C}_2\text{T}_x$ MXene film and the large-area MoS$_2$ film developed in our group are suitable for fabricating high-yield and highly reliable transistor arrays over 1-inch wafers.

### 2.6. Circuits performance
Figure 6. Ti$_3$C$_2$T$_x$-MoS$_2$ circuits performance. a) The optical image of the transistor rectifier and its b) circuit diagram, c) DC rectification operation, d) AC input signal with different amplitude and frequency, and e) half-wave output DC signals under different AC frequency (Curves with the same color in d and e means the same frequency). f) The optical image of the NMOS inverter and its g) circuit diagram, h) output voltage transfer curve, i) gain values, and j) Peak gain values under different supply voltages. k) The optical image of the voltage-shift NMOS inverter and its l) circuit diagram, m) output voltage transfer curve, and n) gain values with fixed $V_{in}$ at 4 V but under different $V_{shift}$. (Scale bar in a, f, k - 200 μm)

Given the well-demonstrated large-area uniformity and reliability of Ti$_3$C$_2$T$_x$ MXene-MoS$_2$ transistor arrays, we were motivated to fabricate more complicated circuits to show its potential for large-area electronics integration. In Figure 6, we discuss three different kinds of circuits: the TFT rectifier (TFTR) integrated with a single transistor, the negative-channel metal oxide semiconductor (NMOS) inverter integrated with two transistors, and the voltage-shift NMOS (V-NMOS) inverter integrated with four transistors. The TFTR relevant test results are illustrated in Figure 6a-e. The TFTR optical image is displayed in Figure 6a; it was designed by short connecting the transistor gate and drain electrodes. The gate-drain terminal could act as the anode and the source terminal act as the...
cathode. Therefore, the TFTR could perform as a traditional diode and could convert AC into DC signal.\[67\] The circuits diagram for TFTR function as AC to DC converter is displayed in Figure 6b. We first confirmed its DC voltage operation performance with the $I-V$ curve illustrated in Figure 6c. The forward current could reach $1.1 \times 10^{-5}$ A at a voltage of 2 V. The rectification ratio is about $0.56 \times 10^{2}$ in between $\pm 2$ V. The AC performance is discussed in Figure 6d-e. AC input sine voltage signals with different frequencies and peak voltages are shown in Figure 6d. Its corresponding output DC half-wave signals can be seen in Figure 6e. We confirmed that the TFTR rectification function performs properly when the AC frequency is less than 20 Hz. The NMOS inverter test results are shown in Figure 6f-j. The optical image of the NMOS inverter is shown in Figure 6f. We designed the inverter with depletion load where the gate is short-connected to the source in the load TFT. The load transistor has an aspect ratio of 5 ($W/L = 250/50 \, \mu m/\mu m$), and the driver transistor with an aspect ratio of 20 ($W/L = 500/25 \, \mu m/\mu m$), resulting in the load ratio (beta ratio) value of 4. Its circuit diagram design is illustrated in Figure 6g. The static voltage transfer characteristics (VTC) are shown in Figure 6h. The sweep range of the input voltage ($V_{in}$) is between $-2$ and 2 V. The sweeping operation was done under different supply voltages ($V_{DD}$) from 1 to 5 V with 1 V per step. We calculated the gain value from the VTC curve negative slope ($-\frac{\partial V_{out}}{\partial V_{in}}$),\[68, 69\] Gain vs. $V_{in}$ curves in Figure 6i show clear sharp peaks near $V_{in} = 0$ V under all $V_{DD}$ voltage sweeps. The peak gain values are plotted in Figure 6j. The quasi-linear increase in the peak gain value with $V_{DD}$ could be observed when $V_{DD}$ is smaller than 4 V. The V-NMOS circuit is another circuit we fabricated; it is more complicated since four transistors are needed. The optical image and corresponding circuit diagram are displayed in Figures 6k and 6g, respectively. Two transistors on the left side are integrated as an NMOS inverter with depletion mode, which is the same structure as shown in Figure 6f. Another two series-connected TFT on the right side are fabricated by short-connecting the gate and drain. The load TFT' gate-drain terminal performs as the $V_{in}$ terminal for the whole V-NMOS inverter, while the driver TFT' source terminal performs as the $V_{shift}$ terminal. The gate electrode in the left NMOS
inverter is connected to the middle point in between load TFT' and driver TFT'. We fixed the \( V_{in} \) at 4 V, and varied the input \( V_{shift} \) from 0 to -1 V during the operation. VTC curves in Figure 6m displayed the left-shift phenomena of the switching voltage when applying \( V_{shift} \) with more negative values. The switching left shift could be quantitatively analyzed from the Gain vs. \( V_{in} \) curves in Figure 6n. The gain peak positions are left-shifted from -0.1 to -0.45 V when the \( V_{shift} \) changes from 0.1 V to -1 V, also the gain values are changed from 10.1 to 6.8. The advantage of V-NMOS is to achieve different VTC profiles without changing the load ratio. Therefore, we demonstrated three kinds of integrated circuits using several MXene-MoS\(_2\) transistors.

3. Conclusion

In summary, we prepared highly conductive Ti\(_3\)C\(_2\)T\(_x\) MXene films by spray coating followed by vacuum annealing process. The conductivity could reach 11,000 S/cm after 400 °C annealing in vacuum for 1 h. We also demonstrated that the vacuum-annealed Ti\(_3\)C\(_2\)T\(_x\) could be reliably patterned through standard cleanroom photolithography and dry etching process. The vacuum-annealed Ti\(_3\)C\(_2\)T\(_x\) has a smaller work function value of 4.5 eV compared to the freshly spray-coated sample (4.6 eV), and thus smaller contact energy barrier with semiconducting MoS\(_2\) channel. The well-prepared Ti\(_3\)C\(_2\)T\(_x\) MXene pattern was further employed as source/drain and gate contact electrodes for a large-area MoS\(_2\) top-gated transistor array. The results show that the transistor array can achieve a high yield of ~96% with very narrow device performance variation when the ALD grown dielectric layer thickness is more than 10 nm. Even if the dielectric layer is reduced to only 8 nm, an 80% yield still can be achieved. The use of such thin gate dielectric layers has rarely been explored for the solution processing of electronic devices. Besides, we also statistically investigated the influences of both dielectric layer thickness and MoS\(_2\)/dielectric interface on the transistor performance. Transistor performance stability and area uniformity was also confirmed by testing devices with different channel sizes over a 1-inch glass wafer. Finally, we also fabricated several circuits to confirm Ti\(_3\)C\(_2\)T\(_x\)-
MoS$_2$ transistor integration feasibility. Even though the average Ti$_3$C$_2$T$_x$-MoS$_2$ transistor performance is somewhat lower than well-developed vacuum-deposited Au/Ti$^{[70, 71]}$ or CVD grown graphene contact,$^{[72]}$ the initial achievement here implies great space to improve. Above all, we demonstrated solution-processed MXene films great potential application in large-area ultrathin 2D nanoelectronics.

4. Experimental Section/Methods

*Synthesis of the Ti$_3$C$_2$T$_x$ MXene*: Ti$_3$AlC$_2$ MAX phase ($\geq$400 mesh) was purchased from Lanzhou Kai Kai Ceramic Materials Co., Ltd, China. Ti$_3$C$_2$T$_x$ MXene was synthesized according to the literature.$^{[44]}$ In a typical process, 1 g Ti$_3$AlC$_2$ MAX was immersed slowly over ~3 min into a mixture of 1 ml of HF (49%), 6 ml of HCl (12 M), and 3 ml of DI water under gentle stirring to avoid overheating from the exothermic nature of the reaction. The mixture was then stirred at 400 RPM at 42 $^\circ$C to etch away Al$^{3+}$ from Ti$_3$AlC$_2$ MAX. After 15 h, the mixture was taken out and washed with DI water, centrifuged at 2600 RPM for 2 min. The centrifugation process was repeated several times until the pH value is 6, where about 250 ml DI water was used. Next, the sediment was mixed with the aqueous LiCl solution (0.75 M), and the mixture was stirred at 500 RPM for 20 min at room temperature. Subsequently, two additional centrifuge cycles were necessary to discard the supernatant and collect the sediment, where about 90 ml DI water was used. During the washing process, shaking was necessary to re-disperse solution before centrifugation. Finally, a delaminated Ti$_3$C$_2$T$_x$ MXene supernatant was obtained by centrifugation using Thermo Scientific™ Sorvall™ Legend™ XT Centrifuge at 500 RCFPM for 10 mins.

*Growth and transfer processes of the MoS$_2$ film*: The quasi-single-crystalline MoS$_2$ film grown on the sapphire substrate was prepared according to an epitaxial phase conversion method previously developed by our group.$^{[57, 61]}$ In this process, epitaxial MoO$_2$ film was firstly deposited on a 2-inch
(001) Al₂O₃ substrate at 400 °C by a pulsed laser deposition process. Then the MoO₂ film was placed on the right zone of the tube furnace for conversion using sulfur powder, which was put in the left zone. Ar gas was utilized to purge the tube furnace thoroughly before starting the conversion process. During conversion, the Ar gas flow, the pressure inside tube, the left zone temperature and the right zone temperature were fixed at 100 sccm, 5-10 torr, 150 °C and 900 °C, respectively. To transfer MoS₂ film, the as-grown MoS₂ film was firstly coated with Poly(methyl methacrylate) (PMMA) layer by a spin coating process and annealed at 180 °C for 1 min to enhance the PMMA adhesion and breaking strength. After that, the sample needs to be immersed in the buffered oxide etchant (BOE) solution until the PMMA/MoS₂ layer can be readily peeled off from the sapphire substrate. Then the PMMA/MoS₂ freestanding film was washed three times in DI water and then transfer onto the device substrate surface. The device with the PMMA/MoS₂ film was annealed in a vacuum oven at 90 °C for 2 h to remove the interface residue water in between the MoS₂ film and the device. In the end, the PMMA was removed by boiled acetone and isopropyl alcohol (IPA).

**Preparation of oxide films:** Tetrakis(dimethylamido)hafnium (IV), trimethylaluminum and deionized water were employed as the sources of Hf, Al, and O for the deposition of HfO₂ (~0.14 nm/cycles) and Al₂O₃ (~0.12 nm/cycles) films in a Cambridge Nanotech ALD system. The deposition temperature of HfO₂ and Al₂O₃ is 160 °C. During the ALD deposition process, pulse/purge times (in second) for Hf, O₃HfO₂, Al, and O₃Al₂O₃ sources used are 0.20/15, 0.015/10, 0.015/10, and 0.02/8, respectively.

**Transistor and circuits fabrication:** In order to obtain the Ti₃C₂Tx MXene film, an aqueous Ti₃C₂Tx MXene suspension with a concentration of 1.0–1.5 mg/mL was spray-coated on the 1-inch clean glass substrates pre-treated via UV-ozone for 10 min. The distance between the airbrush and glass substrate was about 23 cm, and more details could be obtained from Video S1. Then, the film was annealed at 400 °C in a vacuum of ~10⁻¹ Torr for 1 h. Subsequently, Ti₃C₂Tx MXene film was patterned through a conventional photolithography process. The AZ1512HS photoresist (PR) (Microchemicals)
was spin-coated on the substrate at 3000 RPM for 30 s and then baked at 100 °C for 60 s. The sample with PR was aligned and photopatterned in the mask aligner equipment (EVG6200∞). The UV light for photo exposing was fix at 41 mJ·cm⁻². After the UV exposure, the sample was immersed and developed in the AZ 726 MIF developer (Microchemicals) for 20 s. Then a plasma dry etching process was performed to remove the PR uncovered area of the Ti₃C₂Tx film. Finally, the remaining photoresist was removed by acetone combining with an ultrasonication. After the Ti₃C₂Tx source/drain electrode array patterning, MoS₂ film was transferred on the surface of Ti₃C₂Tx MXene electrodes and patterned via the same photolithography and dry etching process. Oxides dielectric layers with different thicknesses and components were grown in ALD. ALD cycles of Al₂O₃/HfO₂ were 10/50, 20/100, 20/180, 0/200, and 0/400 have been tried. The via hole array in the dielectric layer was also patterned through the same cleanroom process. Another Ti₃C₂Tx MXene film was spray-coated on top of the dielectric layer. Finally, another photolithography combining with a dry etching process was applied to pattern the film as the top-gate electrode array.

Materials and Device Characterization: The thickness and surface morphologies of the Ti₃C₂Tx MXene film and MoS₂ film were visualized by the Atomic force microscopy (AFM) (Bruker, Dimension Icon SPM). X-ray diffraction (XRD) patterns of the Ti₃C₂Tx MXene films were collected using a Bruker D8 Advance XRD system with Cu Kα radiation (λ = 1.5406 Å). The Raman spectra were characterized by Wintec Apyron Raman spectrometer equipment with a 633 nm laser source excitation. The surface conductivity, adhesion of MXene films before and after vacuum annealing were characterized in AFM (Bruker, Dimension Icon SPM) with a conductive tip under zero voltage bias. Surface potentials were collected using the Kelvin probe force microscope (KPFM) tapping mode. X-ray photoelectron spectra (XPS) studies were carried out in a Kratos Axis Supra DLD spectrometer equipped with a monochromatic Al Kα x-ray source (hv=1486.6 eV). It was operating at 150 W with a multichannel plate and delay line detector under a vacuum of 1×10⁻⁹ mbar. The survey and high-resolution spectra were collected at 160 eV and 20 eV fixing analyzer pass energies, respectively. They were quantified.
using empirically derived relative sensitivity factors provided by Kratos analytical. Samples were mounted in a floating mode to avoid differential charging. Charge neutralization was required for all samples. Ultraviolet photoelectron spectra (UPS) spectra were obtained using a He-I excitation (21.22 eV) source at pass energy 10 eV. The samples were mounted in contact mode for UPS measurements. The transmission electron microscopy (TEM) sample was fabricated by a focused ion beam (FIB) technique (Helios G4, FEI). The TEM image was obtained using a Titan G2 60-300 (FEI), equipped with a spherical aberration corrector for an imaging system, at an acceleration voltage of 300 kV. The morphology of transistors was observed through an optical microscope (Zeiss AXIO Scope). The electrical characterization of Ti$_3$C$_2$Tx, MXene film before and after the annealing process was collected using a commercially available thermoelectric tester RZ2001i (Ozawa Science Co. Ltd., Japan). A capacitance meter (Agilent E4981A) was employed to collect the capacitance-voltage curves for different oxide dielectric layers. The performances of transistors, transistors-based rectifiers, and transistors-based NMOS inverters were measured at room temperature in the dark by an Agilent B1500A semiconductor device analyzer equipped with a microprobe station (Summit-11600 AP, Cascade Microtech).

Supporting Information

Supporting information is available from the Wiley Online Library or from the author.

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We successfully fabricated large-area transistor circuits using solution-processed $\text{Ti}_3\text{C}_2\text{T}_x$ MXene as source/drain and gate contact electrodes, wafer-scale MoS$_2$ film as channel, and ultrathin HfO$_2$/Al$_2$O$_3$ layer of about 8 nm as the dielectric layer. The high yield and performance uniformity of the device array indicate great potential of the $\text{Ti}_3\text{C}_2\text{T}_x$ MXene in large-area ultrathin 2D electronics.


High-Yield $\text{Ti}_3\text{C}_2\text{T}_x$, MXene-MoS$_2$ Integrated Circuits