Low-Noise High-Precision Readout Circuits for Capacitive MEMS Accelerometer

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ABSTRACT

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Over the past two decades, Micro-Electro-Mechanical System (MEMS) based accelerometers, benefiting from relatively simple structure, low-power consumption, high sensitivity, and easy integration, have been widely used in many industrial and consumer electronics applications. For the high precision accelerometers, a significant technical challenge is to design a low-noise readout circuit to guarantee the required high resolution of the entire integrated system.

There are three main approaches for improvement of the noise and offset of the readout circuit, namely auto-zero (AZ) and correlated double sampling (CDS) for the switched-capacitor (SC) circuit and chopper stabilization (CHS) for the continuous-time circuit.

This thesis investigates the merits and drawbacks of all three techniques for reading the capacitance of a low noise MEMS accelerometer developed in our group. After that, we compare the different effects of the three technologies on noise, offset, output range, linearity, dynamic range, and gain. Next, we present the design of the most suitable structure for our sensor to achieve low noise, low offset, and high precision within the working frequency. In this thesis, the design and post-layout simulation of the circuit is proposed, and the fabrication is currently in progress. The readout circuit has reached the noise floor of the sub-\( \mu \)g, which meets the strict requirements of low noise MEMS.
capacitance-to-voltage converter. A high-performance accelerometer system is regarded as the core of a low-noise, high-resolution geophone. We show that together with the MEMS accelerometer sensor, the readout circuit provides competitive overall system noise and guarantees the required resolution.
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LIST OF ABBREVIATIONS

AC      Alternating Current
ADC     Analog-to-Digital Converter
AZ      Auto-Zero
AZTMD   Auto-Zero Time-Multiplexed Differential
CDC     Capacitance-to-Digital Converter
CDS     Correlated Double Sampling
CHS     Chopper Stabilization
CMFB    Common-Mode Feedback
CMOS    Complementary Metal-Oxide-Semiconductor
CMRR    Common Mode Rejection Ratio
CT      Continuous-Time
CTC     Continuous-Time Current
CTV     Continuous-Time Voltage
CVC     Capacitance-to-Voltage Converter
DAC     Digital-to-Analog Converter
DC      Direct Current
ENEA    Electronic Noise Equivalent Acceleration
IoT     Internet of Things
LPF     Low Pass Filter
MEMS    Micro-Electro-Mechanical System
MNEA    Mechanical Noise Equivalent Acceleration
NMOS    N-type Metal–Oxide–Semiconductor Field-Effect Transistor
OOC-CVC Offset-Canceled Cascaded Capacitance-to-Voltage Converter
OTA     Operational Transconductance Amplifier
PM      Phase Margin
PMOS    P-type Metal–Oxide–Semiconductor Field-Effect Transistor
PSD     Power Spectral Density
PSRR    Power-Supply Rejection Ratio
QNEA    Quantization Noise Equivalent Acceleration
RC      Random Chopper
SC      Switched-Capacitor
SNR     Signal-Noise Ratio
TMD     Time-Multiplexed Differential
TNEA    Total Noise Equivalent Acceleration
VGA     Variable Gain Amplifier
LIST OF SYMBOLS

\( \phi \)  
clock signal

\( k \)  
effective spring constant

\( b \)  
damping factor

\( \pi \)  
a mathematical constant whose value is the ratio of any circle’s circumference to its diameter

\( d \)  
the gap distance between comb fingers

\( A \)  
sensor comb fingers overlap area

\( \varepsilon_0 \)  
permittivity of vacuum

\( \varepsilon_r \)  
the relative permittivity of air

\( D \)  
Damping coefficient

\( m \)  
Mass

\( R \)  
Resistance

\( L \)  
Inductance

\( C \)  
Capacitance

\( k \)  
Boltzmann constant

\( T \)  
absolute temperature

\( f \)  
Frequency

\( \gamma \)  
channel length parameter

\( g_m \)  
transconductance of transistor

\( C_{ox} \)  
Gate oxide capacitance per unit area

\( W \)  
width of the transistor

\( L \)  
length of the transistor

\( f_c \)  
corner frequency

\( \bar{f}_c \)  
chopping frequency

\( R_D \)  
the resistance between drain and source of transistor

\( C_S \)  
sensing capacitor

\( C_F \)  
feedback capacitor

\( R^2 \)  
coefficient of determination

\( V_{OS} \)  
offset voltage
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Chapter 1  Introduction

1.1 Motivation

With the development of artificial intelligence technology, the interaction between humans, machines, and the world has become more frequent, and the Internet of Things is gradually becoming a reality. Humans sense the surrounding world through the sensory system. Similarly, computers need to sense the world through sensors. There is no doubt that the accuracy of sensor input directly determines the computer’s processing capacity.

The accelerometer is a widely used sensor. Acceleration is an essential input data in the navigation system. In other fields, such as oil exploration, seismic surveys, and automobile airbags, the accelerometer also plays an important role. The application of accelerometers on handheld devices makes it profoundly affects our lives.

In nowadays integrated circuits, the power supply voltage is becoming lower to improve integration and reduce energy consumption. The offset and low-frequency noise of the amplifier causes dynamic range reduction and precision degradation. With lower supply voltage, this problem becomes more and more critical. Designing a low-noise, high-precision readout circuit for the accelerometer has become challenging work.

1.2 Overview of MEMS Accelerometers and Readout Circuit

The micromachined inertial accelerometer is one of the most critical devices in today’s life. It is widely used in many industries such as biomedical, automotive, consumer electronics, robotics, and military [1, 2].
The earliest high-resolution accelerometers were applied to spacecraft for an exploration mission. Until the 1970s, these accelerometers were still macroscopic devices with large size, heavyweight, and high cost [3].

With the development of semiconductor fabrication technology, accelerometers based on micromachining techniques were created. They have light weight, small size, low cost, and low power consumption. What is more, the integration of micromachined devices and circuits became possible. Vaganov invented the first Micro-Electro-Mechanical System (MEMS) accelerometer in 1975 [4]. In 1979, a piezoresistive MEMS accelerometer, which had a few mg resolutions, was developed by Roylance and Angell [5]. This accelerometer had a bandwidth larger than 1 kHz. In the 1990s, the popularity of family cars drove the development of the airbags industry. The core sensor of the airbag system was an accelerometer. When the car is applied a sharp acceleration due to collision, the airbag ejects. This application requires the accelerometer to have a small size, low price, and high robustness.

In the new century, especially in the 2010s, mobile devices’ universal, especially smartphones, opened up broad prospects for accelerometers. Nowadays, every smartphone contains multiple sensors. One of them is the three-axis MEMS accelerometer [6].

MEMS technology and the corresponding readout circuit technology have undergone a rapid update in recent years. However, the basic working principle of the MEMS accelerometer is similar. The sensor could be regarded as a first-order approximation of a spring-mass-damp system. The equivalent structure is shown in Figure 1.1. It consists of
a suspended proof mass $m$ in a compliant suspension system and an effective spring constant $k$. $b$ is the damping factor that stands for the accelerometer’s dynamic damping characteristic. These parameters have the relationship:

$$Q = \sqrt{\frac{km}{b}}$$  \hspace{1cm} (1.1) \hspace{1cm} \text{(1.1)}$$

Figure 1.1 Schematic diagrams of a capacitive accelerometer structure and its mechanical lumped parameter model. [3]

The micromachined accelerometer’s transfer function of the motion is expressed as:

$$H(s) = \frac{x(s)}{a(s)} = \left( s^2 + \frac{bs}{m} + \frac{k}{m} \right)^{-1} = \left( s^2 + \frac{\omega_0}{Q} + \omega_0^2 \right)^{-1}$$  \hspace{1cm} (1.2) \hspace{1cm} \text{(1.2)}$$

A MEMS accelerometer could transfer the acceleration to some readable signal. The direct transfer is from the acceleration to proof mass’s placement or mechanical stress on the suspension system. Then, the variation is transferred to capacitive, piezoresistive, piezoelectric, thermal, optical, electromagnetic, tunneling effect, and so on [3]. Capacitive transduction is the most common method used in nowadays productions.
The resolution of a MEMS accelerometer is determined by the total noise equivalent acceleration (TENA). It consists of several components and will be illustrated in chapter 2.

There are several methods that could lower the noise of mechanical parts, which are:

(1) Lower spring constant
(2) Larger proof mass
(3) Higher quality factor
(4) Lower noise interface circuit
(5) Sensing schemes with a higher scale factor

Our primary target is to design a low-noise high-precision readout circuit, so we will mainly focus on the fourth method.

Christian and Gabor wrote a paper about reducing the amplifier’s imperfections in 1996 [7]. At that time, the three main strategies: Auto-Zero (AZ), Correlated Double Sampling (CDS), and Chopper Stabilization (CHS), had been proposed and applied to many practical designs. In this paper, they also introduced some practical implementation issues and did noise analysis. Note that AZ and CDS are discrete methods, while CHS is a continuous method. AZ and CDS can not modulate offset to a higher frequency but have the gain-enhancing ability. CHS is suitable for designs with ultra-low baseband noise.

There are two main kinds of micromachining accelerometers. Bulk micromachined accelerometers [8-10] have lower mechanical and thermal noise and higher sensitivity.
Surface micromachined accelerometers [11-13] have lower manufacturing costs and better integration. Regarding the parasitic capacitance, bulk micromachining is higher because of the out-of-plane schematic.

A Monolithic CMOS MEMS accelerometer was proposed for ultra-small capacitance changes [13]. This research showed that continuous-time voltage (CTV) sensing had the best noise performance than switched-capacitor (SC) and continuous-time current (CTC) methods. A chopper-stabilized method was applied to this design. In that case, the noise floor was a function of both operating frequency and input transistor’s size. So there is an optimum transistor size of best noise performance. The match equation is:

\[ C_{gs} + C_{ga} = \eta (2C_s + C_p) \]  \hspace{1cm} (1.3)

Where \( C_s \) is the sensing capacitor and \( C_p \) is the parasitic capacitance. \( \eta \) is a parameter that refers to channel length and operation region. The relationship between transistor’s size and the noise floor is shown in Figure 1.2
Figure 1.2 noise floor vs. NMOS transistor channel width at 10 MHz with a channel length of 0.5 μm [13].

The CHS method was also used in some other small sensing elements [14]. If the parasitic capacitance is substantial and much larger than the transistor’s capacitances, the capacitance matching could be ignored.

For designs with sizeable parasitic capacitance (such as bulk micromachined sensors), the structure in [13] was sensitive to the parasitic capacitances, so that caused resolution degeneration. Simultaneously, the clock feedthrough and charge injection effect create considerable spikes, amplifying and appearing at output [15]. A large time constant, residual offset, and chopper ripple also appear. In this case, Auto-Zero (AZ) and Correlated-Double-Sampling (CDS) become better methods. Their structures are simpler, fit fast capacitance charging and discharging. The sensing method offers a virtual ground for the input, so it is not sensitive to the parasitic capacitance.

Regarding the structure of the readout circuit, single-ended and differential are also significant categories. The differential structure is an excellent strategy for discrete circuit
design. Because it could cancel DC offset, 1/f noise, and switch errors and get better signal-noise ratio (SNR) and power-supply rejection ratio (PSRR) [16]. However, the most common problem of the differential structure is the input common-mode voltage drift. To solve this problem, the common-mode feedback (CMFB) structure is always applied. Another solution is to use two half-bridge structures and then follow one differential amplifier to build a fully differential signal. However, more complex systems cause more area and power consumption. What’s worse is that more switches lead to more switch sampling noise.

The single-ended AZ structure [17] could avoid these cons. However, the nonideal components (DC offset, 1/f noise, switch error) become dominant. To address this issue, an offset-canceled cascaded capacitance-to-voltage converter (OCC-CVC) was proposed [18] and shown in Figure 1.3.

The reset clock $\phi_1$ turns off earlier than $\phi_2$, which cause the nonideal components of the first stage sampled on $C_4$. However, although the second amplifier significantly reduces the sampling error, there is no much improvement in power consumption.
An Auto-Zero Time-Multiplexed Differential Capacitance-to-Voltage Converter (AZTMD-CVC) [10] was proposed to combine the advantages of the differential structure and also keep it relatively simple. It will be introduced in detail in the design chapter. The differential structure is much easier for the CDS. It is also widely used on the CHS technique as the chopper operation creates differential signals.

In recent years, some other methods combining with CHS were proposed. Expect the capacitance matching, random chopper (RC) architecture [19] was another technique. It randomizes low-frequency 1/f noise to be thermal-noise-like. The Dual-Chopper technique was used in [20, 21] to achieve low power and low noise. But the bandwidth is narrow, and it cannot achieve an ultra-low noise floor. Some other researchers used mixed techniques to combine the advantages of different methods. CHS and CDS were integrated in [22] to suppress low-frequency noise and compensate for DC offset. A combination of Dual-chopper amplifier and CDS was proposed [23] to alleviate 1/f noise and DC offset. However, these two design still kept the total noise equivalent acceleration larger than $10\mu g/\sqrt{Hz}$. Another research [24] also combined CDS and CHS to eliminate the effect of parasitic capacitance. While this design is for tiny sensing capacitor and high g input.

An ultra-low noise CVC [25] was realized by improving the operational amplifier. Its equivalent acceleration noise is only $200ng/\sqrt{Hz}$, and the high-precision and high-bandwidth characteristics are achieved simultaneously. For the price, this design used a vast input pair transistor ($29236\mu m/0.36\mu m$) and consumed 300mW power, which was more than ten times of other designs.
All the designs introduced above are about the capacitance-to-voltage converter (CVC). There is another method that digitizes measurement signals directly [26-29]. Sigma-delta is the most common method used in these designs. However, these circuits usually have higher power consumption (dozens of times of CVCs). The extra electrical and quantization noise of ADC is also added to the analog frontend’s noise. These noises reduce the resolution and dynamic range of the readout circuit.

1.3 Thesis Objectives

As we introduced above, several methods could be used to design low-noise high-precision readout circuits for MEMS capacitance accelerometers. Each technique has its pros and cons, and the main challenges are how to choose the techniques and how to design the readout circuit to match the measurement range and noise requirement.

The main objective of this thesis are listed as follows:

- Objective 1: By using different methods (AZ, CDS, and CHS), design low-noise high-precision readout circuits. Analyze the noise sources and compare the pre-layout simulation result, then choose the proper technique.
- Objective 2: Optimize the sensitivity and structure to match the MEMS sensor and get the best noise performance.
- Objective 3: Design the layout of the circuit and do post-layout simulation. Compare and analyze the difference between pre-layout and post-layout simulation results.
1.4 Thesis Organization

The work is organized as follows:

Chapter 2 introduces the MEMS accelerometers and the following readout circuit. Several kinds of MEMS accelerometers will be mentioned, and capacitance accelerometers will be highlighted. Besides, some basic knowledge about noise sources in the sensor system will be presented.

Chapter 3 compares the three main techniques for low-noise readout circuits briefly at first. After that, the working principle of each method will be explained in detail. Then, the proposed design, simulation result, and noise analysis are shown in separate sections.

Chapter 4 illustrates the final design from the three techniques and then presents the post-layout simulation result and fabrication process. Next, it demonstrates the summary and discussion of the thesis work.

Chapter 5 concludes all the work and then depicts the future work.
Chapter 2  MEMS Accelerometers

In this chapter, we will introduce some basic knowledge about capacitance sensor readout circuits. MEMS sensors could be used in many kinds of applications. We focus on MEMS accelerometers and illustrate the fundamental working principle. After that, a brief introduction of different noise sources (including mechanical noise sources and electronic noise sources) is provided.

2.1 Accelerometers Classification

Accelerometers are devices that can convert acceleration into other kinds of physical quantities such as displacement, capacitance, voltage, frequency, and so on. The structure of the device determines the quantity.

2.1.1 Accelerometer Classifications from Different Aspects

There are three main types of MEMS accelerometers in nowadays applications: capacitive, piezoelectric, piezoresistive. Capacitive one is used most widely. Some other kinds, such as optical, electromagnetic, tunneling effects, are also used in some special situations. In this section, three types of accelerometers’ strengths and weaknesses are described briefly, and the capacitive one will be discussed in detail.

MEMS capacitance accelerometer has lower manufacturing cost and smaller sizes. Almost all of the mobile devices use this type. The measurement method determines that it has a limited bandwidth, and the input acceleration range is relatively small (less than 200g).
Piezoresistive [30-33] is another kind of accelerometer with DC response. The input acceleration causes resistance variation in strain gauges. It has a much higher bandwidth and can measure a pulse signal whose frequency is pretty high. However, the sensitivity of this sensor is relatively low, so that limits its precision. Another disadvantage is that it is sensitive to the variation of temperature. And its price is much higher than the MEMS capacitance accelerometer.

Piezoelectric accelerometers [34-37] usually use a special material to generate charge proportional to the acceleration. It has a comprehensive frequency response and high sensitivity. This sensor can also work in extreme conditions. Another advantage is that it has high efficiency of actuation and high linearity of properties. However, as an AC coupled device, it cannot measure static accelerations and vibrations at a pretty low frequency.

The accelerometers also have the classification of open-loop and closed-loop. The high-resolution accelerometers often work in an open-loop mode to avoid introducing additional electronic noise created by the feedback electronics elements. However, as the high-resolution accelerometers usually have a small full-range application, cause that the calibration effect of closed-loop could be ignored [38]. For the closed-loop design, it is often required in high Q sensing elements, large dynamic range, or high bias stability applications.

2.1.2 Capacitive Accelerometer

As the name suggests, a capacitive accelerometer transfers the accelerometer to capacitance, and then the capacitance is sampled by the readout circuit. The usually
sensing method is the gap changing. When an acceleration applies to the proof mass, the gap between sensor comb fingers changes. The sensitivity from acceleration input to capacitive $SF_{cap}$ (capacitive sensing scale factor) could be expressed as:

$$SF_{cap} \cong \left( \frac{m}{k} \right) \cdot \left( \frac{\varepsilon_0 \varepsilon_r A}{d^2} \right) = \frac{\varepsilon_0 \varepsilon_r A m}{kd^2}$$

(2.1)

Where $d$ is the gap distance between comb fingers, $A$ is the sensor comb fingers overlap area. $\varepsilon_0$ and $\varepsilon_r$ are the permittivity of vacuum and relative permittivity of air.

Capacitive MEMS accelerometers have many advantages, such as low drift, low power consumption, and low-temperature dependence [39].

### 2.2 Readout Circuit for MEMS Accelerometers

As the name suggests, the readout circuit could transfer the sensor’s output signal (such as capacitance, frequency, electromagnetic fields) to signals that can be processed by the circuits (such as voltage and current).

The most common readout circuit for the MEMS capacitance accelerometer is a capacitance-to-voltage converter (CVC) or capacitance-to-digital converter (CDC). Generally speaking, CVC applies drive voltage on both sides of the sensing capacitance and then amplifies the central node voltage to get output voltage. There is usually a following analog-to-digital converter (ADC) to transfer the voltage to a digital signal at last, but some methods applied on the CVC design could optimize the output noise floor.

The CDC usually uses the integrator to sample the capacitance charge and then transfer it to the digital signal directly. This process is often realized by the sigma-delta technique.
It is easier to get high precision, but its power consumption is higher. However, for ultra-low noise design, this operation also introduces considerable quantization noise. We will discuss the readout circuit design in detail in the next chapter.

2.3 Noise Sources

Our objective is to design a high-precision low-noise readout circuit for accelerometers. To achieve that requirement, we need to know where the noise comes from.

Noise is a random fluctuation of the quantity to be measured. It is unpredictable and unavoidable. Noise determines the minimum value of the signal that a circuit could deal with. Considerable noise will cause degeneration of the circuit’s performance. At the same time, noise is also a tradeoff with speed, power consumption, and other parameters.

This section introduces all of the primary noise sources of MEMS accelerometers, including mechanical thermal noise, electronic noise (thermal noise, flicker noise, and shot noise). Each section illustrates noises’ sources and characteristics.

2.3.1 Mechanical Thermal Noise

Mechanical thermal noise is originated from the random fluctuation of gas molecules, which causes the MEMS structure and damping gas to have energy transfers at a specific temperature.

Electronic systems and mechanical systems have a similar differential equation to describe the relationship between the RLC and spring-mass damper systems. The correspondences are shown in Table 2.1:
Table 2.1 Similarity between RLC system and spring-mass damper system.

<table>
<thead>
<tr>
<th>Electrical system</th>
<th>Mechanical system</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistance, R</td>
<td>Damping, D</td>
</tr>
<tr>
<td>Inductance, L</td>
<td>Mass, m</td>
</tr>
<tr>
<td>Capacitance, C</td>
<td>Compliance, $K^{-1}$</td>
</tr>
<tr>
<td>Voltage, V</td>
<td>Force, F</td>
</tr>
<tr>
<td>Current, I</td>
<td>Velocity, $\dot{x}$</td>
</tr>
<tr>
<td>Charge, q</td>
<td>Displacement, $x$</td>
</tr>
</tbody>
</table>

According to the electronic thermal noise $S_v(f) = 4kTR$, the mechanical thermal noise is given by:

$$\overline{F_n^2} = 4kTD \frac{N^2}{Hz}$$

where D is the viscous damping coefficient.

2.3.2 Electronic Thermal Noise

The electrons’ random movement in the conductor causes fluctuation of the voltage, even though there is neither applied current nor voltage. So, the noise spectral density is proportional to the absolute temperature [40].

The power spectral density keeps flat to a very high frequency (100THz) and decreases at higher frequencies. However, the limited bandwidth shows an almost Gaussian amplitude distribution. For this reason, it is precise enough to use white noise to describe the thermal noise. For a given resistor, its thermal noise could be modeled by a voltage source whose one-sided spectral density is:
\[ S_v(f) = 4kTR, \ f \geq 0 \]  

(2.3)

Where \( k \) is Boltzmann constant, \( T \) is the absolute temperature of the resistor, and \( R \) is the resistor’s value. The unit of \( S_v(f) \) is \( V^2/Hz \). For a given bandwidth \( \Delta f \), \( V_n \) stands for the root mean square (RMS) of noise, and it is given by:

\[ \bar{V}_n = \sqrt{4kTR\Delta f} \]  

(2.4)

Another way to model noise sources is to use Norton equivalent. It is convenient in some circuits. As \( \frac{\bar{V}_n^2}{R^2} = \bar{I}_n^2 \), the RMS of equivalent current noise is given by:

\[ \bar{I}_n = \sqrt{\frac{4kT\Delta f}{R}} \]  

(2.5)

![Figure 2.1 Equivalent noise source of the resistor.](image)

For the transistors, the electronic thermal noise is mainly from channels. If the long-channel transistor works in the saturation region, the noise can be modeled by a current source connected between drain and source, which is given by:
where $\gamma$ is a parameter determined by the channel length.

### 2.3.3 Flicker Noise

The floating band causes flicker noise at the interface of the gate oxide and silicon substrate. Charge carriers near the interface are trapped and released by these energy states randomly, which causes flicker noise in the drain current.

It is not easy to estimate the average power of flicker noise. It depends on the oxide-silicon interface’s cleanness and CMOS fabrication technology. Flicker noise can be modeled by a voltage source in series with the gate and given by:

$$\overline{V_n^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f}$$  \hspace{1cm} (2.7)

where $K$ depends on the process and is a constant on the order of $10^{-25}V^2F$. As the trapping and releasing occur easily at a lower frequency, the flicker noise is also called 1/f noise.

From the formula, we get that the flicker noise is inversely proportional to the product of width and length. An efficient way to reduce this noise is to increase the transistor area. It is common to apply a huge transistor in a low-noise design. Simultaneously, as holes have a more considerable distance to the silicon-oxide interface, PMOS transistors usually have lower flicker noise than NMOS transistors.
In electronic devices, flicker noise shows a low-frequency character because flicker noise is covered by white noise at a higher frequency. There is an important parameter $f_c$ which stands for the corner frequency.

![Figure 2.2 ADA4622-2 voltage noise spectral density [41].](image)

The corner frequency is the boundary between the region dominated by flicker noise and the region dominated by white noise [41].

### 2.3.4 Shot Noise

Shot noise is another type of electronic noise. We can use the Poisson process to model it. The charge of electrons makes up the current, the discrete nature of the electron charge, together with random fluctuations in a DC, causes shot noise.

In general cases, shot noise is ignorable. However, shot noise is different from the other two noises because it is independent of temperature and frequency. Therefore, shot noise may be the dominant noise in some high frequency and low-temperature situations [42].
2.3.5 Total System Noise

For an accelerometer, obviously, the noise should be equivalent acceleration, and the unit should be $g$. According to the previous illustration, the noise source could be divided into mechanical noise equivalent acceleration (MNEA) from the sensor and electronic noise equivalent acceleration (ENEA) from the readout circuit. The definition of the total noise equivalent acceleration (TNEA) is:

$$TNEA = \sqrt{MNEA^2 + ENEA^2} \quad (2.8)$$

Suppose there is an analog-to-digital converter (ADC) or a digital-to-analog converter (DAC). ADC usually appears at the sensor’s open-loop output and in the closed-loop control system, such as a MEMS sigma-delta modulator [43, 44]. In that case, the total noise should also consider the quantization noise equivalent acceleration (QNEA), so the new total noise equivalent acceleration (TNEA) is:

$$TNEA = \sqrt{MNEA^2 + ENEA^2 + QNEA^2} \quad (2.9)$$
Chapter 3  Low-noise Readout Circuit Design

In this chapter, we introduce the main kinds of techniques of low-noise readout circuits. These techniques have been widely used since the last century. In recent years, some new methods based on these fundamental methods are proposed. Some of them innovate the circuit structure, some optimize the clock signal and frequency, and some focus on the improvement of operational amplifier performance.

The three main approaches are auto-zero (AZ) and correlated double sampling (CDS) for switched-capacitor (SC) circuits and chopper stabilization (CHS) for continuous-time (CT) circuits.

In this chapter, the working principles of three techniques are described, the advantages and disadvantages will be discussed in detail. Afterward, some new methods for improving fundamental techniques will be introduced and compared with each other.

3.1 Techniques for Low-Noise Readout Circuits

3.1.1 Switch-Capacitor (SC) Solutions

Switch-capacitor circuits is a typical class of discrete-time system, and it is a fundamental part of some advanced circuits, such as filters, comparators, ADCs and DACs. SC circuits are widely used in the sampling system.

A simple example is given in Figure 3.1(a). Assuming that the amplifier’s open-loop gain is very high. In phase 1, S₁ and S₂ are on and S₃ is off. Figure 3.1(b) shows the equivalent circuit. For a high gain amplifier, \( V_B = V_{out} \approx 0 \), then the voltage between \( C_1 \) is approximately equal to 0. The charge stored on \( C_1 \) is equal to \( V_{in0}C_1 \). After that, when
\[ t = t_0, S_1 \text{ and } S_2 \text{ are off, } S_3 \text{ is on, node A connects to the ground, the voltage of } C_1 \text{ is equal to } 0. \text{ According to the principle of conservation of charge, the charge on } C_1 \text{ transfer to } C_2, \text{ then the output voltage becomes to } V_{in0} C_1 / C_2. \text{ Therefore, the SC circuit amplify } V_{in0} \text{ by a factor } C_1 / C_2. \]

![Diagram](image)

**Figure 3.1** Switched – Capacitor (SC) Amplifier.

There are some differences between SC circuits and continuous-time circuits. Firstly, SC needs to sample the input signal and cannot amplify the signal simultaneously. Secondly, after \( t_0 \), no matter how the input signal changes, the output only amplify the sampling signal, which is the input signal at \( t_0 \). Thirdly, as the SC circuit needs to transfer from one state to another in one loop, there exist stable issues.
3.1.1 Auto-zero (AZ) technique

A switched-capacitor (SC) circuit is a discrete-time circuit, which means the operation could be divided into sample and hold functions. If we could record the nonideal signal components and then subtract them from the output signal, it will eliminate the errors and improve the readout circuit’s accuracy.

Auto-zero (AZ) technique uses this idea. During the reset phase, the error is sensed and then feedback to the amplifier. The input signal will be amplified and then subtract nonideal components. The specific working principle will be explained in separate chapters of AZ.

3.1.1.2 Correlated double sampling (CDS) technique

Correlated double sampling (CDS) is another method used for the SC circuit. Initially, the difference between AZ and CDS is how to store the nonideal parts. For CDS, the error and noise signal is usually held on a capacitor, and the amplified signal need to subtract the error components and then goes to the next stage.

However, for nowadays designs, CDS often combines with the differential technique to sample the differential signal with the same error components. It then uses the differential output to eliminate the nonideal signals. The specific working principle will be explained in separate chapters of CDS.

3.1.2 Continuous-Time (CT) solutions

Continuous-time means the whole circuit, especially the amplifier, operates all the time. And the signals of all time transfer to the output terminal. For continuous-time design, we
don’t have a reset operation for each period, so it is hard to eliminate the noise in the time domain. However, continuous-time signal provides an opportunity for transformations in the frequency domain. Regarding the frequency domain, modulation is the most common technique. The chopping technology is based on the modulation method.

3.1.2.1 Chopper Stabilization technique (CHS)

Our input signal is the center node voltage, and it cannot change abruptly. That means it is a continuous-time signal and works in relatively low frequency. Suppose we could transfer the noise to high-frequency while keeping the signal at low-frequency. In that case, we could use a low-pass filter to eliminate a considerable amount of noise. That’s what chopper stabilization (CHS) does. The specific working principle will be explained in separate chapters of CHS.

3.1.3 Low-Noise Design in Amplifiers

The amplifier is the core of the readout circuit. The amplifiers deal with the signal and guarantee the circuit’s stability. What’s more, the amplifier is also the primary source of the noise. It is essential to decrease the noise floor of the amplifiers in our design. This section gives the amplifier’s primary noise source and lists some methods to reduce the noise.

3.1.3.1 Noise analysis of an amplifier

We have introduced different types of noise sources of circuits in chapter 2.3. This section gives some practical examples of amplifiers.
The transistor’s output thermal noise and flicker noise could be expressed as:

\[ \bar{I}_n^2 = 4kT \frac{2}{3} g_m, \quad \bar{V}_n^2 = 4kT \frac{2}{3} g_m r_D^2 \]  \hspace{1cm} (3.1)

\[ \bar{I}_{n,1/f}^2 = \frac{K}{c_{ox} W L f} \frac{1}{g_m^2}, \quad \bar{V}_{n,1/f}^2 = \frac{K}{c_{ox} W L f} \frac{1}{g_m^2} \]  \hspace{1cm} (3.2)

For a resistor, the thermal noise is:

\[ \bar{I}_n^2 = 4kT \frac{1}{R}, \quad \bar{V}_n^2 = 4kTR \]  \hspace{1cm} (3.3)

For the common-source amplifier, the total output noise could be written as:

\[ \bar{V}_{n,\text{out}}^2 = \left( 4kT \frac{2}{3} g_m + \frac{K}{c_{ox} W L f} g_m^2 + \frac{4kT}{R_D} \right) R_D^2 \]  \hspace{1cm} (3.4)

And as the gain is equal to \( g_m R_D \), the total input noise could be written as:

\[ \bar{V}_{n,\text{in}}^2 = \frac{\bar{V}_{n,\text{out}}^2}{A_v^2} = 4kT \frac{2}{3 g_m} + \frac{K}{c_{ox} W L f} \frac{1}{g_m^2} + \frac{4kT}{g_m^2 R_D} \]  \hspace{1cm} (3.5)
In practical cases, we usually use an active load (current mirror) to replace the resistor.

Figure 3.3 shows the structure:

![Figure 3.3](image)

(a) CS amplifier with active load; (b) equivalent model with noise sources.

After the replacement, the output thermal noise of the active load common-sources amplifier is:

$$V_{n,\text{out,thermal}}^{2} = 4kT\left(\frac{2}{3}g_{m1} + \frac{2}{3}g_{m2}\right)(r_{o1}||r_{o2})^{2}$$  \hspace{1cm} (3.6)

As the voltage gain $A_v = g_{m1} \cdot (r_{o1}||r_{o2})$, the input noise is:

$$V_{n,\text{in,thermal}}^{2} = 4kT\left(\frac{2}{3g_{m1}^{2}} + \frac{2g_{m2}}{3g_{m1}^{2}}\right)$$  \hspace{1cm} (3.7)

According to the expression, make $g_{m1}$ larger and $g_{m2}$ smaller could reduce the amplifier’s thermal noise. For this purpose, it is a feasible method to increase the current or make the transistor’s (input transistor, not the active load) width larger. However, increasing $I_d$ causes more significant power consumption and decreases the voltage
swing range, increasing the transistor’s width makes the input and output capacitance larger.

For flicker noise, as the input noise is proportional to $\frac{1}{WL}$, so the primary method is increasing the transistor’s area. It is normal to use a huge transistor as the input of the amplifier. The actual circuit design is always a compromise among speed, power consumption, output range, noise, and other parameters.

At last, for the differential amplifier, its noise is double of the single-ended amplifier. This conclusion will be used in the following chapters about the circuit’s noise analysis.

### 3.2 Auto-Zero (AZ)

Auto-Zero is one of the fundamental low-noise design methods. This section will introduce how it works, analyze the noise characteristic, and then apply it to the accelerometer readout circuit design.

#### 3.2.1 Work Principle of Auto-Zero (AZ)

The Auto-zero (AZ) fundamental idea is to sample the nonideal quantities (such as noise and offset) and then use the op-amp’s instantaneous value to subtract the sampled unwanted value. Figure 3.4 shows the basic principle of the AZ technique.
For the offset voltage, when $\varphi_2 = 1$, the op-amp is disconnected from the input signal. The two input terminals of the amplifier are short-circuited and keep their value at appropriate common-mode voltage. The offset voltage is amplified and then detected by $A_2$ and then sampled and hold. Due to the high open-loop gain of the amplifier, the output voltage is forced to approximate zero. Then, when $\varphi_2 = 0$, the input signal is amplified, then subtracts the holding offset voltage to get a more precise result.

According to the working principle, if the offset is constant over time, it will be eliminated by the auto-zero operation. The output of the amplifier will be ideal and not suffer from the offset components.

For low-frequency noise, such as 1/f noise, Auto-zero also affects. However, different from the offset, which could be regarded as constant, the noise is random and time-varying. Thus, the correlation between sampled noise and instantaneous noise determines the performance of auto-zero. As the sampling frequency is constant for noises of different frequencies, the correlation between them is vital, especially the noise whose frequency is lower or around sampling frequency. If the noise has a much higher
frequency than sampling frequency, such as wideband white noise, the correlation is very weak. So the AZ helps low-frequency noise but useless for high-frequency noise.

For the high-frequency random noise (such as thermal noise), a high-pass filter is used in the following stage, which could significantly decrease the noise at low frequency. However, since auto-zero is a sampling technique, the aliasing effect will transfer wideband noise to the baseband. Therefore, the wideband noise aliasing effect increases the in-band power spectral density (PSD).

In conclusion, Auto-Zero could eliminate the DC offset and strongly reduce the $1/f$ noise at low frequency. In exchange, AZ increases the broadband white noise foldover component. This component is because of the aliasing effect caused by sampling operation. The white noise (mainly thermal noise) multiplies a factor equal to equivalent noise bandwidth and Nyquist frequency ratio.

The last part of the AZ technique is the residual offset. The zero input signal with offset and noise generates an output voltage in the sampling phase. It is amplified and stored by a hold circuit. This voltage will create a control variable named $x_c$. In an ideal case, the control variable will eliminate the offset and noise entirely in the next phase. However, in the practical matter, there always exist some effects which cause some error $\Delta x_c$, such as charge injection and charge feedthrough during the switching process and the quantization error due to the ADC (Analog to Digital Converter). The error $\Delta x_c$ introduces residual offset. The strategy of decreasing residual offset also needs to be considered in circuit design.
3.2.2 Auto-Zero (AZ) Design

In this section, combining with a previous structure [39], an AZ low-noise readout circuit is applied. The whole design consists of sensing components, capacitance to voltage converter (CVC), variable gain amplifier (VGA), RC low-pass filter, and output buffer. The whole structure uses the AZ technique to improve the noise characteristic.

Meanwhile, to achieve a compromise among power consumption, performance and area, we use the time-multiplexed differential (TMD) technique to replace the differential amplifier. This structure uses the TMD signal to eliminate the offset and noise.

![Diagram of AZ design components](image)

Figure 3.5 Sensing component, CVC, and VGA of the AZ design.

The first three parts: sensing component, capacitance to voltage converter (CVC), and variable gain amplifier (VGA), are shown in Figure 3.5. \( V_{off} \) stands for the nonideal voltage sources, such as offset voltage, flicker noise.

3.2.2.1 Sensing circuit and time-multiplexed capacitance to voltage converter (TMD-CVC)

For the sensing component, there are two voltage sources \( V_{REF+} \) and \( V_{REF-} \) connecting to both sides of sensing capacitors. When the MEMS sensor is accelerated, the proof mass’s
displacement causes capacitors’ value changes on each side. One varies from $C_s$ to $C_s + \Delta C$, and another one becomes $C_s - \Delta C$. The control clock diagram of this design is shown in Figure 3.6:

![Control Clock Diagram](image)

**Figure 3.6 clock diagram of TMD-AZ design.**

The working principle of this design is shown as below:

(a) When $\phi_1$ is high, the circuit work in reset mode. Both sides of the sensing capacitor are zero, the input of the amplifier $OA_1$ is connected to the output, charge on $C_F$ is reset to zero.

(b) $\phi_1$ turns off and $T_1$ turns on. Positive reference voltage connects to $C_{1S}$ and negative reference voltage connects to $C_{2S}$. Due to the virtual ground effect of the amplifier, the negative input terminal of $OA_1$ is set to $V_{off}$. Because of the charge transfer of the capacitor $C_F$, the output voltage of op-amp varies to $V_{o1}$. 
(c) To stabilize the output signal, after a certain delay, $T_{1S}$ turns on, and the output voltage is sampled and stored on the hold capacitor $C_{h1}$.

(d) $T_1$ turns off and $\phi_1$ turns on again to reset the whole circuit. The charge on $C_F$ is reset to zero again.

(e) $\phi_1$ turns off and $T_2$ turns on. This time positive reference voltage is applied to $C_{2S}$ and the negative reference voltage is applied to $C_{1S}$. The output node of the op-amp is set to a new value.

(f) After a certain delay, $T_{2S}$ turns on, and the output voltage is sampled and stored on the hold capacitor $C_{h2}$

(g) All of the previous operations will repeat.

Note that as the clock edges don’t overlap each other, the glitch because of the spicks is greatly suppressed.

After the TMD-CVC process, the voltages stored on the two hold capacitor could be expressed as:

\[
V_{o1}(n) = -\frac{2V_{REF+}\Delta C_S}{C_F} + V_{off} - \frac{Q_{sw1}(n)}{2C_F}
\]

\[
V_{o2}(n + 1/2) = -\frac{2V_{REF-}\Delta C_S}{C_F} + V_{off} - \frac{Q_{sw1}(n+1/2)}{2C_F}
\]

Where $V_{REF+} = -V_{REF-}$, $\Delta C_S$ is the variation of the sensing capacitor due to the acceleration. $Q_{sw1}(n)$ and $Q_{sw1}(n + 1/2)$ are the channel charge errors caused by the off operation of the switches parallel to the feedback capacitor $C_F$ when reset ends.
As we applied differential reference voltage on sensing capacitors, the amplitudes of the $V_{o1}$ and $V_{o2}$ are the same, but signals are opposite. The time-multiplexing signal could be regarded as the differential signal.

What’s more, the time-multiplexing procedure repeats the same action of the sensing by the same devices. The low-frequency nonideal components, such as offset voltage, 1/f noise, switch error due to charge injection, clock feedthrough effect, and thermal drift [39], could be regarded as a common-mode error. As a result, the following stage could almost eliminate this error by the differential-to-single-ended operation. Also, some mismatches (such as feedback capacitor mismatch, switch mismatch) and asymmetry don’t need to be considered because of the same devices. Simultaneously, the common-mode-feedback (CMFB) block could be saved to reduce the area and power consumption.

### 3.2.2.2 Differential-to-Single-Ended Variable Gain Amplifier (VGA)

The following VGA transfers the TMD signal to the signal-ended signal. The operations and working principles are shown in Figure 3.6.

The switched-capacitor differential amplifier structure is proposed in [45]. It is shown separately in Figure 3.7:
Figure 3.7 Schematic of the switched-capacitor differential amplifier.

The difference between this structure and a traditional switched-capacitor is the two additional capacitor $C_3$ and $C'_3$. They are added to replace the switches at the position of $C_3$. In the traditional design, the output voltage is set to about zero every time during the reset phase. And in the amplify phase, a new output voltage is generated. In contrast, in this new structure, during the reset phase, $C_3$ is connected to the input and output node of the amplifier. As the output is not connected to input directly, the result does not change a lot but only slightly, which approximately equals the offset input voltage. The acceleration cannot produce mutation as long as the sampling rate is high enough. So the output value between the two adjacent periods cannot have an enormous difference. That means the difference between two adjacent output voltages is much smaller than the difference between zero and output voltage. Therefore, it is much easier to meet the high slew rate requirement. The output of the amplifier can also retain a more continuous value. Also, $C_3$ could help maintain the value of the input node at an almost zero value.
Therefore the charge could transfer to $C_3$ directly to improve the accuracy regardless of how large is the gain of the amplifier.

Regarding the working principle of this circuit, at first, the input nodes before $C_1$ and $C'_1$ are reset to zero. After the output signals of CVC sampled on $C_{h1}$ and $C_{h2}$ ($T_{1S}$ and $T_{2S}$ are off), $P_2$ is on. The sampled and hold voltage transmit to input nodes of VGA. Note that as the charge stored on $C_1$ and $C'_1$ have been released to zero, there exists charge sharing between $C_1$ and $C_{h1}$. So do $C_2$ and $C_{h2}$. The new value of input signal after charge sharing could be expressed as:

$$V_{o1}^* = \frac{C_{h1}}{C_{h1}+C_1} \cdot V_{o1}, \quad V_{o2}^* = \frac{C_{h2}}{C_{h2}+C_1} \cdot V_{o2} \quad (3.10)$$

After amplified by the VGA, the output voltage is:

$$V_{out} = \frac{C_2}{C_2} (V_{o1}^* - V_{o2}^*) = -\frac{C_1}{C_2} \cdot \frac{C_{h1}}{C_{h1}+C_1} \cdot \frac{2V_{REF} \cdot \Delta C_S}{C_F} \quad (3.11)$$

In the design, $C_{h1}$ is much larger than $C_1$ (6 times in this design) to reduce the voltage degeneration, which may decrease the accuracy of the operation circuit.

As the accelerometer’s test range may vary significantly in practical application, $C_2$ is usually designed to be a variable capacitor that could modify the whole readout system’s gain. There are two common ways to achieve that goal, one is adding external capacitors, and another one is using programmable capacitor arrays.

### 3.2.2.3 Operational Transconductance Amplifier (OTA) design

In this design, we need the OTA to have the characters of high-gain, low-noise, and high output range. As the sampling frequency is not quite high, there is no strict requirement
for the rate. Refer to the power consumption, the lower, the better. Therefore, a two-stage cascade operational amplifier is a good choice.

In light of the low noise amplifier’s previous illustration, a larger input pair aspect ratio could create larger transconductance, leading to a low noise floor. For the input pair in this design (MP1 and MP2), the aspect ratio is 250μm/180nm. For the transistors that are not on the signal path, a smaller aspect ratio could contribute less noise. Based on the experiment result that PMOS input usually has lower noise than NMOS input pair, the OTA schematic is shown in Figure 3.8:

![OTA schematic](image)

Figure 3.8 Schematic of the core OTA.

Considering the stability of the OTA, two compensation capacitors $C_1$ and $C_2$ are applied.

As these two capacitors do not connect to the Gate terminal of the transistors, which are
in the signal path, they will not introduce any dominant poles. So it is easier to guarantee the phase margin (PM) meets the stability requirement.

The Bode plot of the proposed OTA is shown in Figure 3.9:

![Bode plot of core OTA in AZ design](image)

Figure 3.9 Bode plot of core OTA in AZ design.

The single OTA’s phase margin is \(180° - 126.998° \approx 53°\), which guarantees signals steadily during amplifying operation. In the simulation, the clock period is 10 kHz. At this frequency, the gain is still larger than 80dB, which could ensure calculation accuracy.

### 3.2.2.4 Low-offset Low-Noise Output Buffer

To minimize the offset and strengthen the circuit’s load capacity, a low-offset low-noise output buffer is applied at the end of the design [46]. It is shown in Figure 3.10:
The cascade differential amplifiers (Stage 1 and Stage 2) significantly suppressed the input offset. Similarly, the high aspect ratio of the input pair (40\,\mu m/1\,\mu m for M_1 and M_2, 146.66\,\mu m/1\,\mu m for M_5 and M_6) create slight noise compare with the output noise floor of the low-pass filter. Stage 3 is a class-A output stage. A high gain structure is applied, which reduces the gain error to a minimum. The circuit achieves the low offset, low noise, and high common-mode rejection ratio (CMRR) requirements by combining the above characteristics.

The key of the first two stages is that the early stage output is clamped to the second gain stage directly, which cause the input voltage of M_5 and M_6 keep at almost the same value. Therefore, V_A and V_b follow each other, and then the systematic offset is reduced. That improves the circuit’s stability under variable supply voltage, process, and temperature.
To ensure the stability of the output buffer, compensation capacitors $C_{C1}$ and $C_{C2}$ and the compensation resistor $R_{C1}$ are added to improve the phase margin (PM) of the circuit. The transistor $M_{13}$ is added to meet the slew rate requirement of the class-A amplifier [47]. The Bode plot of the output buffer in AZ design is shown in Figure 3.11:

![Bode plot of the output buffer of AZ design](image)

According to the Bode plot, the phase margin of the output buffer is $180^\circ - 117.6775^\circ \approx 62^\circ$, which guarantees the output signal’s stability.

3.2.3 Simulation Result

3.2.3.1 Transient simulation result

The simulation result of the first stage is shown in Figure 3.12. According to the working principle illustrated in the previous part, the clock $\phi_1/2$ is the system clock. The CVC
finishes the two sample operations in one period and then stores them on the hold capacitor.

![Figure 3.12 Simulation result of TMD-CVC.](image)

From the clock diagram, we get that $T_1$ and $T_2$ turn on in different sub-periods when $\phi_1$ is low. Therefore, $CVC_{Vout}$ shows the different values (almost opposite) in the $n$ period and $(n + 1)$ period. $T_{1S}$ and $T_{2S}$ are the store clock. When it opens, there are new values stores on $C_{h1}$ and $C_{h2}$. The stored values will be used in the following VGA stage.

It seems that $V_{o1}$ and $V_{o2}$ are not differential because the result contains offset voltage, noise, and the switch error. The following differential structure will eliminate these nonideal components

The simulation result of the second stage (variable gain amplifier) is shown in Figure 3.13:
As mentioned before, when $P_2$ turns on, charge from stored capacitor transfer to $C_1$ and $C'_1$, at the same time, $V_{out}$ is set to a value close to the previous output voltage. When $P_1$ turns on, one side of $C_1$ connects to ground the amplifier $OA_2$ compute the output of this period.

From Figure 3.13, we find when $P_1$ turns on, Gain_vout is calculated to have a new value. However, there exists some spikes and high-frequency noise. After the low-pass filter, the curve becomes smooth. As long as the following circuit (ADC, for example) samples the output signal when $P_1$ is high, a proper value could be gotten.

From the previous analysis, the theoretical sensitivity from capacitance to voltage is:

$$V_{out} = -\frac{C_1}{C_2} \cdot \frac{C_{h1}}{C_{h1} + C_1} \cdot \frac{2V_{REF} + \Delta C_S}{C_F}$$

(3.12)
\[
\frac{V_{out}}{\Delta C} = - \frac{c_1}{c_2} \cdot \frac{C_{h1}}{C_{h1} + C_1} \cdot \frac{2V_{REF} + 2V_{REF}}{c_F} = - \frac{1pF \cdot 6pF}{100fF \cdot 7pF} \cdot \frac{2 \times 300mV}{2pF} \approx -2.571V/pF \quad (3.13)
\]

which is very close to the simulation result of the readout circuit.

![Graph showing the output voltage of AZ output buffer.](image)

Figure 3.14 The output voltage of AZ output buffer.

Our input range \( \Delta C \) varies from -500\( pF \) to 500 \( pF \). As the signal has gone through the low-pass filter, the output buffer’s output voltage curve becomes smoother. For the linearity, the result is shown in Figure 3.15:
Figure 3.15 The linearity of buffer output voltage.

The $R^2$ is still 0.99996, which stands for that the linearity is pretty good. The sensitivity after the low-pass filter and output buffer now is $2.568V/pF$. It is also very close to the theoretical result.

In conclusion, for the pre-layout simulation of AZ design, the result shows the readout circuit could work properly and has good linearity. The simulation sensitivity is very close to the theoretical value so that the circuit accuracy is high.

3.2.4 Noise Analyze

For the readout system, the primary noise source is the amplifier.

As our OTA is a two-stage cascode structure, according to [48], for a multistage amplifier, the noise figure is primarily determined by the first stage. It has been illustrated
that for the long-channel transistor, the noise parameter $\gamma$ equals 2/3 [40]. For our design, the first stage is a cascode amplifier, and its input-referred noise could be expressed as:

$$
\overline{V_{n,\text{in}}^2} = 8kT \left( \frac{2}{3g_{mP1,2}} + \frac{2g_{mN3,4}}{3g_{mP1,2}^2} \right) + \frac{2K_p}{(WL)_{P1,2}C_{oxf}} + \frac{2K_N}{(WL)_{N3,4}C_{oxf}} \frac{g_{mN3,4}^2}{g_{mP1,2}^2}
$$

(3.14)

From the expression, we find that: to make the noise lower, we need to make the input pairs’ transconductance ($g_{mP1,2}$) higher and the transconductance of the active load ($g_{mN3,4}$) (current mirror) lower.

For our design, as the input pairs’ aspect ratio is pretty high, while the active loads’ are much lower, the input-referred noise is simplified to:

$$
\overline{V_{n,m}^2} \cong \frac{16kT}{3g_{mP1,2}} + \frac{2K_p}{(WL)_{P1,2}C_{oxf}}
$$

(3.15)

The output noise simulation result is shown below:
The specific value of the output noise of AZ design is listed in the table below:

Table 3.1 Result of output noise of different input capacitance of AZ.

<table>
<thead>
<tr>
<th>Delta C (fF)</th>
<th>Output noise (µV/√Hz)</th>
<th>Delta C (fF)</th>
<th>Output noise (µV/√Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-500</td>
<td>102.515</td>
<td>50</td>
<td>24.89944</td>
</tr>
<tr>
<td>-450</td>
<td>19.79024</td>
<td>100</td>
<td>11.18485</td>
</tr>
<tr>
<td>-400</td>
<td>18.04969</td>
<td>150</td>
<td>8.505513</td>
</tr>
<tr>
<td>-350</td>
<td>34.64528</td>
<td>200</td>
<td>8.044562</td>
</tr>
<tr>
<td>-300</td>
<td>42.0216</td>
<td>250</td>
<td>6.860267</td>
</tr>
<tr>
<td>-250</td>
<td>26.72523</td>
<td>300</td>
<td>5.950309</td>
</tr>
<tr>
<td>-200</td>
<td>26.29901</td>
<td>350</td>
<td>5.053883</td>
</tr>
<tr>
<td>-150</td>
<td>24.61235</td>
<td>400</td>
<td>5.744181</td>
</tr>
<tr>
<td>-100</td>
<td>27.74601</td>
<td>450</td>
<td>7.18987</td>
</tr>
<tr>
<td>-50</td>
<td>31.10819</td>
<td>500</td>
<td>10.39555</td>
</tr>
<tr>
<td>0</td>
<td>28.96953</td>
<td>Ave</td>
<td>18.68978</td>
</tr>
</tbody>
</table>
As the output noise of -500fF (input capacitance’s lower limit) is pretty large, we did not include it when calculating the average noise. Note that there is an interesting point that the lowest output noise does not appear when input is zero, but at $\Delta C = 350fF$.

When we print the noise figure of $\Delta C = 350fF$ and $\Delta C = 250fF$, Figure 3.17 shows the result:

![Table](image)

Figure 3.17 (a) Noise figure of $\Delta C = 350fF$; (b) Noise figure of $\Delta C = 250fF$.

Comparing the two results, we find that the dominant component is from I11/MP7, where I11 is the OTA of the second stage, and MP7 is the current source of the differential pair.

In the previous analysis, we ignore the noise from MP7. Because for a differential pair, the drain terminal could be regarded as a virtual ground. The current that goes through the current source could keep its value. So its noise would not be introduced in the signal path. However, there is no common-mode feedback (CMFB) component in this design,
and the common-mode voltage of the time-multiplexed signal is not zero. Although the common-mode voltage could be regarded as offset and canceled by the differential amplifier, it changes the operation point of the current source. Then the current source's noise is introduced into the signal path, and it dominates the whole readout circuit’s noise. The noise of MP7 increases when the operation point’s drift becomes larger.

For the equivalent zero input capacitance noise at the input node (there is common-mode voltage in the signal, so we choose DeltaC = 350fF as the zero input), we get:

\[
Noise_C = \frac{\text{Noise}_V}{\text{sensitivity}_{C \to V}} = \frac{5.053883 \mu V/\sqrt{Hz}}{2.571 \times 10^{12}V/F} = 1966zF/\sqrt{Hz} \tag{3.16}
\]

In conclusion, the time-multiplexed differential technique could reduce the complexity of the readout circuit and the area, simultaneously improve the mismatch and asymmetry of the devices, and omit the common-mode feedback module. The differential structure could also cancel the charge error and offset. However, without CMFB, the common-mode voltage drifts from the ground. The noise of the current source is introduced to the signal path and then causes a large amount of noise.

### 3.3 Correlated Double Sampling (CDS)

#### 3.3.1 Work Principle of Correlated Double Sampling (CDS)

Correlated Double Sampling (CDS) is another technique used for switched-capacitor (SC) circuits. There are some similarities between CDS and AZ. CDS could be described as a combination of AZ and hold operation [49]. The main difference is that the amplifier noise and offset are correlated sampled twice in one period to eliminate the error. The structure of the basic CDS readout circuit is shown in figure 3.18.
The difference between primary sampling circuits is that a CDS circuit add an error-storage capacitor $C_H$ and another clock phase. At first, all of the reset switches are closed. There is no input signal, and the charge on both sides of $C_H$ is also equal to zero. At the end of the reset phase, $S_1$ (sampling switch) opens. During the signal sensing phase $\phi_{SN1}$, as there is still no input signal, all the unexpected voltage (thermal noise, 1/f noise, offset, injecting charge) will be stored on $C_H$. After that, during the signal sensing phase $\phi_{SN2}$, $\pm V_S$ are applied to sensing capacitors, while, the instantaneous signal including not only input signal but also errors. However, as the error has been stored on $C_H$, the error is subtracted from the signal.

Although AZ and CDS’ operations have a slight difference, AZ’s output is still the signal but subtracts the error in the amplifier. The output of CDS is a sample and hold circuit. The effects of AZ and CDS on noise are pretty similar. Their transfer function is both zero at the origin, so that eliminates offset and 1/f noise hugely. For the other noise...
component, apart from the baseband, the foldover effects are similar because they both have sampling operations.

Actually, nowadays, readout circuit design often uses a structure like a differential CDS circuit to eliminate the noise. One sample is shown below [22]:

![Figure 3.19 Schematic of Correlated Double Sampling (CDS) [22].](image)

With a differential drive voltage, the input voltage is shown as:

\[ V_{in+} = -V_0 + V_{error1} \]  \hspace{1cm} (3.17)

\[ V_{in-} = V_0 + V_{error2} \]  \hspace{1cm} (3.18)

Where \( V_{error1} \) and \( V_{error2} \) includes offset and noise. They stand for the error voltage of two sampling phases. During \( \phi_1 \), the charge on \( C_{cds} \) is shown below:

\[ Q_{cds1} = -V_{in+} \cdot C_{cds} \]  \hspace{1cm} (3.19)

After that, during \( \phi_2 \), the result will be a new charge subtract the previously-stored charge on \( C_{cds} \).
\[ V_{\text{cds}} = \frac{-V_{\text{in}+} + V_{\text{in}-}}{C_{\text{cds}}} \approx 2V_0 \] (3.20)

This result shows that the correlated double sampling operation eliminates the error. The following differential amplifier could be added to realize the subtraction operation.

### 3.3.2 Correlated Double Sampling (CDS) design

The CDS design is shown in figure 3.20 [51]:

- **(a) Precharge phase 1**
- **(b) Sample phase 1**
- **(c) Precharge phase 2**
- **(d) Sample phase 2**

Figure 3.20 Working principle of Correlated Double Sampling (CDS) process.
In the precharge phase, the charge on $C_{SAMPLE}$ is set to zero. Due to the high gain of the amplifier and the OTA’s negative feedback, the center node of the sensor capacitor ($C_{SENS}$) and reference capacitor ($C_{REF}$) is set to virtual ground ($V_{REF}$). When entering the sample phase, $C_{SENS}$ and $C_{REF}$ switch their polarity, and the switch turns off. The OTA amplifies the center node voltage, which is proportional to $C_{SENS}$ and $C_{REF}$. The same operation is repeated in the second period. And the output voltage of the second period has the same magnitude but opposite sign. Therefore, the two output voltage $V_{OUT1}$ and $V_{OUT2}$ have differential signal and contain the same $V_{REF}$ variation and offset voltage ($V_{OS}$). These components could be regarded as common-mode signals and eliminated by the differential output. The output voltages during the operation are shown below:

$$V_{OUT1} = \frac{C_{SENS}-C_{REF}}{C_{SAMPLE}} \cdot VDD + (V_{REF} + V_{OS})$$ \hspace{1cm} (3.21)

$$Q_{SAMPLE1} = (C_{SENS} - C_{REF}) \cdot VDD$$ \hspace{1cm} (3.22)

$$V_{OUT2} = \frac{C_{REF}-C_{SENS}}{C_{SAMPLE}} \cdot VDD + (V_{REF} + V_{OS})$$ \hspace{1cm} (3.23)

$$Q_{SAMPLE2} = (C_{REF} - C_{SENS}) \cdot VDD$$ \hspace{1cm} (3.24)

After applying the differential output, the output voltage is:

$$V_{OUT} = V_{OUT1} - V_{OUT2} = 2 \cdot \frac{C_{SENS}-C_{REF}}{C_{SAMPLE}} \cdot VDD$$ \hspace{1cm} (3.25)

$$Q_{SAMPLE} = Q_{SAMPLE1} - Q_{SAMPLE2} = 2 \cdot (C_{SENS} - C_{REF}) \cdot VDD$$ \hspace{1cm} (3.26)

The output result shows that the CDS process eliminates the common-mode signal components ($V_{REF}$ and $V_{OS}$). But as the theoretical analysis illustrates, the high-frequency
noise components (such as thermal noise and flicker noise) still exist in the differential output signal.

### 3.3.3 Simulation Result

The transient simulation result is shown in Figure 3.21:

![Figure 3.21 the transient simulation output voltage of CDS design.](image_url)

The transient simulation result shows good linearity and signal stability. To verify it, Figure 3.22 shows the linearity of the output voltage vs. different input capacitance:
The linearity result shows that the $R^2$ equals to 0.99969, which is enough to guarantee the linearity. The slope is about $1.752V/pF$.

Referring to the theoretical analysis, the sensitivity from capacitance to voltage is shown as:

\[
\frac{V_{out}}{\Delta C_S} = \frac{V_{DD}}{C_{SAMPLE}} = \frac{1.8V}{1pF} = 1.8V/pF
\]  \hspace{1cm} (3.27)

There is some difference between the theoretical value and the actual value. The reason is that when the output voltage is approximately $VDD$ or ground, the amplifier has a little distortion.
3.3.4 Noise Analyze

The output noise of the CDS design is shown in Figure 3.23:

![Figure 3.23 Output noise of AZ simulation with the different input capacitance.](image)

The results show that except for the full range input capacitance (500fF and -500fF), the difference among other output noises is relatively tiny. The output noise values at 200Hz are listed in Table 3.2:
Table 3.2 Result of output noise of different input capacitance of CDS.

<table>
<thead>
<tr>
<th>Delta C (fF)</th>
<th>Output noise ($\mu V/\sqrt{Hz}$)</th>
<th>Delta C (fF)</th>
<th>Output noise ($\mu V/\sqrt{Hz}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-500</td>
<td>0.711102</td>
<td>50</td>
<td>1.61726</td>
</tr>
<tr>
<td>-450</td>
<td>1.31741</td>
<td>100</td>
<td>1.6172</td>
</tr>
<tr>
<td>-400</td>
<td>1.5631</td>
<td>150</td>
<td>1.61741</td>
</tr>
<tr>
<td>-350</td>
<td>1.58931</td>
<td>200</td>
<td>1.61727</td>
</tr>
<tr>
<td>-300</td>
<td>1.59964</td>
<td>250</td>
<td>1.61668</td>
</tr>
<tr>
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<td>1.6055</td>
<td>300</td>
<td>1.6194</td>
</tr>
<tr>
<td>-200</td>
<td>1.60905</td>
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</tr>
<tr>
<td>-150</td>
<td>1.61188</td>
<td>400</td>
<td>1.60015</td>
</tr>
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<td>1.61392</td>
<td>450</td>
<td>1.41632</td>
</tr>
<tr>
<td>-50</td>
<td>1.61561</td>
<td>500</td>
<td>0.91895</td>
</tr>
<tr>
<td>0</td>
<td>1.61181</td>
<td>Ave</td>
<td>1.509542</td>
</tr>
</tbody>
</table>

From the noise summary, we find that the dominant noise source is the flicker noise of the input pair and the active loads. For the flicker noise, it could be expressed as:

$$\overline{V_{n,\text{out}}^2} = \frac{K}{c_{ox}W L} \frac{1}{f} g_m^2$$  \hspace{1cm} (3.28)

where $g_m = 2I_D/(V_{GS} - V_{th})$. As the current mirror is applied in this design, $I_D$ is almost a constant. The input capacitance only imposes a small signal at the gate of the input pair. So the $g_m$ changes a little. Therefore, the noise of the input pair and active load varies slightly. While when the input is a full range, the $V_{DS}$ of the input pair and active loads change a lot so that the transistor is not in the saturation region. For this reason, the output noise has a more considerable change.

For the equivalent zero input capacitance noise, it could be calculated by:

$$\text{Noise}_C = \frac{\text{Noise}_{V}}{\text{sensitivity}_{C\text{ to }V}} = \frac{1.61181 \mu V/\sqrt{Hz}}{1.752 \times 10^{12} \text{V/F}} = 919.98 \text{zF/}\sqrt{Hz}$$  \hspace{1cm} (3.29)
Note that it is much lower than the AZ design. However, the AZ design has a variable gain stage of realizing transfer differential signal to single-ended and following low-pass filter, which introduces some other extra noise sources.

The most important thing is that according to the noise summary of AZ and CDS design, the flicker noise always dominates all the noise sources. Unfortunately, as illustrated in the theoretical part, the SC circuit’s two techniques could eliminate the very low-frequency noise and DC noise. However, they do not have a strong enough effect on the flicker noise at our circuit’s operating frequency.

In conclusion, the CDS design could read the input capacitance properly and have acceptable linearity. What’s more, the CDS design achieves a better noise floor than the AZ design, although without the differential output and low pass filter. However, neither AZ nor CDS technologies allow us to achieve the ultra-low noise requirements at a frequency of 200 Hz, so we investigated the chopper stabilization (CHS) design which enables us to shift the flicker noise from low frequencies to higher frequencies.

3.4 Chopper Stabilization (CHS)

Unlike AZ or CDS techniques, the chopper stabilization (CHS) technique is a continuous-time method so that the sample and hold operation is not allowed. It is not feasible to subtract the nonideal component from the signal.

In this section, we will first introduce the working principle of chopper stabilization (CHS) briefly. Then we discuss the CHS design and finally present the simulation results and noise analysis.
3.4.1 Work principle of Chopper Stabilization (CHS)

For the continuous-time circuit, modulation is a typical operation. CHS also uses modulation and demodulation to eliminate the nonideal signal components.

Figure 3.24 Chopping principle including signals in frequency and time domain [52].

Figure 3.24 shows the chopping principle. The original signal has a low frequency, then modulated by the chopper to a much higher chopping frequency. In the frequency domain, the signal after modulation appears at the chopping frequency and its odd harmonics, while the offset is in the baseband. Then the signal and offset are amplified together. After that, the signal is demodulated to baseband again, while offset and noise are modulated to chopping frequency.

A vital property of the chopper stabilization technique is that the signal is modulated twice. So the signal still has a low frequency at the output. In contrast, the amplifier’s nonideal component (offset, noise) is only modulated once so that it has a high frequency at the output. Then the nonideal components could be eliminated by the low-pass filter.
Unlike AZ and CDS, as long as the chopping frequency is higher than 1/f noise corner frequency, the white noise components are almost equal to the wideband thermal noise. Without sample operation, it couldn’t fold the wideband thermal noise back to the baseband. Due to the excellent 1/f noise characteristics at low frequencies, CHS is widely used in the readout circuit, especially the designs with ultra-low noise requirements.

However, CHS is not perfect. First, the low pass filter limits the circuit’s bandwidth. Besides, the residual offset is another main nonideal component. The residual offset is mainly from the input chopper spikes [7]. The spikes are caused by the mismatch of charge injection of the switches. After demodulation, the spikes are transferred to residual offset. The process is shown in Figure 3.25:

Figure 3.25 Residual offset caused by spikes. (a) Spike signal; (b) Demodulation signal; (c) Demodulated spike [52].
From Figure 3.25, the residual offset is proportional to the chopping frequency, so lower the chopping frequency is a method to reduce the residual offset. It could also be reduced by lowering the input impedance and charge injection. However, the first method is not practical as the chopping frequency must higher than the corner frequency. The input impedance is also not easy to optimize because it depends on the input source. Well-matched transistors in layout could improve the charge injection. By using nested-chopper and some other techniques for the readout circuit, an offset lower than 100nV could be achieved.

Chopping ripple is another nonideal component and appears at the amplifier’s output. The modulated offset creates it in high frequency. Some other techniques, such as a notch filter [53] and an AC-coupled ripple reduction loop [54], could eliminate the ripple. However, these structures also introduce some extra filtering or complexity.

3.4.2 Chopper Stabilization (CHS) Design

3.4.2.1 Separate parts of the whole readout circuit

The chopper stabilization design is shown in Figure 3.26:
Figure 3.26 Schematic of CHS readout circuit design.

The readout circuit consists of five parts: MEMS sensor, capacitance-to-voltage converter (CVC), variable gain amplifier (VGA), demodulator, and low pass filter (LPF).

There are two opposite clock $\phi_1$ and $\phi_2$, they could be regarded as a modulator and create the chopper input signal. When the acceleration is applied to the sensor, the proof mass’s displacement causes the capacitance bridge variation. The imbalance of capacitance causes charge redistribution. The differential charge is integrated into the feedback capacitor $C_{\text{int}}$ and is proportional to the capacitance difference $\Delta C_s$. The output of CVC is:

$$V_{out1,1} = \frac{\Delta C_s}{C_{\text{int}}} \cdot V_{\text{drive}}, \quad V_{out1,2} = -\frac{\Delta C_s}{C_{\text{int}}} \cdot V_{\text{drive}}$$

(3.30)

where $V_{\text{drive}}$ is the MEMS sensor’s drive voltage, and the $V_{\text{CM}}$ in Figure.3.26 is the common-mode voltage. In this design, it is ground.
The third stage is a variable gain amplifier, and the gain is defined by the input capacitor $C_a$ and feedback capacitor $C_b$, the gain is:

\[
V_{out2,1} = \frac{C_a}{C_b} \cdot V_{out1,1}, \quad V_{out2,2} = \frac{C_a}{C_b} \cdot V_{out1,2}
\]  

(3.31)

Therefore, the output voltage is:

\[
V_{out} = V_{out2,1} - V_{out2,2} = 2 \cdot \frac{\Delta C_s}{C_{int}} \cdot \frac{C_a}{C_b} \cdot V_{drive}
\]  

(3.32)

3.4.2.2. Operational transconductance amplifier (OTA) design

Our design needs low noise, high gain, and high output range. The requirement of the circuit’s speed requirement is not very high, so the two-stage amplifier is a proper choice. The amplifier we used is shown in Figure 3.27.

Figure 3.27 Differential two-stage amplifier.
In the first stage, we use telescopic topology. The second stage is a class-A amplifier to achieve a high output range. To reduce the 1/f noise, a large input pair (250μm/180nm) is selected. $V_{P1}$ and $V_{N1}$ are two bias voltage. $C_1$ and $C_2$ are the feedback capacitor to improve the phase margin (PM). $V_{CM}$ is connected to the common-mode feedback (CMFB) component to stabilize the output signal’s operation point. The CMFB topology is shown in Figure 3.28:

![Figure 3.28 Common-mode feedback structure of OTA.](image)

For a differential amplifier, its advantage is that the differential topology could eliminate the error created by the circuit because of its symmetry. Simultaneously, a disadvantage is that another CMFB structure is needed to guarantee the stabilization of the output signals’ common-mode voltage. If not, it is possible to have a common-mode voltage drift which causes the circuit can not to work correctly. The resistor and capacitor bridge sense the common-mode voltage of the output ($V_{out,CM}$). Then the $V_{out,CM}$ is compared with the reference common-mode voltage $V_{CMREF}$. In this design, as $V_{DD}$ is 1.8V and $V_{SS}$ is -1.8V, the $V_{CMREF}$ is defined as $V_{CMREF} = (V_{DD} + V_{SS})/2 = 0V$. If $V_{out,CM}$ is larger
than $V_{CMREF}$, the output of the CMFB amplifier $V_{CM}$ will be lower, which makes the $V_{out,CM}$ lower, then form the negative feedback and vice versa.

### 3.4.2.3. Bias resistor design

A bias resistor is added between the input and output of the amplifier and parallel to the feedback capacitor to define the common-mode voltage at the amplifier’s input. As the internal CMFB net stabilizes the common-mode output voltage, the resistor could apply the same DC common-mode operation point at the input. However, to avoid affecting the feedback capacitor’s operation, we need to guarantee that the bias resistor’s impedance is much larger than the feedback capacitor at the working frequency (chopping frequency). So, the resistor’s is selected by the limitation shown below [55]:

$$R_f \geq \frac{100}{2\pi f_C C_f}$$  \hfill (3.33)

where $f_C$ is the chopping frequency and $C_f$ is the value of the feedback capacitor. As our feedback capacitors are in the pF order, and chopping frequency is 100 kHz, we have:

$$R_f \geq \frac{100}{2\pi \cdot 100kHz \cdot 1pF} \approx 160 M\Omega$$  \hfill (3.34)

It is too large to make a poly resistor on the chip. Transistors working in the deep subthreshold region could be used. The schematic of the bias resistor is shown in Figure 3.29:
This bias resistor consists of two antiparallel series PMOS. As the voltage between VGA’s input and output is much larger than that of CVC’s, the transistor size for CVC is \(360\, \text{nm} / 1\, \mu\text{m}\), while for VGA, it is \(360\, \text{nm} / 18\, \mu\text{m}\).

### 3.4.2.4. Current source

The current source schematic is shown in Figure 3.30.
$M_1$ is biased in the weak inversion region, and its aspect ratio is large so that the bias current is defined as:

$$I_{ref} = \frac{V_{SG1}}{R_1}$$  \hspace{1cm} (3.35)

This current source could offer a robust reference current. By applying supply voltage from 1.6V to 2.2V, the variation of the reference current result is shown in Figure 3.31:

![Reference current variation with VDD variation](image)

Figure 3.31 Reference current variation with VDD variation.

The result shows that the reference current only changes 32.6nA, which won’t influence the readout circuit’s operation.

### 3.4.3 Simulation results

The transient simulation result is shown in Figure 3.32. From the result, a chopper ripple is shown, but it has a small value of 50mV. When we use a low pass filter with a lower cutoff frequency and make the circuit works at a lower frequency, the ripple could be improved. The residual offset is strongly reduced by the differential structure.
Figure 3.32 Transient simulation result of CHS.

This result also shows excellent linearity. The linearity and linear fitting results are shown in Figure 3.33. The $R^2$ is 0.99999, which is pretty high. And the slope is $5.73\text{V/pF}$. 
Figure 3.33 Linearity of CHS differential output signal.

In the design section, we introduced that the output voltage could be expressed as:

\[ V_{\text{out}} = 2 \cdot \frac{\Delta C_s}{C_{\text{int}}} \cdot \frac{C_a}{C_b} \cdot V_{\text{drive}} \]  

(3.36)

Then we get the sensitivity of the readout circuit is:

\[ \frac{V_{\text{out}}}{\Delta C_s} = 2 \cdot \frac{C_a}{C_{\text{int}}} \cdot \frac{C_b}{1pF} \cdot V_{\text{drive}} = \frac{2}{600fF} \cdot \frac{1pF}{1.8V} = 6V/pF \]  

(3.37)

There is some difference between the theoretical result and the practical result. The main reason is that the parasitic capacitance will share the sensing capacitor and feedback capacitor's charge, which causes accuracy distortion. Another main reason is that the demodulation and low pass operation also decrease the precision a little. However, as the linearity of the readout circuit is acceptable, the accuracy degeneration could be compensated by modifying the gain slightly.
Another interesting topic is the spectrum analysis of the different stage signals. The spectrum result is shown in Figure 3.34:

The purple and orange curves are the spectrum amplifier outputs of stage 1 and stage 2. As the design’s chopping frequency is 100 kHz, the signal’s main component concentrates on 100 kHz, and others are concentrated on the odd harmonics of 100 kHz. This result matches the theoretical analysis. After demodulation (shown as the red curve), the signal is moved to the baseband, and there are still some signals on the wideband, although the density is small. According to the result, the minimum frequency of the portion is 200 kHz, which is larger than the chopping frequency. It is easy to eliminate the high-frequency components by a low pass filter. After that, only the baseband signal
exists. The results of spectrum analysis perfectly verify the working principle of the chopping method.

### 3.4.4 Noise Analysis

The output noise of different $\Delta C$ is shown in Figure 3.35. Due to the chopping technique using the frequency domain method like modulation, the output noise density spectrum is different from the result of SC circuits.

![Figure 3.35 Noise result with different $\Delta C$.](image)

The chopping stabilization technique shows better noise characteristics at low frequency, which is more in line with the accelerometer requirements. The output noise at 200Hz is shown in Table 3.3:
Table 3.3 Output noise of CHS at 200Hz.

<table>
<thead>
<tr>
<th>Delta C (fF)</th>
<th>Output noise ($nV/\sqrt{Hz}$)</th>
<th>Delta C (fF)</th>
<th>Output noise ($nV/\sqrt{Hz}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-500</td>
<td>281.93</td>
<td>50</td>
<td>103.18</td>
</tr>
<tr>
<td>-450</td>
<td>163.98</td>
<td>100</td>
<td>103.78</td>
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<tr>
<td>-400</td>
<td>146.34</td>
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<td>-350</td>
<td>135.04</td>
<td>200</td>
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</tr>
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<td>281.93</td>
</tr>
<tr>
<td>0</td>
<td>102.4</td>
<td>Ave</td>
<td>138.089</td>
</tr>
</tbody>
</table>

According to the table, the noise of the chopper stabilization design is much lower than the two SC designs (AZ and CDS). Simultaneously, the components of the noise are also different. Figure 3.36 shows the noise summary of the output noise of the CHS design.
From the noise summary, the 1/f noise is no longer the dominant component. The most significant part is contributed by the thermal noise of low pass filter resistors. I7 and I74 are the amplifiers of CVC and VGA. They also contribute some noise but not dominant. At the same time, as we make a pretty large size for the input pair (M1 and M2), their 1/f noise is also limited.

For the equivalent zero input capacitance noise, it could be expressed as:

$$ \text{Noise}_c = \frac{\text{Noise}_{V}}{\text{Sensitivity}_c} = \frac{102.4 \text{nV}/\sqrt{\text{Hz}}}{5.72962 \times 10^{12} \text{V}/\text{F}} = 17.87 \text{zF}/\sqrt{\text{Hz}} $$  (3.38)
There is an order of magnitude lower than AZ and CDS designs. Note that if the low pass filter resistor is lower, there is still space to improve the noise, although the price is to use a larger capacitor, which means a larger area. Another method is to use a smaller resistor or a large external capacitor. It is easier but causes degradation of integration.

Figure 3.37 Input and output noise VS output voltage.

Another point is that when we decrease the sensitivity, the output range also decreases. The input-referred noise, which equals output noise divided by sensitivity, has an optimum value. It is important to match the sensor’s input range and parasitic capacitance with a proper sensitivity and output range.

When sweeping other parameters, such as input capacitance range, Ca, Cb, and Cint, an optimum point exists that has the best noise characteristic. We do the noise optimization for all the parameters in the circuit and get the best noise value at the end.
3.5 Comparison of Different Techniques

In this chapter, we introduced three main techniques, designed corresponding circuits, and got simulation results. For the transient simulation result, three designs all have pretty good linearity. Their output voltages are closed to the theoretical value. AZ and CDS have more stable values but need an extra phase to reset. CHS output voltage has a chopping ripple due to the modulation operation, but it is continuous and could be sampled at any time. In conclusion, they all could work properly and give accurate results corresponding to the input signals.

The main difference among the three designs is the noise characteristic. For AZ and CDS, the low-frequency 1/f noise of the input pair and current source transistors dominate the noise figure. For CHS design, as the chopper technique is applied to eliminate the 1/f noise, transistors still contribute some 1/f noise, but they are no longer the dominant components. The noise sources are evenly distributed throughout the whole circuit. The CHS technique could decrease the 1/f noise a lot to optimize the readout circuit’s low-frequency noise.

<table>
<thead>
<tr>
<th>Designs</th>
<th>Zero input capacitance output noise units</th>
<th>C to V sensitivity</th>
<th>Input equivalent capacitance noise units</th>
</tr>
</thead>
<tbody>
<tr>
<td>AZ</td>
<td>5.054E-06 V/Sqrt(Hz)</td>
<td>2.57E+12 V/F</td>
<td>1.966E-18 F/sqrt(Hz)</td>
</tr>
<tr>
<td>CDS</td>
<td>1.612E-06 V/Sqrt(Hz)</td>
<td>1.75E+12 V/F</td>
<td>9.1998E-19 F/sqrt(Hz)</td>
</tr>
<tr>
<td>CHS</td>
<td>1.02E-07 V/Sqrt(Hz)</td>
<td>5.73E+12 V/F</td>
<td>1.787E-20 F/sqrt(Hz)</td>
</tr>
</tbody>
</table>
Chapter 4  The Proposed Design and Post-Layout Simulation Result

4.1 Post-layout simulation result

After the optimization, we choose 1.35V as the full output range, and the input capacitance range is from -600fF to 600fF. In the pre-layout simulation, the output noise of zero input at 200Hz is about 90 nV/Sqrt(Hz).

Figure 4.1 Layout of CHS two-stage CMFB amplifier.

Then we do the layout for each component and then integrated them into a whole system layout. The layouts of some core components are shown in Figure 4.1 to Figure 4.3.
To reduce the mismatch of the amplifier, the layout of the CHS CMFB amplifier is distributed in a strict symmetric structure. This method could minimize the imbalance and nonideal components caused by the mismatch and asymmetric of the transistors and transmission gates. Keeping the current in the two branches of the OTA equal is important. Without guaranteeing the virtual ground at the drain terminal of the current source transistor, the none-virtual-zero voltage generates much noise in the signal path. As the current source transistor always loads a large amount of current, the noise usually has a considerable effect and even dominates the output noise.
Regarding the CMFB bridge structure, we use antiparallel transistors to replace the resistor. This structure creates a large enough resistor to avoid additional power consumption in the bridge.

We apply a rphpoly resistor between the gate and source terminals of the reference transistor. As rphpoly uses polysilicon to build the resistor, it has the same temperature coefficient as transistors. When temperature changes, some parameters vary considerably. However, as long as they change proportionally, the reference current keeps its value. This design guarantees the robustness of the reference current.

![Figure 4.4 Layout for the whole readout circuit](image)

The layout for the whole readout circuit is shown in Figure 4.4. All the parts of the readout circuit, including amplifiers, clock generator, current source, low-pass filter, are integrated into one layout.

Next, we do a post-layout simulation for the circuit. The difference between pre-layout and post-layout is that pre-layout simulation only according to the schematic of the
circuit. In contrast, post-layout simulation combines the schematic and layout to simulate the result. So post-layout simulation result is more precise and close to the measurement result.

The transient post-layout simulation is shown in Figure 4.5. From the result, the circuit still shows pretty good linearity. However, the chopping ripple still exists. Regarding the difference between the pre-layout simulation result and post-layout simulation result, we put two curves in Figure 4.6.
Both of the two curves are about full-range input (600fF), and the output range is almost 2.7V. The difference between them is only 7.9571mV which is only 0.295% of 2.7V. So this difference is acceptable.

The linearity of the result is shown in Figure 4.7.
The post-layout simulation result’s sensitivity is 4.41 \( V/pF \). The theoretical result is:

\[
\frac{V_{\text{out}}}{\Delta C_s} = \frac{2}{2.4pF} \cdot \frac{1.8pF}{600fF} \cdot 1.8V = 4.5V/pF
\] (4.1)

There is little difference between the theoretical result and the simulation result. The sensitivity degeneration is mainly because of the charge sharing between circuit capacitance and parasitic capacitance. However, as the linearity is pretty good, we could modify the gain of the amplifier to compensate for the degeneration. For the post-layout noise simulation, its result is shown in Figure 4.8 and Table 4.1.
Figure 4.8 Post-layout noise simulation result of CHS

The output noise when input is zero at 200Hz is 80.77$nV/\sqrt{Hz}$, so the equivalent zero input capacitance noise is 17.95$zF/\sqrt{Hz}$. This value is slightly larger than the pre-layout simulation result but still keeps at a pretty low level.
Table 4.1 Output noise of post-layout simulation

<table>
<thead>
<tr>
<th>Delta C (fF)</th>
<th>Output noise ((nV/\sqrt{Hz}))</th>
<th>Delta C (fF)</th>
<th>Output noise ((nV/\sqrt{Hz}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>-600</td>
<td>83.55574</td>
<td>50</td>
<td>84.34587</td>
</tr>
<tr>
<td>-550</td>
<td>81.48791</td>
<td>100</td>
<td>88.33571</td>
</tr>
<tr>
<td>-500</td>
<td>81.00173</td>
<td>150</td>
<td>81.14801</td>
</tr>
<tr>
<td>-450</td>
<td>80.55873</td>
<td>200</td>
<td>94.32661</td>
</tr>
<tr>
<td>-400</td>
<td>80.19137</td>
<td>250</td>
<td>82.5175</td>
</tr>
<tr>
<td>-350</td>
<td>79.8731</td>
<td>300</td>
<td>79.75863</td>
</tr>
<tr>
<td>-300</td>
<td>79.73953</td>
<td>350</td>
<td>79.90737</td>
</tr>
<tr>
<td>-250</td>
<td>81.82486</td>
<td>400</td>
<td>80.18121</td>
</tr>
<tr>
<td>-200</td>
<td>82.95541</td>
<td>450</td>
<td>80.70174</td>
</tr>
<tr>
<td>-150</td>
<td>81.77583</td>
<td>500</td>
<td>81.49727</td>
</tr>
<tr>
<td>-100</td>
<td>89.84634</td>
<td>550</td>
<td>81.67879</td>
</tr>
<tr>
<td>-50</td>
<td>84.49941</td>
<td>600</td>
<td>85.32989</td>
</tr>
<tr>
<td>0</td>
<td>80.77262</td>
<td>Ave</td>
<td>82.71245</td>
</tr>
</tbody>
</table>

4.2 Fabrication

The readout circuit is implemented in the TSMC 180 nm CMOS process. TSMC (Taiwan Semiconductor Manufacturing Company) is the world’s leading CMOS foundry and offers a mature 180 nm manufacturing technology.

180 nm is called the “feature size”, which stands for the minimum channel length of the transistors. The TSMC 180 nm CMOS process has a 1.8V/5V design rule and offers six layers of metal for connection. We use the Muse semiconductor company Multi-Project Wafer (MPW) service to fabricate our circuit this time. The package integration we use is shown in Figure 4.9.
Figure 4.9 Package integration of MEMS accelerometer.

The MEMS sensor and readout circuit chip are wire-bonded in a 116 LCC package. The size of the package is 32mm*32mm. The layout of the PCB is shown in Figure 4.10.

![Figure 4.10 PCB layout of the package and ADC.](image)

When doing the measurement, a PCB is fabricated to integrate all the components on it. The connector like BNC and SMA guarantee the precision of the signal.
Chapter 5  Conclusions and Future Works

5.1 Thesis Contribution

Overall, in this thesis, we discussed the most widely used three techniques for the low-noise readout circuits. They are Auto-Zero (AZ), Correlated Double Sampling (CDS), and Chopper stabilization (CHS). We applied three different techniques to design three different readout circuits. After that, we did pre-layout simulations for all of them. By comparing the simulation results of these designs, we found out that CHS is preferred to AZ and CDS as it has the best noise characteristic. CHS moves the noise to a higher frequency using modulation and demodulation techniques. Then it reduces and eliminates the noise by a low-pass filter. Therefore, the best low-frequency noise characteristic is obtained. At the working frequency of about 200Hz, CHS could achieve a much lower level noise floor. So we choose CHS as our design to be optimized and fabricated.

Next, parameter optimization is applied to the design. With different input range and output range, different sensing capacitance $C_s$ and $C_{int}$ (integration capacitance) and $C_a$, $C_b$ (calculate capacitances) are used to get the best noise floor.

After the post-layout simulation, we get the zero input equivalent capacitance noise of $17.95 zF/\sqrt{Hz}$. It is an ultra-low noise level. Compared to recently published results [25], our design gets lower noise value and consumes less power.

After that, we do layout and post-layout simulation for the circuit and will fabricate in a standard 0.18 $\mu m$ CMOS process.
This readout circuit could combine with the MEMS sensor to make up an accelerometer. Its high-precision and low-noise characteristics could be used in various high-accuracy applications such as petroleum detection.

5.2 Future Work

The work presented in this thesis is about design and fabrication. The future work still including package, wire-bonding, PCB design, and measurement.

The accelerometer design can still be improved to obtain better performance. These improvement directions include:

- Applying some mixed techniques and other techniques (dual-chopper, ripple elimination, and so on) could further improve the noise characteristic.
- Consider more parameters, increase the matching degree between the sensor and the readout circuit, and find the optimal parameters.
- Optimize the amplifiers and low-pass filter structure to achieve lower power consumption and better noise.
- Use the closed-loop accelerometer structure is to correct the displacement error, improve the sensitivity, and then reduce the equivalent input noise.
- Monolithically integrate sensor, readout circuit, analog-to-digital converter, digital signal processing module, improve circuit performance, while reducing package volume
REFERENCE


