

COMMENT



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Yield, variability, reliability, and stability of two-dimensional materials based solid-state electronic devices

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The importance of statistical analyses on 2D materials-based electronic devices and circuits is sometimes overlooked. Here the authors discuss the most pressing integration issues for such devices and emphasize the need for yield, variability, reliability, and stability benchmarking, and outline viable strategies resulting in research papers that are useful for the industry.

Taking advantage of the outstanding properties of two-dimensional (2D) materials to fabricate advanced solid-state electronic devices *beyond* the complementary metal oxide semiconductor technology is an attractive approach that may provide a solution to extend Moore's law^{1,2}. A plethora of studies have reported the fabrication of 2D materials-based electronic devices with excellent performance, such as field effect transistors (FETs) that exhibit current on/off ratios $>10^9$ and subthreshold swing (SS) ~ 62 mV/decade³, photodetectors with high form factor and modulation bandwidths for communication beyond 180 Gb/s⁴, and memristors with excellent flexibility, transparency, and thermal stability^{5,6}. In order to provide useful technological knowledge, research papers in the field of 2D nano/micro-electronics should satisfy four requirements: (i) all methods used for the synthesis of the materials and the fabrication of the devices must be scalable to wafer level (i.e. mechanical exfoliation of bulk crystals should be avoided), (ii) the morphology and density of non-idealities in the 2D materials used (e.g. thickness fluctuations, lattice distortions) should be clearly specified and statistically demonstrated, (iii) the size of the devices must be small enough to be compatible with the integration density requirements of the target technology (in general, for exploratory studies, lateral sizes <100 nm are recommended), and (iv) information about yield, device-to-device variability, reliability, and stability (including descriptions of the main failure mechanisms for each type of device) must be provided. Within the available literature, still few reports adopted these methods and provide such information.

The year 2019 marked the achievement of important milestones towards the wafer-scale production of 2D materials-based microelectronic devices, which overcame critical difficulties on material synthesis and device patterning. Taiwan Semiconductor Manufacturing Company demonstrated the fabrication of p-type FETs with 6-layer-thick and 40 nm-long WS₂ channels that exhibit 10⁶ on/off current ratio, SS of ~ 97 mV/decade, and nearly zero drain-induced barrier

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lowering⁷. IMEC developed n-type FETs with ~3-layer-thick MoS₂, with 29 nm channel length and 13 nm contact length, and achieved an on-state current of ~250 $\mu\text{A}/\mu\text{m}$ and an excellent SS = 80 mV/decade using 50 nm SiO₂ and 4 nm HfO₂ as back-gate dielectric, respectively⁸. Ref. ⁸ presents a variability study of the SS, threshold voltage (V_T) and contact resistance (R_C) for hundreds of devices, which allowed the authors to design a detailed strategy for future optimizations. Similar studies were carried earlier in academia⁹ but not in such small devices. As it is expected that many other papers in this direction will follow in the next years^{1,2,10,11}, here we discuss the status and prospects of the yield, variability, reliability, and stability of solid-state microelectronic devices (mainly FETs and memristors) made of layered 2D materials.

Yield and device-to-device variability

Device yield is defined as the percentage of devices that work properly, according to specifications and within tolerance windows, among the total number of devices measured, and it is an essential magnitude to evaluate the quality of the fabrication process and the maturity of an integrated device¹². The device-to-device variability is defined as the deviation of the main chosen parameters and figures of merit of the devices, such as carriers' mobility, gate oxide leakage current, subthreshold swing, and threshold voltage in FETs, form factor and modulation bandwidths in photodetectors, and switching voltages and state resistances in memristors. A detailed list of parameters and their target values for each device and its applications can be found in the last updated version of the International Roadmap of Devices and Systems (IRDS)¹³. The device-to-device variability is normally evaluated by calculating the coefficient of variance (C_V), which can be calculated as the standard deviation divided by the mean value¹⁴. Both yield and device-to-device variability are related to the introduction of different types and amounts of defects during the fabrication process of the devices, including material synthesis, aging during storage, transfer process, patterning steps, and deposition of other materials (e.g. contacts). In the case of 2D materials-based devices, the most common intrinsic defects are vacancies, impurities, atomic misalignments, strained bonding, impurities, cracks, wrinkles, and thickness fluctuations in the 2D sheet, while the most common extrinsic defects are related to the changing interaction with the environment resulting in variable adhesion and interaction with the adjacent materials. When the influence of the defects introduced is small, it can modify the characteristics of the devices, resulting in an increase of the device-to-device variability but within an accepted window of operation. However, if the influence of the defects introduced is too large, then the device may fail to perform the actions required, resulting in a decrease of the yield.

Ref. ⁹ fabricated and measured hundreds of back-gate MoS₂ FETs, spread over an area >1 cm², with channel widths (W) of $11.74 \pm 0.13 \mu\text{m}$, channel lengths (L) ranging between 4 μm and 9 μm , and channel thicknesses mainly monolayer with few bilayer islands ($\leq 0.5 \mu\text{m}^2$). The authors reported values of V_T of $-1.78 \pm 1.05 \text{ V}$, density of charge traps (n_t) of $(1.1 \pm 0.9) \times 10^{11} \text{ cm}^{-2}$, hysteresis (H) of $0.14 \pm 0.07 \text{ V}$, current max/min ratio ($\log_{10}[I_{\text{MAX}}/I_{\text{MIN}}]$) of 6.68 ± 0.40 , and carriers' mobility (μ) of $34.2 \pm 3.6 \text{ cm}^2/\text{V/s}$ (see Fig. 1). This statistical evaluation of the key parameters gives a good view on the potential material performance, and in parallel it highlights the parameters which are the most sensitive to variability and which will require attention in device tuning for stable circuitry. Ref. ⁹ indicated that ultra-low MoS₂ roughness after fabrication (~0.3 nm), the use of planar Ag/Au contact electrodes, and the use of ultra-clean environment are essential to achieve such low

variability. It was also reported that, for the back-gate FETs configuration of those sizes, the presence of bilayer islands in the MoS₂ channel does not increase the variability of these parameters. In ref. ⁸, 60° twin boundaries were identified as the main type of dislocation present in the MoS₂ channels grown by chemical vapour deposition (CVD), but the impact of individual dislocations and bilayer islands on electrical performance of individual nanoscale devices could not yet be established. However, the large amount of data collected allowed the authors to discern that the standard deviation of V_T increases with narrower W but not with shorter L , suggesting that the Schottky contacts are responsible for V_T variability. Following up on this statistical approach, ref. ¹⁵ not only fabricated MoS₂ FETs at the wafer level (using liquid phase exfoliation) with reasonably stable μ but also used the devices to construct logic gates. However, the main drawback of that work is that the size of the devices is too large ($L \sim 100 \mu\text{m}$). Recently, ref. ¹⁶ reported the fabrication of operational amplifiers using MoS₂ FETs with channel lengths down to few micrometers (i.e. the smallest FET used has $W = 5 \mu\text{m}$ and $L = 10 \mu\text{m}$) and presented transfer characteristics with a low device-to-device variability. Additional effort and focus will be required for high-density electronic circuits made of 2D materials-based FETs with nanoscale dimensions and integrated through state-of-the-art wafer-level processes.

In the field of memristors, the effect of materials defects on the variability is different, as the current does not flow along the 2D material but across it. In such vertical devices, the resistive switching (RS) is a stochastic phenomenon that always takes place at the electrically weakest location of the active area of the device under electrical field. In this context, the presence of cracks in the 2D materials reduce the physical thickness and therefore promote RS at that specific location¹⁷ (i.e. reduce the switching voltage). Lattice distortions and dopants normally act as trapping sites, facilitating out-of-plane charge transfer and generation of additional defects, which also tend to promote RS and reduce the forming—and switching voltages¹⁸. On the contrary, wrinkles and polymer residues from the transfer are insulating and increase the out-of-plane resistance, meaning that RS will never take place at those sites¹⁹; this merely represents a reduction of the effective area of the memristors and it has no remarkable effect in their variability if the samples are relatively clean (i.e. <50 nm² of contaminants per μm^2). In the field of 2D materials-based memristors, the information available about yield and device-to-device variability is so far scarce. Ref. ²⁰ claimed the fabrication of Ag/SnO_x/SnSe memristors with a yield of 100% (out of 80 devices) and presented statistics for the set and reset voltages (V_{SET} and V_{RESET} , respectively). However, the window of operation defining the device yield-pass criteria is expected to be narrower in industrial memristive circuits, and therefore the circuit yield would drop substantially. Refs. ^{21,22} also presented variability information of the switching voltages for few (<10) devices. So far, the most complete report in this direction is the one in ref. ²³, which analysed hundreds of Au/hexagonal boron nitride (h-BN)/Au memristors and reported yield >98% and device-to-device variability of switching voltages comparable (if not smaller) to that of metal/oxide-based memristors fabricated at industrial facilities²⁴, i.e. C_V of $V_{\text{SET}} \sim 5.74\%$. Ref. ²³ also reported that the variability of the currents in high resistive state (HRS) and low resistive state (LRS) is low enough to ensure 100% state recognition in >1500 cycles measured in 48 devices, even at low LRS currents <500 nA (which are highly desirable to reduce sneak path currents and power consumption). These statistical demonstrations have helped to clarify the real potential of h-BN for memristive technologies, and conducting similar analyses in memristors made of other 2D materials is highly recommended.

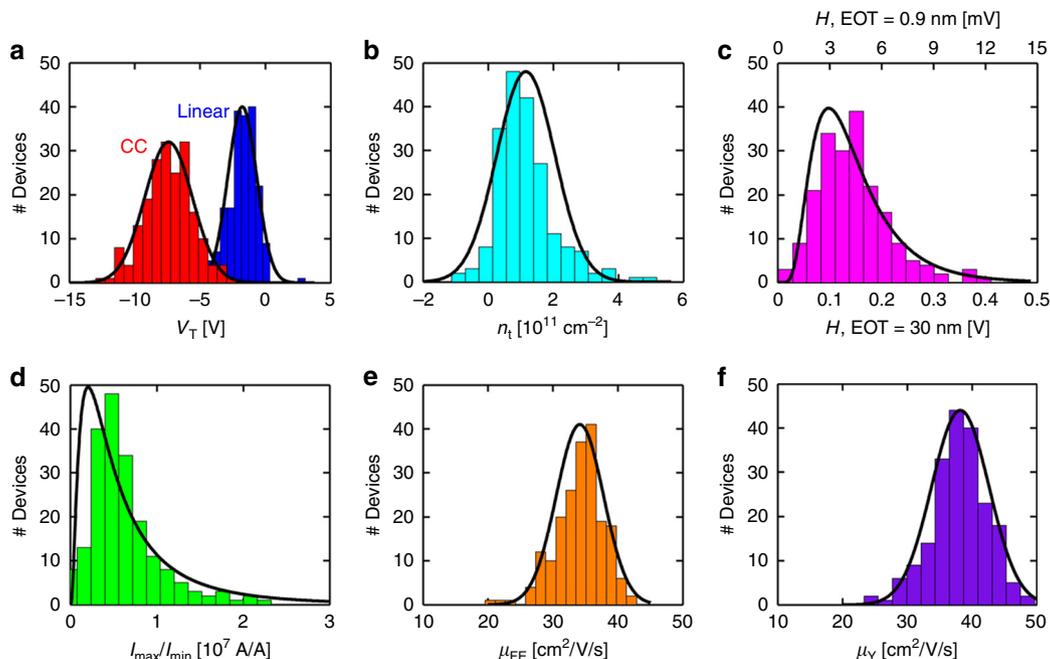


Fig. 1 Example of an outstanding variability analysis of multiple parameters of hundreds of MoS₂ FETs, which furthermore are grown using a scalable method (i.e. CVD). **a** shows the value of V_{TH} for both the linear extrapolation (blue) and constant-current (red) methods, **b** shows the value of n_t , **c** the value of the hysteresis, **d** the I_{MAX}/I_{MIN} ratio, and **e**, **f** the values of the mobility extracted from the field-effect approach and the Y-function approach (respectively). Reproduced with permission from ref. ⁹ Copyright American Chemical Society, 2017.

Reliability and stability. In the field of 2D materials-based microelectronic devices, reliability is defined as the time that one electronic device can continuously operate in a predefined operation window. This is determined by the device degradation and failure due to the application of stresses during operation, which can be electrical, mechanical, thermal, chemical, and magnetic²⁵. Stability refers to the degradation of the properties of the devices with time, unrelated to operational stresses, but instead by contamination produced by e.g. the relative humidity of the environment and/or atomic diffusion. Note that, under this definition, concepts like thermal stability are included in the term reliability, as it only applies to the devices under operation. Both reliability and stability could be understood as a time-dependent variability, and therefore the failure strongly depends on the window (i.e. criteria) set for each device, circuit, and/or application.

The failure of a microelectronic circuit can have its origin within a device (i.e. front-end of line), at the interconnections between them (i.e. back-end of line), or at the materials used during encapsulation (i.e. packaging)²⁵. While studying packaging issues may not be responsibility of academics, dealing with front-end and back-end failure mechanisms should be a priority; however, so far very few authors made remarkable efforts in this direction. Ref. ²⁶ analysed the stress-induced leakage current and time-dependent dielectric breakdown in h-BN dielectric stacks using both conductive atomic force microscopy and device-level stresses and concluded that the failure is triggered by the generation of boron vacancies. Refs. ^{27,28} reported that charge trapping and de-trapping in the dielectrics of FETs with MoS₂ channels increases the hysteresis and negative bias temperature instability and that these problems can be reduced using 2D layered or crystalline self-passivated materials (such as h-BN and CaF₂, respectively). Ref. ²⁹ reported that trilayer graphene barrier stacks prevent Cu diffusion much better than ~3 nm TaN films (which is the industrial standard) and that it could represent a very useful strategy to reduce R_C and improve the reliability of

back-end of line interconnections in microelectronic circuits. Regarding stability, some 2D materials like black phosphorous and silicene (among others) have shown rapid degradation when exposed to air environment, which emphasizes the need to monitor the electrical properties of the devices over storage time. In ref. ³⁰, the authors observed that black phosphorous FETs could keep their performance for >17 months using a 25-nm-thick Al₂O₃ capping layer, and this strategy also remarkably increased the stability of silicene-based FETs³¹.

In the field of memristors, the concept of reliability is linked to cycle-to-cycle variability of the electrical characteristics. Some figures of merit, such as the endurance and the retention plots can give some idea about how the values of the resistance in HRS and LRS evolve with the number of cycles and time (respectively)¹⁷, but other parameters such as the switching time and energy have not been analysed depending on the number of cycles. Moreover, the stability of 2D materials-based memristors has been only partially analysed³², and more studies in this direction are necessary.

It should be highlighted that the degradation of 2D materials-based microelectronic devices is considerably connected with energy dissipation during device operation. In FETs, non-equilibrium charge carriers flowing in-plane at the channel region can undergo energy relaxation either with the lattice of the 2D material or with the adjacent layers (i.e. substrate, gate dielectric, electrodes), which makes necessary investigating multiple physical phenomena, such as thermal radiation from hot electrons, electron-electron scattering, scattering with optical phonons in the substrate and/or dielectric, thermal decoupling of hot electrons from acoustic phonons, electron-hole recombination, and Peltier effect³³. These phenomena are strongly related to the thermal conductance of the 2D materials, and while it has been widely demonstrated that their high in-plane thermal conductivities (provided by covalent bonds) enhance the performance of the FETs³⁴, inefficient heat transfer out of plane (due to van der Waals gap) and towards adjacent materials

(due to disordered bonding) may remarkably decrease the reliability of the devices³⁵. In memristors, the out-of-plane current requires the formation of local defects in the lattice of the 2D layered dielectric, and the chemical stability of the materials and energy for defect formation (either intrinsic vacancies or metallic ion penetration) as the electrical stress proceeds play a more important role^{17,36}. For both types of devices, additional investigations linking energy dissipation phenomena with device reliability and lifetime are highly necessary.

Discussion

Fabricating nanoscale devices made of 2D materials to wafer level using scalable methods while achieving excellent performance is a significant challenge even for the most advanced companies. The performance metrics reported for devices with synthetic materials are still severely degraded compared to devices with mechanical exfoliation. As an example, in 2010 an h-BN encapsulated graphene FET was fabricated via mechanical exfoliation, and a carriers' mobility of 60,000 cm²/V/s was observed³⁷; the same experiment was repeated 8 years later using CVD-grown graphene and h-BN³⁸, and the average mobility observed was only 2500 cm²/V/s. While research on mechanically exfoliated 2D materials may still be relevant as reference to evaluate materials performance, there is an urgent need for statistical investigations dealing with integration issues of 2D materials-based microelectronic devices and circuits, the up-scalability of the methods, and targeting industry-standard performance metrics. In this regard, it is worth noting that the parameters and figures of merit of each device depend on the application. As an example, the FETs used in logic gates need to show performances and fit reliability criteria different to those used (for example) to control the current across a memristor. Similarly, memristors used as non-volatile memory and memristors used as electronic synapses need to exhibit different performances. For this reason, it may not be straightforward to provide exact values herein; a complete list of parameters and their target values for different applications can be found in last updated edition of the IRDS¹³. While extended guidelines on how to evaluate the yield, reliability, variability, and stability of transistors^{39,40} and memristors^{17,41} can be found in the literature, some general criteria include: (i) fabricating and characterizing multiple devices, (ii) presenting statistical information of all the parameters and figures of merit determining the reliability of the devices, and (iii) analysing and discussing the failure mechanisms based on experimental measurements with nanometric (if not atomic) resolution, avoiding to only rely on schematics based on intuition. The importance of statistical analyses on 2D devices needs to be emphasized on a broader level in order to enable a technological shift, particularly because critical integration issues risk to be overlooked in academic publications.

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Author contributions

All the authors wrote the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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