A NANOELECTROMECHANICAL RESONATOR-BASED FLASH STYLE ANALOG TO DIGITAL CONVERTER

Xuecui Zou[1], Sally Ahmed[1], Syed Kazmi[3], Pedro Da Costa[2], Mohammad Younis[2], and Hossein Fariborzi[1]

[1]CEMSE Division, King Abdullah University of Science and Technology, Thuwal, Saudi Arabia
[2]PSE Division, King Abdullah University of Science and Technology, Thuwal, Saudi Arabia
[3]Netherlands Institute for Space Research, Groningen, the Netherland

ABSTRACT

In this work, the design of a flash-style nanoelectromechanical resonator-based analog to digital converter (ADC) is presented. The operation of the proposed ADC depends on tuning the beam resonance frequency by the sampled voltage, using the electrostatic softening effect. In this paper, experimental results are demonstrated for a 3-bit ADC. The proposed solution reduces design complexity by 20 times and reduces energy consumption by one order of magnitude compared to conventional complementary metal-oxide-semiconductor (CMOS) counterpart. While the measured sampling rate is 8 kS/s, resonators with GHz resonance frequency can increase the sampling rate to MHz and above, making this technology a viable option for medium speed, ultra-low power IoT and sensor applications.

KEYWORDS

Analog to digital converters (ADC); flash ADC; NEM resonator; electrostatic softening effect, low power design.

INTRODUCTION

The high power density of complementary-metal-oxide-semiconductor (CMOS) chips caused by the continuous scaling of this technology has encouraged researchers to look for alternative low-power technologies for implementing digital circuits. In particular, the interest in mechanical computing and digital logic design using NEM relays and resonators has increased significantly due to their ultra-low power consumption compared to their CMOS counterparts. Although the speed of such electromechanical devices is not comparable to CMOS, they are useful for applications that require low-to-moderate speeds and ultra-low power consumption, such as the internet of things (IoT) devices [1]. The main advantage of using resonators is that their operation does not involve physical contact, which makes them more reliable and wear-free compared to contact-based devices such as relays which suffer from wearing and high contact resistance [2]. MEM and NEM resonator-based logic gates and memory devices have been demonstrated using different techniques such as frequency mixing [3], activation and deactivation of vibration modes [4, 5] and resonance frequency tuning using electro-thermal current [6, 7]or DC voltages[8, 9]. In addition to the simple logic and memory elements, more complicated circuits, such as full adders, was demonstrated recently using MEMS resonators [10, 11], which requires fewer devices than conventional CMOS full adder. In order to build full systems based on resonators, interface circuits between sensors/actuators and the core blocks are required. In previous work, a MEMS resonator-based digital-to-analog (DAC) converter was demonstrated [12]. In this work, we complement the interface circuits and present a novel design of a NEM resonator-based ADC. This paper is organized as follows. It starts by explaining the design and operation of the proposed ADC followed by the fabrication process and the experimental results for a 3-bit ADC. The last part discusses some important parameters of the ADC such as system complexity, sampling speed, and energy consumption.

DEVICE OPERATION AND CIRCUIT ARCHITECTURE

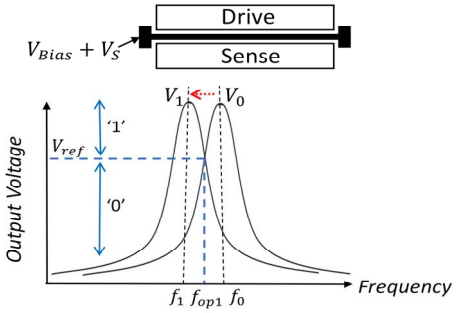
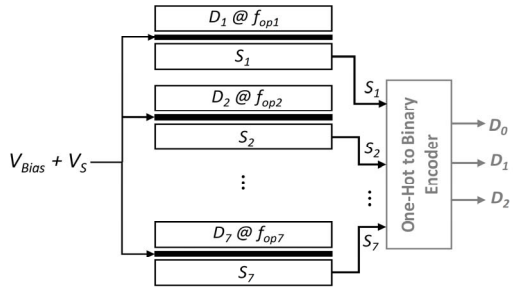


Figure 1. A 2D schematic of the resonator is shown where the sampled input V_S is added to the beam bias V_{Bias}. By fixing the frequency of the drive signal to f_{op1}, if the sampled voltage is between V_0 and V_1, the output voltage will be greater than V_{Ref} and a digital '1' is produced, otherwise, the output will be $<V_{Ref}$ which results in digital '0' output.

The proposed NEM resonator-based ADC design is similar to CMOS flash ADC design in its parallel operation [13]. For an n-bit ADC, 2^n-1 resonators, operating at different frequencies, are required. These resonators will generate a one-hot code that represents the input (only one resonator produces a digital '1' while the rest produce digital '0's). The sampled voltage V_S is applied to all resonators in parallel. Ideally, all resonators should be identical in structure and natural resonance frequency. Practically, it might be very hard to obtain identical resonators due to fabrication imperfections and residual stresses. However, the resonance frequencies can be made identical by applying different voltage biases on the different beams. Each resonator consists of an in-plane clamped-clamped nano-beam, and one electrode on each side of the beam as shown in Figure 1. All beams are biased with a DC voltage (V_{Bias}). An AC signal is applied to the drive electrode to electrostatically actuate the beam. If the frequency of the applied signal is sufficiently close to the resonance frequency, the beam resonates, and a relatively high motional current is detected at the sense electrode. The sampled voltage signal (V_S) is added to the beam bias which

results in a shift in the resonance frequency of the beam due to the electrostatic softening effect.

In order to describe the operation, we will consider a 3-bit ADC as an example. Let's assume that the sampled voltage V_S (the input) can take any value between two different voltages V_0 and V_7. Since the output is represented by 7 bits generated by 7 resonators, the voltage range ($V_7 - V_0$) is divided into seven segments as follows: $V_0 \rightarrow V_1$, $V_1 \rightarrow V_2$, $V_2 \rightarrow V_3$, $V_3 \rightarrow V_4$, $V_4 \rightarrow V_5$, $V_5 \rightarrow V_6$, and $V_6 \rightarrow V_7$. Each resonator will be assigned one voltage segment and will produce a digital '1' only if the sampled voltage V_S lies within its assigned range. These different voltage range assignments are realized by the proper choice of the drive signal frequency for each resonator. To determine the frequency of operation for each resonator, we will consider the first resonator which is assigned the first range $V_0 \rightarrow V_1$. As shown in Figure 1, if the sampled voltage V_S equals V_0, the corresponding resonance frequency for all beams is f_0. When V_S increases to V_1, the resonance frequency decreases and shifts to f_1. By fixing the drive signal frequency of the first resonator only to f_{op1}, which is defined in Figure 1 as the intersection between the resonance peaks resulting from V_0 and V_1, the output is digital '1' only if V_S lies between V_0 and V_1, otherwise, the output is '0'. Note that the output voltage amplitude at f_{op1} is considered the reference voltage V_{ref} that defines the threshold between the digital '1' and the digital '0' output regions for all resonators.



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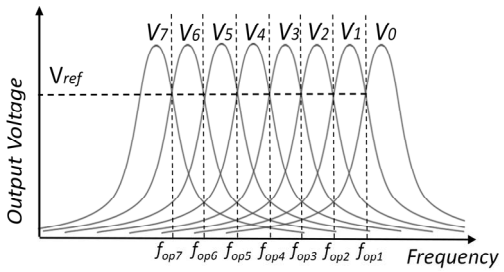


(b)

Figure 2. (a) System architecture of a 3-bit resonator-based flash ADC, where the sampled input V_S is applied to all the resonators in parallel. The resonators' outputs S_1 to S_7 can then be converted to a binary code using an encoder. (b) A general plot for the frequency response for different sampled voltage values and frequencies of operation for the different resonators.

Figure 2 (a) shows the system architecture of a 3-bit resonator-based ADC. Figure 2 (b) shows the general shape of the frequency response for different ranges of the sampled input. The resonators should work in the linear regime to make use of the symmetry of each peak. Implementing the 3-bit ADC requires seven resonators (D_1 to D_7), operating at seven different frequencies (f_{op1} to f_{op7}). A one-hot code (S_1-S_7) is generated by these resonators depending on the value of V_S as illustrated earlier. For example, if ($V_5 < V_S < V_6$), only the output S_6 will be '1' while the rest of the outputs will be '0's. The output vector can then be converted into a 3-bit binary code using a one-hot to binary encoder.

FABRICATION PROCESS

The nano-resonator is fabricated using a <100>, heavily boron-doped silicon on insulator (SOI) wafer. The device layer thickness is around 1.85 µm, while the oxide thickness is 1 µm. The fabrication process is illustrated in Figure 3. It starts with cleaning the wafer and spinning a positive photoresist (950 PMMA A4) with a thickness of 210 nm on the wafer. Electron beam lithography (EBL) is then used to define the device pattern. After exposure, the wafer is immersed in a solution of (MIBK: IPA) with a (1: 3) ratio for 90s to develop the exposed resist. The silicon device layer is then etched to define the beam and the electrodes using reactive ion etching (RIE) with alternate cycles of C_4F_8 and SF_6 gases. Finally, the remaining resist is stripped off, and the sacrificial oxide layer is etched using HF vapor for 25 min.

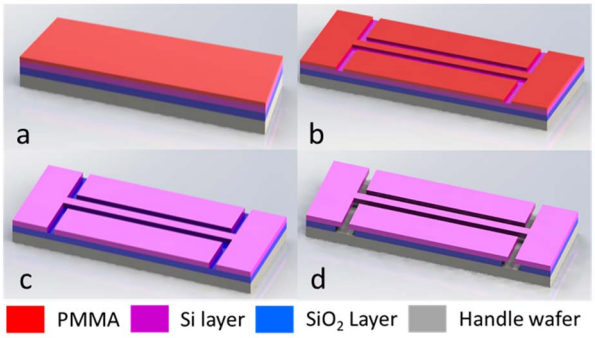


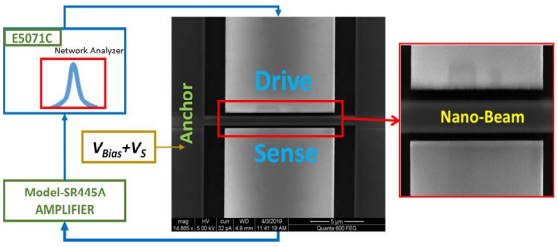
Figure 3. The fabrication process steps for the nano-beam resonators: (a) resist spinning on SOI wafer, (b) resist patterning using electron beam lithography (EBL), (c) silicon anisotropic etching and photoresist removal, and (d) beam release using a timed HF vapor etching.

RESULTS

Figure 4(a) shows a scanning electron microscopy (SEM) image of the fabricated device with its dimensions and the experimental set-up. The device is tested in a vacuum chamber at 6.8e-5 mbar and at room temperature. A network analyzer is used to supply an AC signal to the resonator and sense its output after passing through an amplifier. The beam is biased with 48.5V. The results demonstrated here are for a 3-bit ADC. The sampled input takes values between 0 and 3.5V. The results are obtained in two steps. First, frequency responses are measured and plotted together for different values of the sampled input starting from 0 to 3.5V with a step of 0.5V. Next, the seven frequencies of operation are determined from the plot and time response is measured by fixing the drive signal frequency for each resonator to the obtained frequencies of operation.

Frequency Response

To determine the frequency of operation of each resonator, frequency responses for the following values of the sampled input are measured (from 0 to 3.5V with a step of 0.5V) as shown in Figure 4(b). As mentioned earlier, for a 3-bit ADC, 7 resonators, operating at different frequencies, are required. The frequencies of operation f_{op1}-f_{op7} are determined by the intersections of the frequency responses which are marked by the black circles in Figure 4 (b). The voltage difference between two consecutive peaks, which is 0.5V in this case, is chosen such that the intersection of these peaks happens at -3dB from the maximum S_{21} value, thereby defining the reference voltage above which the resonator produces a logic '1' output.



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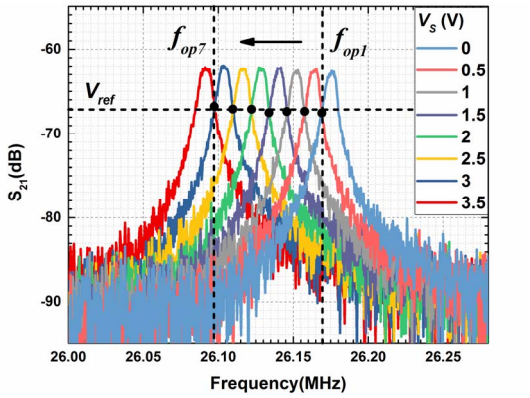
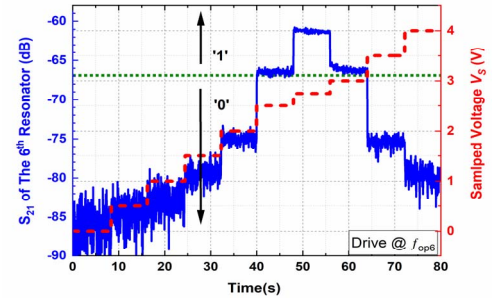


(b)

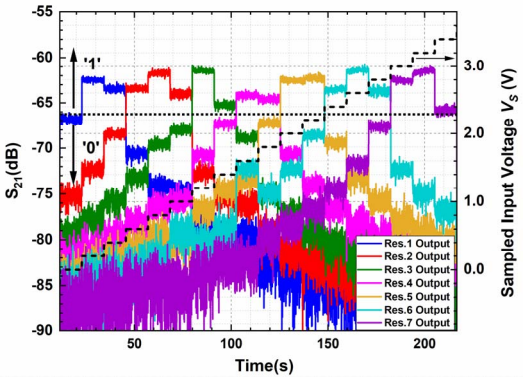
Figure 4. (a) A scanning electron microscopy (SEM) image of the fabricated device showing the experimental set-up. The nano-beam is 15 µm long, 750 nm wide, and 1.85 µm thick. The air gap between the beam and the side electrodes is approximately 250 nm. (b) Frequency responses of the resonator for different values of the sampled input voltage V_S.

Time Response

After identifying the frequencies of operation for each resonator in the previous step, time response is measured by fixing the frequency of the drive signal to the frequency of interest and varying the sampled voltage in steps of 0.5V and 0.2V. Among the 7 resonators, only one of them should produce a logic '1' output depending on the sampled input value. In Figure 5(a), the frequency of the drive signal is fixed at f_{op6}, and the output of that resonator is '1' when $2.5V < V_S < 3V$ as expected. If the sampled input does not lie in this range, a '0' output is detected. Similarly, by fixing the frequency of the drive signal for each resonator to the obtained frequencies in the previous step, the output of all resonators under different values of Vs is shown in Figure 5(b). When V_S (black dashed stair case in Figure 5 (b)) lies between 0V and 0.5V, only the first resonator generates a logic '1' at the output. When V_S increases, the first resonator turns off and the second turns on (red) and so on.



(a)



(b)

Figure 5. Time response showing (a) the output of the resonator S_6 (solid blue line) with its drive frequency fixed at f_{op6} for different values of V_S (dashed red line), and (b) the outputs of all 7 resonators when V_S is varied in 0.2V steps (the black dashed line).

DISCUSSION

Micro/nano resonator technology has become a very attractive alternative for circuit design for many reasons. In this part, some important aspects such as system complexity, sampling speed, and energy consumption are discussed.

One of the very attractive aspects of using micro/nano-resonators for digital circuit design is the reduced complexity of the required circuits [6, 9, 11]. This can be achieved by using resonator characteristics that do not exist in CMOS and developing a new design paradigm tailored for resonator-based circuits. This is different from merely replacing CMOS transistors with resonators, so a fair comparison between the two technologies must be done in the circuit and system level, rather than the device level. For the flash ADC design presented in this paper, only seven resonators are required to generate the one-hot code of a 3-bit ADC, which is 14-22 times less than the number of required transistors in CMOS counterparts [14-16].

Another important aspect is the sampling rate of the ADC. In general, the switching speed of resonators depends on the resonance frequency and the quality factor (f/Q) [17]. The measured resonance frequency of the current device is 26.14 MHz and the quality factor (Q) is 3227, which yields a sampling rate of 8kS/s. COMSOL simulations were done for a clamped-clamped 1.5 um long, 400 nm wide and 600 nm thick beam resonator, under 40V beam bias resulting in 1.142 GHz resonance frequency. Using a voltage step of 2V, the minimum required Q to guarantee proper separation of the peaks and correct operation of the ADC is around 3700, which results in a speed of 0.3 MS/s. The speed can

be further increased by more aggressive scaling, exploring new materials and decreasing the quality factor.

The energy consumed by the proposed 3-bit ADC is 177.9 fJ per conversion step. For the 4-bit and 5-bit versions of the proposed ADC, the energy per conversion step is 10 and 8 times smaller than CMOS counterparts in [15] and [14], respectively. Since the energy consumption of off-resonance devices is many orders lower than the active device, increasing the resolution (ADC bits) does not increase the total energy consumption considerably, so the energy efficiency benefits of the proposed design become more pronounced for larger ADCs. The N/MEMs ADC can be used in mobile platforms or some unattended ground sensor systems which operate at sample rates less than 1 MHz continuously for long periods of time and require ultra-low power consumption [1, 18].

CONCLUSION

In this paper, a novel idea for implementing a nano-resonator based flash-style ADC is presented and experimentally verified. The operation of the circuit is based on changing the resonance frequency of the resonator beam according to the sampled input. The proposed solution reduces the circuit complexity by at least one order of magnitude compared to CMOS based flash ADCs. The sampling rate of the tested device is around 8kS/s and can be further increased by aggressive downscaling and lowering *Q*. The characterized ADC consumes only 177.9 fJ/Conv.step, which makes it an appealing choice for sensor networks and IoT applications that require medium operation speed and ultra-low power consumption.

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CONTACT

*Xuecui Zou, xuecui.zou@kaust.edu.sa

*Hossein Fariborzi, hossein.fariborzi@kaust.edu.sa