Resonator-based M/NEMS Logic Devices: Review of Recent Advances

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Abstract

As transistors are reaching their fundamental limits in terms of power consumption, miniaturization, and heat generation, there is an imminent need to develop alternate computing technologies. One such an alternative is through micro/nanoelectromechanical systems (M/NEMS) that focuses on ultra-low energy consumption. Computing based on static MEMS switches has been proposed, however these suffer from reliability issues due to contact and stiction. Recently, logic devices based on electro mechanically excited vibrating structures, resonators, have emerged as a potential solution that overcomes these issues. This paper reviews the recent advancements of resonator-based M/NEMS logic devices. First, pioneering works in the field are surveyed. Then, logic devices based on frequency tuning are discussed. Next, cascadability of such logic devices is demonstrated. Finally, a discussion about the challenges of such technology and future prospects is presented.

1. Introduction

Transistors are reaching their fundamental limits in terms of size, energy consumption, and heat generation. Today, to keep up with Moore's law, there is an urgent need to shift the paradigms from conventional computing and to search for alternative computing technologies [1]. Among alternative technologies [2, 3], micro/nanoelectromechanical systems (M/NEMS) based logic and memory devices have been an active area of research over the past couple of decades. Some of the attractive features of such devices include ultra-low energy consumption due to their zero off-state leakage, reprogrammability of a single active unit to perform multiple logic operations, immunization to ionic radiations, and the potential to operate in harsh environment conditions [4-8].

Logic devices based on MEMS switches utilize a mechanical structure such as a micro/nano beam which is switched ON "1"and OFF "0" under various electrical input conditions to perform different logic operations [5, 17]. Electrostatically actuated NEMS cantilevers with a dual electrode configuration have been proposed for logic operations [7]. The study in [7] combines several units to perform fundamental logic gates such as NOR/XOR/NAND and an inverter. Similarly, a 3 stage ring oscillator comprising of single cells of curved cantilever nanobeams are utilized to perform a single stage inverter and a buffer [9]. Piezoelectric parallel dual beam relay design has been demonstrated to perform logic operations XOR, OR, AND, Half-Adder, Latch, and a 2-Stage Inverter at low (~1 V_{pp}) voltages [8]. In another study, body-biased aluminum nitride (AlN) piezoelectric MEMS switches are used as NOR and NAND logic gates [10]. Complementary MEMS switches that work in a see-saw manner have been popular architectures for such logic application due to multiple actuation and switching possibilities. A four terminal

relay technology uses the complementary motion of the switches to perform an inverter [11]. Using a similar technology, a seesaw-relay-based device has been used for logic and memory applications capable of executing the fundamental AND and OR gates [12]. Furthermore, torsional actuators, have been used to perform multiple logic operations using different electrical interconnect schemes [13-15]. The study in [15] experimentally demonstrates a universal logic device capable of performing all the fundamental logic operation using different electrical interconnects. Furthermore, piezotronic NEMS devices have been also demonstrated to perform high speed and low power logic and memory operations [16-19].

Despite having some major advantages such as cascadability and zero off-state leakage, M/NEMS switch based devices suffer from contact reliability and stiction issues [20-23]. This limits the practicality of such devices. One possible solution is capacitive adiabatic logic (CAL), which is a contactless logic operation that promises better reliability than M/NEMS switch-based logic devices [24-27]. The capacitive adiabatic logic approach relies on a smooth capacitive modulation to achieve quasi zero-power logic dissipation. A detailed analysis and comparison of NEMS and CMOS technologies for low power CAL logic implementation is presented [25]. It is predicted that for a low contact resistance and sub 1 V operation, the energy dissipation by a NEMS based CAL logic operation can potentially be an order of magnitude better than that of the CMOS technology. The study in [26] utilizes four terminal MEMS comb-drive devices for capacitive adiabatic logic. This theoretical investigation shows an energy dissipation of 1 pJ for a mm scale device. Similarly, logic gates AND, OR, XOR, and 1-bit full adder are theoretically demonstrated using a five-terminal comb-drive actuator [27]. Furthermore, cascadability of this technology is also established.

Another solution to contact reliability and stiction issues associated with M/NEMS switch-based devices is dynamic resonator-based M/NEMS logic devices. In this approach, an on(off)-resonance state of a resonator can be attributed to the 1(0) of the logic outputs. This manuscript will review the different technologies and advancements made in the area of dynamic resonator-based M/NEMS logic devices.

The rest of the paper is organized as follows. Section 2 explains the operating principle of resonator-based logic devices. Section 3 presents an overview of various techniques developed to realize various computing operations. Finally, Section 4 presents the conclusions.

2. Operating Principle

The operating principle of the resonator-based logic devices relies on the on-resonance and off-resonance state of a resonator. The on-resonance state, where the resonator vibrates with a significantly high amplitude, is attributed to the High (1) logic output, while the off-resonance state, where the resonator vibrates with low amplitude, is attributed to the Low (0) logic output, Figure 1. This transition from on-resonance to off-resonance can either be achieved by manipulating the input conditions, e.g., electrical interconnect configurations, manipulating an AC or DC input voltage, or by using a certain dynamic phenomenon, such as tuning resonance frequency, activation and deactivation of resonance modes, and utilizing the bistable regime in a nonlinear resonator. In the following sections different technologies and methodologies that have been used to achieve these logic devices will be reviewed.

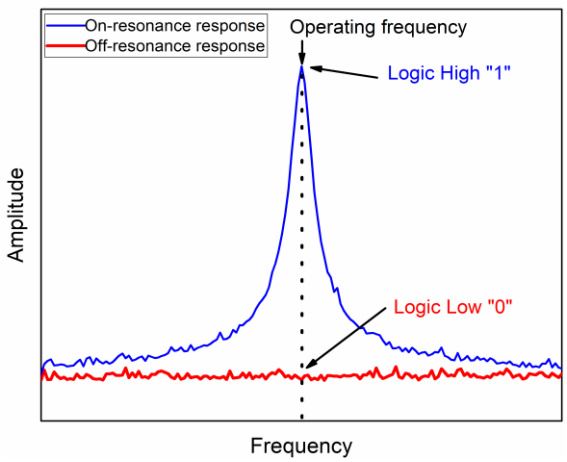

Figure 1. Schematic of an on-resonance and off-resonance resonator response. Choosing the resonance frequency as the operating point a High "1" logic output is achieved in the on-resonance state, while a Low "0" logic output is achieved in the off-resonance state.

3. Dynamic Resonator-based Logic Devices

The first resonator-based logic device was experimentally demonstrated in [28] using a piezoelectric NEMS actuator. The device consists of an L-shaped NEMS resonator, Figure 2. The device relies on the crystallographic anisotropy of the piezoelectric material to perform the XOR logic operation. When the device is driven from input A or B as shown in the Figure 2(A, C), the entire structure resonates around 10 MHz. It can be also observed from Figure 2(C) that inputs A and B result in equal magnitude but opposite phase due to the orthogonality of the crystallographic directions of the two halves of the L-shaped resonator. Therefore, when both inputs are applied, the response of the resonator is negligible as the motion of the two halves cancel each other, Figure 2(C).

In another seminal work, logic operations are realized by utilizing the bistable response of a resonator operating in the nonlinear regime [29]. Using a laterally actuated clamped-clamped beam resonator, the authors demonstrate a reprogrammable and re-configurable AND/NAND and OR/NOR logic devices. The resonator operates at one of the two stable vibration states that co-exist and an added power (input signal) can force the resonator to jump from one state to the other, e.g., off-resonance to on-resonance, and thereby performing the logic operation, Figure 3. Furthermore, the added noise power is used to avoid any uncertainty in executing the desired logic operations. The logic devices show an extremely low energy consumption of ~10^{-17} J per switching operation, while the maximum power consumption of the device is given by 0.3nW in the high-level state.

Since then, the bistable behavior of nonlinear resonators has been exploited further for several logic and memory devices [30-34]. The devices in [30, 31] utilize the bistability of a NEMS resonator and assign binary values to the two allowed states of the bistable region. The transition between the memory states is achieved by modulating the nonlinear resonance via DC bias. Similarly, the devices in [32, 33] utilize the bistable regime of a nonlinear resonator and further add a closed loop control to realize memory and logic operation. The authors also examine the nonlinear dynamics with and without the control input. They also further extend the principle and utilize the two coupled comb drive actuators of [32, 33] to realize a 2-bit binary counter [34].

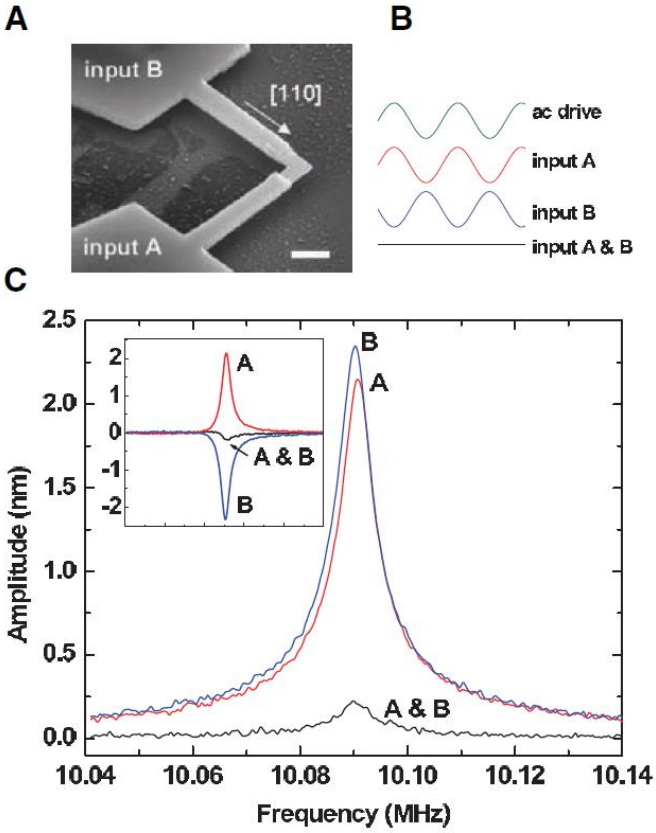

Figure 2. Experimental demonstration of an XOR logic gate. (A) L-shaped cantilever with electrically isolated but mechanically connected inputs. Scale bar, 1 mm. (B) Measured frequency response to a 5mV AC driving signal applied to the inputs: A not B, red; B not A, blue; and A and B, black. (C) Schematic illustration of the mechanical XOR logic gate's operational principle, exploiting piezoelectric anisotropy. When an AC drive was applied across only one of the inputs, the device responded with equal mechanical amplitude but opposite phase (the "on" state). This resulted in an effective cancellation of motion ("off" state) when the drive was simultaneously applied to the two inputs. (Inset) The real component of the response signal, indicating the 180° phase shift between the response due to driving at input A and that due to driving at input B. Re-printed with permission [28].

Another significant contribution is the experimental demonstration of a reversible Fredkin logic gate [35]. This is achieved using a NEMS architecture comprising of four clamped-clamped nanobeams electrically interconnected together, Figure 4, to realize a universal logic gate capable of performing any reversible computation. AND, OR, NOT, and FANOUT gates are experimentally demonstrated. The authors also show an energy consumption requirement of the device to be equal to the existing transistor-based technologies, i.e., ~10^{-17}J. However, these energy computations do not involve the losses due to the resonator dissipation and transduction.

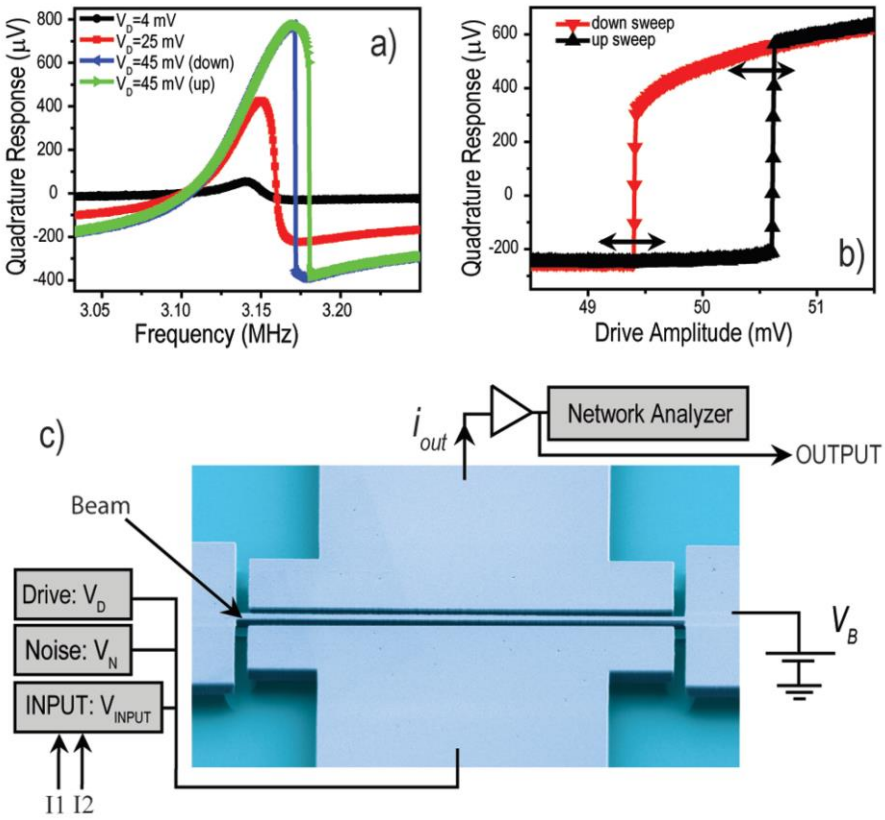

Figure 3. (a) Response of the resonator showing a transition from linear to nonlinear bistable regime as the input voltage is increased. (b) Response of the resonator as a function of the drive amplitude for a fixed frequency (3.158 MHz) in the bistable regime. In the absence of noise this modulation is not able to produce switching between the two states, but as noise is added switching between the two states inside the hysteretic regime becomes possible. The arrow on the top right represents the NOR/OR situation while the arrow on the bottom left represents the NAND/AND situation. (c) Micrograph of the resonator and experimental setup. Re-printed with permission [29].

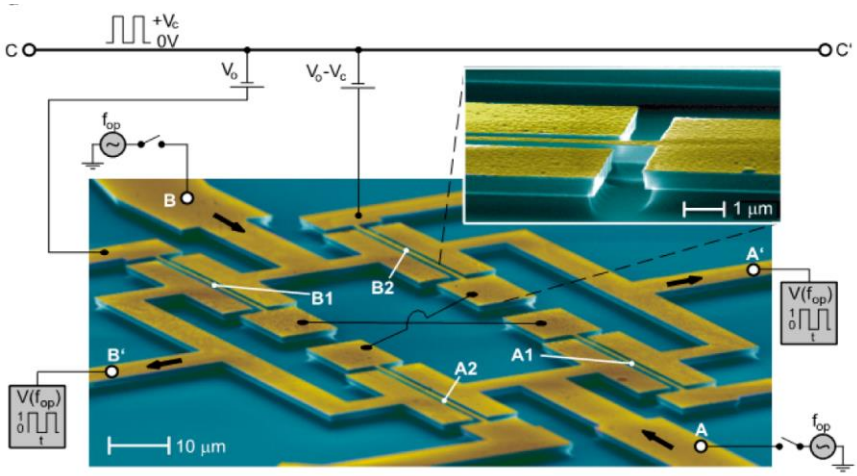

Figure 4. SEM image of the logic device architecture of the Fredkin gate. The device, which consists of silicon (thickness 500 nm) with top gold electrodes (thickness 40 nm), features four nanomechanical beams (A1, A2, B1, B2) of dimensions 20 μm × 300 nm. Capacitive actuation and detection are achieved via parallel electrodes situated 450 nm to either side of each resonator.17 With a DC bias placed on each beam, a high-frequency voltage at an input electrode (A or B) drives in-plane motion through electrostatic forcing. A resonating beam in turn induces

current at an output electrode (A′ or B′), which is amplified and converted into a voltage signal. Re-printed with permission [35].

In another noteworthy contribution, the authors study the function of a digital computing element utilizing parametric oscillation (parametron) [36, 37] and extend it to realize NEMS bit flip and bit storage operation [38]. Two stable phases of an excited harmonic oscillators are used to perform the basics of logic operation. In this work, the first order parametric resonance of a clamped-clamped beam resonator is excited by an AC signal at twice the natural frequency to achieve these stable phases. Transition from one state to another state is used to demonstrate the bit flip and bit storage operation, where the input voltage and its associated phase is varied to achieve this transition. The authors experimentally demonstrate a power consumption of ~10 pW per bit flip/storage operation, which is comparable to the bit operations in CMOS transistor. However, the power consumption of the mechanical oscillation is ~0.1 pW, which is significantly lower. This indicates a piezoelectric transducer efficiency of ~1%. It is anticipated that even if such an inefficient system is realized in a NEMS high frequency resonator ~1GHz, the power consumption can be potentially lower than that of CMOS based technology.

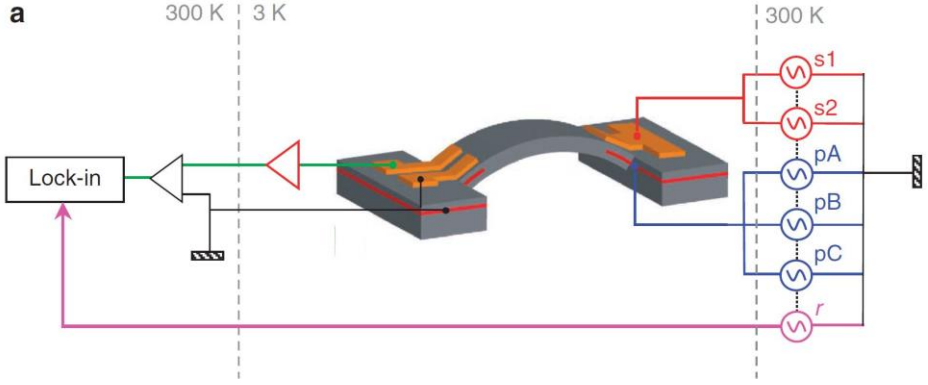

Figure 5. A schematic of the clamped-clamped beam resonator along with the experimental setup. The mechanical oscillator has Schottky Au-electrodes (orange) located above both clamping points, below which a 2DEG is located (red). Application of AC bias to either the 2DEG or the Au-electrodes can trigger both harmonic and parametric resonances where the mechanical motion is monitored by detecting in either a lock-in amplifier or a spectrum analyzer the motion-induced piezovoltage, which is amplified by an on-chip amplifier (red triangle) and a room temperature transimpedance amplifier (black triangle). Pump signals through pA, pB and pC are applied as logic inputs to achieve differ logic gates. Re-printed with permission [39].

Same authors later utilize a similar NEMS resonator, Figure 5, under parametric and multi frequency excitation to perform various fundamental 2-bit logic operations such as AND, OR, XOR, and also multi-bit logic operations [39]. The authors propose to encode multiple channels of binary information on separate frequencies applied to the resonator. These frequencies are then mixed at the resonator and new resonances are produced. These resonances are then recorded and their presence/absence is attributed to the logic High/Low. It is predicted that such a technology when implemented in a NEMS resonator of high frequency ~1GHz and low quality factor ~100, can achieve a bandwidth of 10MHz. Hence, it can potentially execute 5×10^6 64-bits logic operations per second with a single NEMS resonator, which indicates a data-processing capacity of 10^{14}Hzcm^{-2}. Further, the possibility of executing several logic operations simultaneously is shown, which highlights the potential for unprecedented data-processing power with parallel computing.

Arrays of MEMS/NEMS coupled resonators have been proposed for neurocomputing applications due to their interesting nonlinear behavior such as frequency Locking, phase

locking, and synchronization [40-43]. A theoretical network of all-to-all coupled MEMS oscillators, in the presence of stochasticity, is shown to synchronize and store information in the relative phase differences. The study shows that such a system can potentially be robust against noise sources and fabrication imperfections [41]. Recently, the Duffing nonlinearity of a silicon-based MEMS resonator is utilized to experimentally demonstrate reservoir computing [42]. The system predicts a time series and classifies spoken words. Similarly, the nonlinear dynamic phenomena of bi-stability and hysteresis in MEMS coupled structures are exploited to demonstrate and simulate the detection and memory of a single rate model neuron [43].

3.1.Frequency tuning based logic devices

More recently, frequency tuning has been used effectively to perform various computing operations. Here, the device operates on a fixed operating frequency, which is usually the resonance frequency of the device. The switch from on-resonance to off-resonance is made by shifting the resonance frequency away from this operating point to another frequency. This new frequency can be an operating point for another logic gate. This frequency tuning/shifting results in an amplitude change from a high on-resonance amplitude to a low off-resonance amplitude, which is then attributed to the logic output 1(0). This has been primarily achieved by either electrothermal [36, 43] or capacitive tuning of the resonance frequency [44, 49].

3.1.1. Electrothermal tuning

When electric current is passed through a structure, such as a clamped-clamped microbeam, the structure heats up due to Joule's heating [44]. This results in either decreasing or increasing the structure's stiffness depending on its geometry. This causes an increase/decrease in the resonance frequency. A very small value of electrothermal voltage can induce significant change in the resonance frequency of the M/NEMS resonators. Electrothermal actuation of a MEMS clamped-clamped resonator was first used in [45] to perform all the fundamental 2-bit logic gates. It was also shown that the principle is extendable to n-bit logic operations. The devices utilize both the resonance and anti-resonance peaks to perform multiple logic operations. It can be observed from Figure 6, that the resonance frequency of the resonating structure, an arch beam, is increased as the electrothermal logic input is applied. By choosing a different frequency of operation, different logic gates can be performed. For example, NOR/OR logic gate can be performed in region 1 depending on the choice of resonance/anti-resonance frequency as operating point, Figure 6 (black). Similarly, XOR/XNOR can be performed in region 2, and AND/NAND can be performed in region 3. The authors also show that for this specific design the mechanical transition time (4.2ms) defines the operating speed of the device rather than the electrothermal heating and cooling cycle time (152μs).

The same principle of electrothermal frequency modulation was then extended into the nano regime, where a clamped-clamped arched beam was used to demonstrate NOR, NOT, XNOR, XOR, and AND gate operation [46]. The device was shown to be resilient to temperature change within 25^{o}C to 85^{o}C, which is sufficient for most logic operations. Since then, electrothermal actuation has been used to perform different computing operations. Complex logic and computing operations such as single bit binary comparator and single bit 4 to 2 decoder, have been experimentally demonstrated using multiple electrically interconnected clamped-clamped arch microbeams [47]. This work also shows parallel logic operations where an XOR/XNOR, and AND/NOT are performed in parallel. In a similar work, a 4 bit parity checker is also demonstrated experimentally by two electrically connected clamped-clamped arch microbeams

[48]. Electrothermal tuning of frequency can also further be extended to perform memory operations by utilizing the bistable regime of the resonator operating in the nonlinear regime [49, 50], similar to the work in [30].

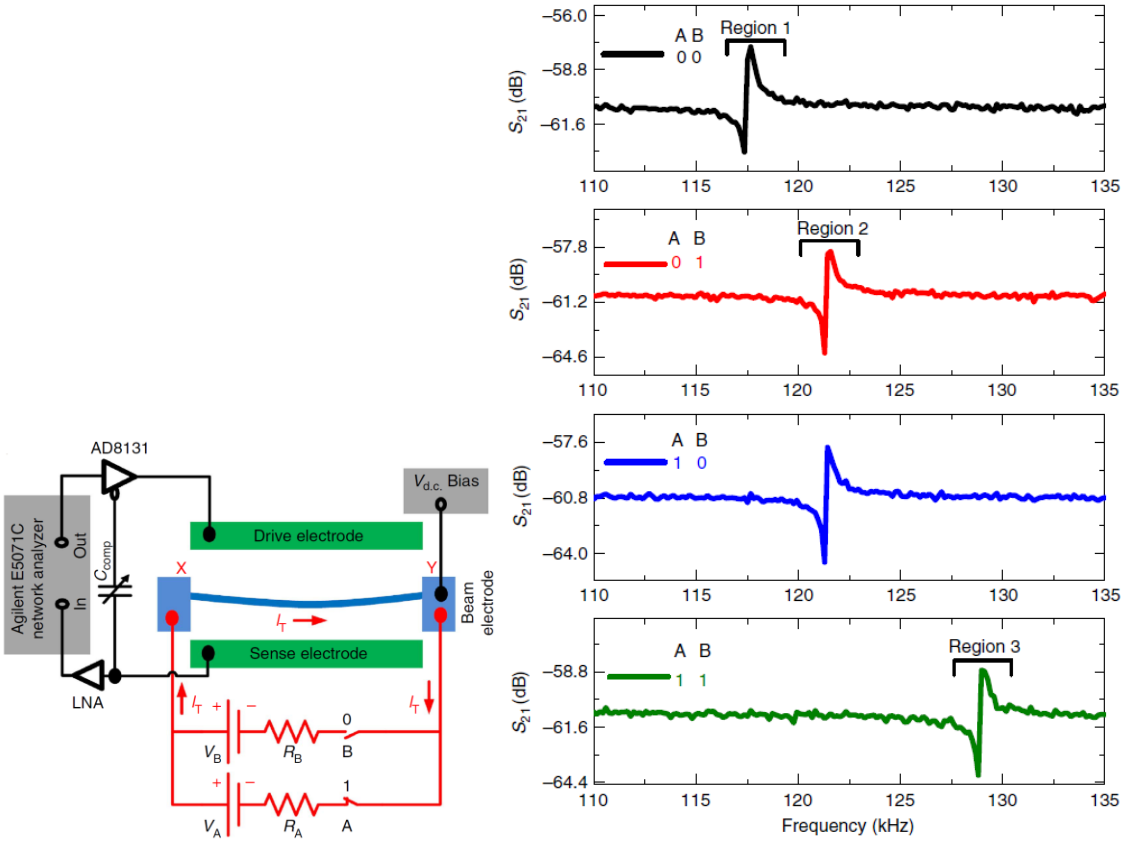

Figure 6. (a) . Schematic of the arch beam resonator and the two-port electrical transmission measurement configuration together with a parasitic current compensation circuitry using single-to-differential driver (AD8131) and a variable compensation capacitor, Ccomp. The drive electrode is provided with an AC signal from one of the outputs from AD8131 and the beam electrode is biased with a DC voltage source. The output current induced at the sense-electrode is coupled with the compensation capacitor and followed by a low-noise amplifier (LNA) whose output is coupled to the network analyzer input port. Two voltage sources, V_A and V_B and switches, A and B are connected in parallel across the beam to perform logic operations by electrothermal tuning of the resonance frequency. The arrow in the red represents the current flowing through the beam, responsible for electrothermal frequency modulation. (b) Frequency responses of the resonator for different logic input conditions (0,0), (0,1), (1,0), (1,1) shown in black, red, blue, and green respectively. The beam is actuated with a V_{DC}=45V, V_{AC}=2dBm at all times. The logic inputs V_A=0.4V and V_B=0.7V. Re-printed with permission [45].

Finally, an unconventional compound resonator consisting of a clamped-guided electrostatically actuated arch beam that is attached to another resonant beam from the side, is used to experimentally demonstrate parallel logic operation [51]. The logic operations are based on the electrothermal linear frequency modulations of the arch resonator and the side microbeam. The device is capable of performing 2-bit fundamental logic operations, such as OR, AND, XOR, NOR, and complex logic operation like half-adder in a single structure.

Electrothermal logic devices provide the advantage of very small voltage logic inputs. Thermal actuation is not however energy efficient compared to other methods like electrostatic

actuation. Furthermore, the thermal time constant of these devices is much higher than the mechanical transition time. Hence, the speed of operation for such devices is limited by the thermal transition time. These issues can be mitigated to some extent by further miniaturization of the devices.

3.1.2. Capacitive frequency tuning

Electrostatic force when applied on a resonator results often in a decrease in its resonance frequency and can also induce softening behavior upon large excitation values [52]. Using the DC bias as logic input is another way to realize logic devices based on frequency tuning. The device in [53] utilizes a laterally electrostatically actuated nano-cantilever beam with fixed electrodes on either side, Figure 7, to achieve the fundamental logic operations of XOR, AND, NOR, OR, and NOT. The switching between the two logic states is performed by applying a gate input in the form of a DC bias on either side of the nanobeams. The device was experimentally demonstrated to be operational up to 100^{o}C, which reduces the need for thermal management systems. Furthermore, a tunable bandwidth of 5MHz is shown, which can be useful in parallel computing and higher bit logic operations. Using DC bias for frequency tuning can result in large logic input voltage values. In order to tackle this, a system of two laterally actuated electrostatically coupled micro-cantilevers was utilized for reduced voltage operation, where also parallel logic gates are experimentally demonstrated [54]. The study has shown a 2-bit XOR, 2- and 3-bit AND, 2- and 3-bit OR, and an inverter. The coupling strength between the two coupled resonators is changed in order to tune/shift the resonance frequency of the first coupled mode and perform these logic operations.

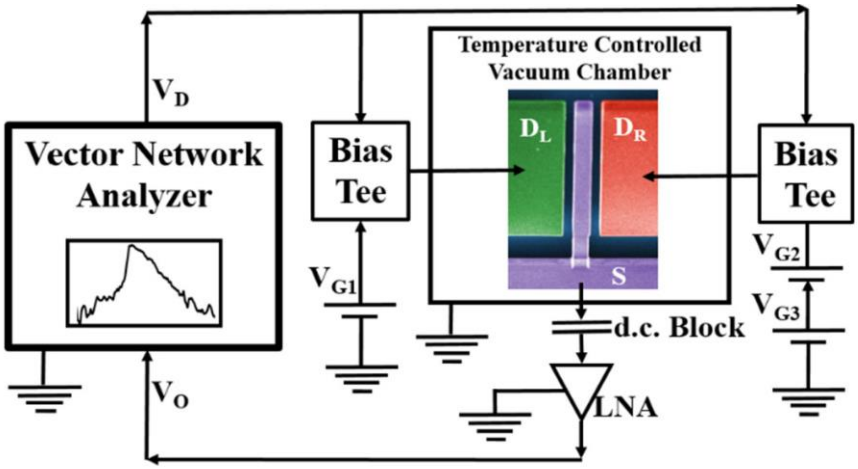

Figure 7. A schematic of the experimental setup configuring the nanobeam as a dual oscillator for reprogrammable universal logic gate. The nanobeam is used as the sense electrode (S) and the two fixed electrodes (opposite to each other) are configured as the drive electrodes (DL, DR). The gate dc inputs are interfaced to the drive electrodes using bias tees. All the fundamental Boolean logic gates are realized in a single device by programing the gate inputs (V_{G1}, V_{G2}, V_{G3}). Re-printed with permission [53].

An in-plane clamped-clamped microbeam with partial electrodes sandwiching it from both sides has been utilized to perform logic and memory operations [55]. Each electrode on either side of the device can act as a logic input, which can be used to bias the beam and hence shift the resonance frequency. One electrode on each side is used for drive/sense while the other two are used as logic input bits. Different logic gates, such as NOR, XOR, and AND, are

experimentally demonstrated. The device is also capable of performing memory operations, which makes it a compact multi-functional computing unit. The same principle is then extended to perform a full-adder and 4-input reprogrammable logic gates [56]. In this case, three electrodes on either side of the resonator are used, where the two electrodesu in the center are used for drive and sense, while the remaining 4 electrodes are used as inputs to the device. It is shown that the ability of resonator-based logic devices to perform complex operations using a single unit can potentially save space and avoid electrical interconnect losses. The authors also experimentally demonstrate a 4 bit AND and NOR gate operation.

Additionally, a clamped-guided arch microbeam has been utilized to perform logic and memory operations [57]. The resonance frequency is modulated through an axial electrostatic force from the guided side of the microbeam. AND, XOR, and NOR logic gates are experimentally demonstrated. The device is also capable of performing single bit read and write memory operations. Resilience to temperature change with a temperature coefficient of frequency ~224 ppm/^{o}C is also experimentally demonstrated.

Unlike electrothermal devices, DC logic input based devices, can have very low energy consumption per logic operation. However, the input values required to achieve the desired tuning can be large and might need additional charge pump circuits, which can increase the total energy consumption of the system by several orders. This however can be resolved by smart design and miniaturization into the nano regime.

3.2.Cascadable logic devices

Logic gates act as basic building blocks, where a multitude of these can be cascaded in different configurations to perform different complex computing operations. Cascadability here refers to the ability of using the logic output of one gate as a logic input for another one. Hence, by cascading several gates, deep logic operations can be executed. Despite the fact that the M/NEMS based logic devices can perform operations like full adder in a single unit, the need to cascade these devices to perform complex logic operations is inevitable. In order to achieve cascading, there are two pre-requisites. First, all the logic gates must operate at the same frequency, and second, the input and output waveform of the signal should be the same. These features must be built into the technique used to perform the logic operations in order to cascade different logic operations without the need of extra electrical components. This is where the DC-based devices suffer (input DC and output AC), which limits their applications as standalone units only rather than part of more complex computing units.

The first attempt towards providing a cascadable architecture was made in [58], where AC signals are used as the logic inputs to perform different logic operations at the same operating frequency. The concepts relies on the activation and deactivation of the combinations resonances arising as a results of electrostatic frequency mixing [59]. The study in [58] uses a simple doubly clamped microbeam to demonstrate an OR, NOR, AND, NAND, and a tristate logic gate. A roadmap is presented for potential cascadability; however, this requires an additional electrical component, i.e., frequency divider, which adds undesirable complexity. Another technique was also shown using an AC only subharmonic excitation of a clamped-clamped microbeam resonator [60]. The logic operation is performed using frequency tuning through the input AC voltage. Successful AND/NAND logic operation has been shown. However, due to an AC only excitation, large logic input voltages are required, which is not favorable toward realizing energy efficient devices.

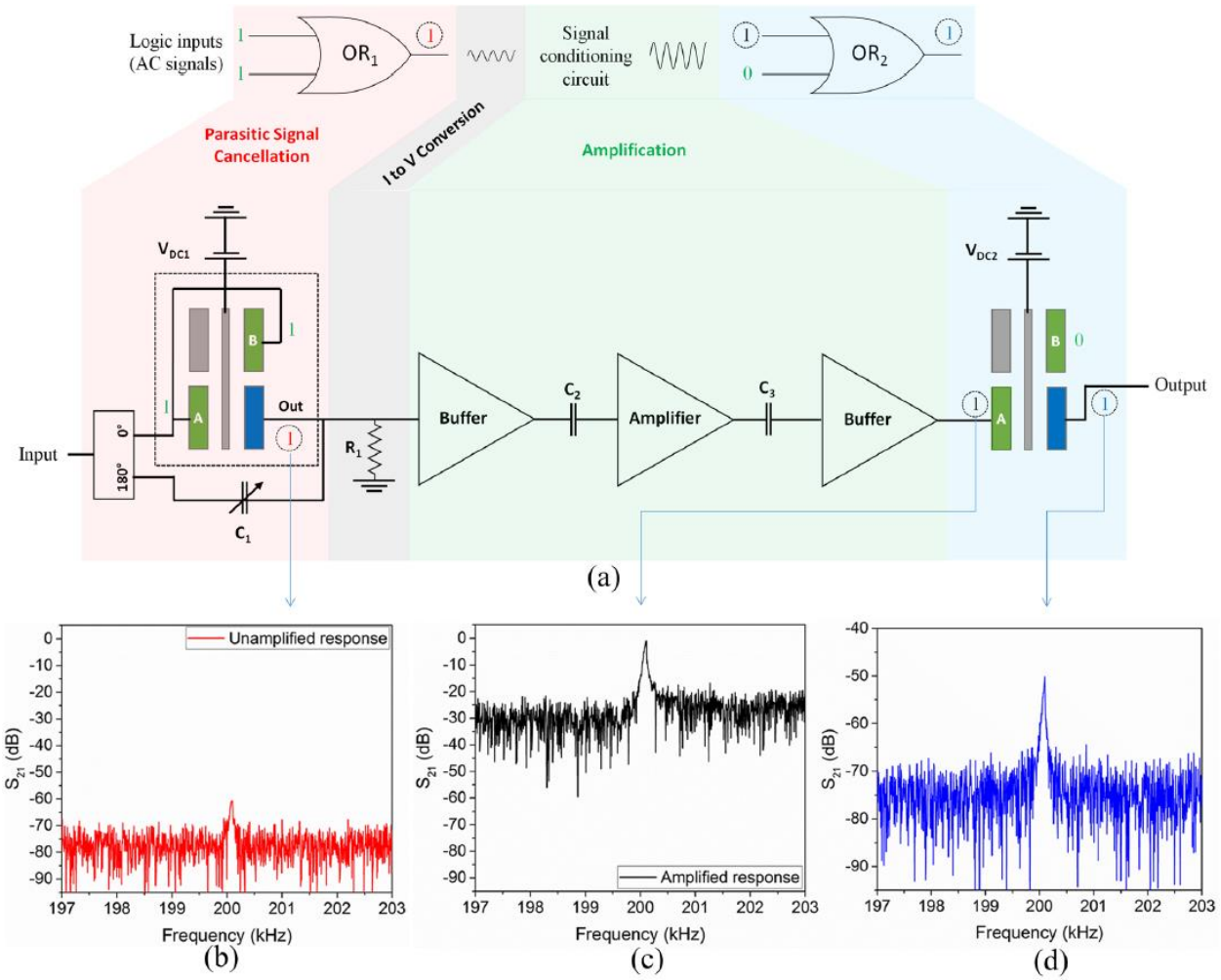

Figure 8. Cascading microresonators. (a) Schematic showing the setup for cascading two OR gates. (b) Response of the first resonator for (1,1) logic input condition. The output is then amplified via the signal conditioning circuit. (c) Amplified response of the resonator after the signal conditioning. This output signal is then applied to the next resonator logic device (OR_2) as '1' logic input. (d) Response of OR2 to a logic input of (10), where the input '1' is the output of OR_1. The experimental parameters are V_{DC} (OR_1) = 55 V, V_{DC} (OR_2) = 65 V, V_{AC} (logic inputs) = −30 dBm (0.007 V_{RMS}), P = 20 mTorr, and T = 25 °C. Re-printed with permission [61].

In spite of all the new techniques and advancement over the past decade, cascading such devices has remained a serious challenge. One solution for this issue has been proposed recently in [61, 62]. The study in [61] utilizes the second mode activation of a laterally actuated clamped-clamped microbeam to perform the fundamental logic operations, such as OR, XOR, and NOT. Further, cascadability is demonstrated experimentally by realizing a logically complete NOR logic gate through cascading an OR and NOT gate. Multi or higher mode excitation for logic devices has been used previously but to show different gates operating at different vibration mode/frequencies, which is not cascadable [63]. It is worth to mention here that the study in [63] utilizes a 2D membrane to perform these logic operations. 2D structures have a possibility of having degenerate modes [64], which then requires a careful selection of frequencies in order to execute the logic gates with certainty.

The study in [61] uses two AC signals as the two logic inputs, hence unifying the input and output waveform. Furthermore, all the gates are performed at the second mode of excitation of the resonator, and hence have a single operating point. Figure 8 shows schematic and

experimental results for a cascade of two resonators set in an OR gate configuration. The response of the first resonator goes through steps of parasitic signal cancellation and amplification before it is fit to drive the next resonator. Figure 8(b) shows the raw motional signal received from the first OR gate. This signal is then conditioned to drive the next OR gate, Figure 8(c). Finally, Figure 8(d) shows the response of the second resonator in OR gate configuration driven only by the output from the first resonator. The same experimental setup is then used to cascade OR and NOT gate to realize the logically complete NOR gate.

4. Discussions and Conclusions

Different performance aspects, advantages, and challenges faced by resonator-based logic devices are discussed in this section. A detail of different performance parameters of the state-of-the-art logic devices is summarized in Table 1.

4.1. Energy Consumption

Energy consumption of M/NEMS resonator-based devices is defined as the energy required to perform a single switching cycle of the logic device. The energy consumption per switching cycle for an electrostatically actuated device using a DC logic input can be calculated by using [29, 35]

$$E_{DG} \approx CV_BV_L \tag{1}$$

where C is the capacitance between the beam and the fixed electrode, V_B is the bias voltage on the beam, and V_L is the logic input.

Similarly, the energy consumption per switching cycle for an electrostatically actuated device using a AC signal as the logic input can be calculated by using [44, 56, 58, 61]

$$E_{AC} \approx \frac{V_{AC}^2}{Z} t_s \tag{2}$$

$$Z = 50\Omega \times 10^{\frac{S_{21}}{20}} \tag{3}$$

where V_{AC} is the AC input signal, Z calculated using (3) is the impedance of the microresonator at resonance including the parasitic impedances, and t_s is the switching time.

Finally, the energy cost per switching cycle for the logic devices that use electrothermal voltage as login input is estimated by calculating the energy dissipation through the resonator [45, 46, 48]

$$E_T \approx \frac{V_R^2}{R_R} t_s \tag{4}$$

where V_R is the electrothermal voltage applied to the resonator and R_R is the resistance of the resonator.

It can be observed from Table 1 that electrothermally operated logic devices consume several orders of magnitude higher energy compared to the electrostatically operated logic devices. Similarly, for relatively bigger devices (sizes in micrometers) [61, 62], the energy consumption is much higher compared to the NEMS resonators. This shows that careful miniaturization of the devices can positively impact the energy performance. Furthermore, as observed from Table 1, NEMS resonators can potentially achieve an energy consumption as low as ~10^{-18}J, which is comparable or even surpasses in some cases, the CMOS based transistor technology i.e., ~10^{-16}J (45nm node) and ~10^{-18}J (7nm node) [61]. It is also important to note here that that a single resonator can be used to perform one or more logic gates while a few transistors are

interconnected to execute the same operations. Hence, for more complex operations where hundreds of transistors are interconnected, resonator-based logic devices can surpass CMOS based computing devices in terms of energy consumption. A detailed analysis for a full-adder is presented in [56], where 2 resonators are interconnected can execute a full adder with 2.39 fJ of energy consumption compared to 28 transistors (65nm node) with an energy consumption of 6.32 fJ. It is important to note that the study in [56] utilizes a big micro scale structure to execute this operation. With careful optimization in size, such devices can potentially provide significant advantage in terms of energy consumption over their CMOS counterpart.

However, it is worth to mention here that apart from the energy required to perform the switching action, an activation energy is also required to vibrate the resonator, for example, an AC signal is necessary to achieve a resonance response of the resonator. Considering the state of the art, this response is then manipulated by a DC signal, either capacitively or electrothermally, in order to achieve the desired logic operation. However, a constant AC signal is provided to the resonator at all times to keep it in a working/vibrating state leaks power in the form of parasitic losses and is analogous to the off-state current leakage of the transistor. Such a configuration cannot be claimed to produce ultra-low energy devices. Hence, for future devices it is necessary to perform logic operations using AC logic inputs to fully capitalize on the potential of resonator-based logic devices. Further, the output of resonator-based devices is always an AC signal; hence having an AC input naturally unifies the input and output signal waveform, which is a pre-requisite for cascading. The study in [61, 62] capitalizes on both these aspects and presents a ground work for future ultra-low energy consumption and cascadable logic devices. However, it is worth to mention that ~ 10^{-13} J in Table 1 is the energy consumption for an individual logic gate. Energy consumption for a cascaded gate must include the losses through the intermediate electronic components, which is estimated to be of the order ~ 10^{-10} J for NOR gate [61]. However, it is predicted that this value can be lowered with careful design for a multitude of cascaded logic gates.

4.2. Reconfigurability and Space density

Reconfigurability and space density is another feature of the resonator-based logic devices that can potentially provide an advantage over its CMOS counterpart. As observed from Table 1, a single resonator-based logic device can perform several different logic operations by changing the active input signals at different electrodes. On the other hand, different number of transistors must be connected in different electrical interconnect schemes to realize different logic gates, and once connected, they cannot be reconfigured to perform different logic gates. This has serious implication on the integration/space density that can be achieved on a circuit when using such devices. The need towards miniaturization demands high integration and packing densities of these computing components. It can be observed that integration densities as high as ~10^7 cm^{-2} can be achieved, which surpasses some of the transistor based logic gates, i.e., ~10^6 cm^{-2} (45 nm node-2 input XOR) [56, 61]. This advantage is further amplified when performing complex computing operations. For example, the study in [56] utilizes two resonators to realize a full adder with a space density of ~10^8 cm^{-2}, while the same is realized by interconnecting 28 transistors with a integration density of ~10^6 cm^{-2}. Furthermore, active reprogrammability of the resonator-based logic devices to switch from one logic gate to another in a single device is a unique feature that is absent in CMOS technology. This can potentially allow for achieving high density computing units with simple and less electrical interconnect schemes.

4.3. Speed of operation

The speed of operation in resonator-based logic devices is defined by the mechanical transition time of the resonator given by

$$t_s = \frac{Q}{f} \tag{5}$$

where Q is the quality factor of the resonator and f is its resonance frequency. It is worth to mention here that the formula of (5) accounts for the settling time and ensures a steady state operation. Hence, for cascaded systems, any commands directed to the gate can come at the earliest after the settling time and at the proposed calculated speed. So, the next stage has to wait for commands to come after steady state.

This technology cannot compete with the CMOS based counterpart. Even though with miniaturization into few nanometers, a high frequency (GHz) of operation could be potentially achieved, however, is challenging and will amplify signal to noise ratio issues. Hence, the goal of the resonator-based logic devices should be to target low (kHz) to medium (MHz) frequency operations, which are commonly used for microcontrollers, embedded systems as well as others sensors and computing devices that do not require high speed of operation. This does not undermine the potential impact of such a technology as these low speed devices are widespread in our daily life and will certainly benefit from such technology.

Table 1. Specifications of the state-of-the-art resonator-based logic devices

Research work	Actuation technology	Principle of logic operation	Speed of operation	Energy consumption per logic operation for a single gate	Space density	Logic gates
Masmanidis *et al.* [28]	Piezoelectric	Cancellation of vibration motion using crystallographic anisotropy of piezoelectric material	~0.2 ms	~5fW, ~10^{-18} J	~10^{7} cm^{-2}	XOR Gate only
Guerra *et al.* [29]	Electrostatic	Utilizing the bi-stable regime of a nonlinear resonator	~0.2ms	~10^{-17} J	~10^{7} cm^{-2}	NOR/OR. NAND/AND
Wenzler *et al.* [35]	Electrostatic	Resonance frequency tuning	~0.2µs	~10^{-17}J	~10^{7} cm^{-2}	Reversible AND, OR, NOT, and FANOUT gate
Mahboob *et al.* [38, 39]	Piezoelectric	Parametric excitation and frequency mixing	~0.83s	~ 0.1 pW, ~10^{-14}J	~10^{4} cm^{-2}	Bit flip/storage, AND, OR, XOR, and Multibit gates
Chappanda [53] *et al.*	Electrostatic	Resonance frequency tuning	~200 μs	~ 10^{-15} J	~10^{6} cm^{-2}.	XOR, AND, NOR, OR and NOT
Kazmi *et al.* [46]	Electrothermal	Resonance frequency tuning	~35 µs	~ 10^{-9} J	~10^{6} cm^{-2}	NOR, NOT, XNOR, XOR, and AND.

Saad *et al.* [61, 62]	Electrostatic	Activation and deactivation of a resonant mode	~35 ms	~ 10^{-13} J	~10^{3} cm^{-2}	OR, XOR, NOT, and cascaded NOR

4.4. Amplification of output signal

Another major challenge facing the electrostatic resonator-based logic devices is the low output signal. Despite the advantages of electrostatic actuation, the electrostatic transduction suffers from the fact that the output motional signal of the resonators is very small. This is an issue not only for cascadability of such devices but also for standalone logic units, which will require electrical components in order to effectively readout the logic output signal. These components can have several order of magnitude higher power consumptions compared to the logic unit itself. A promising scheme has been presented theoretically in [61], however is yet to be verified experimentally. Hence, future research is needed to either minimize these transduction losses or to come up with a different transduction and signal amplification (for example mechanical) schemes. For example, a hybrid resonator with electrostatic actuation and piezoelectric detection can be employed to benefit from the strength of both technologies.

4.5. Frequency Mismatch

Apart from the amplification circuit required for cascadability, another challenge is the frequency drift between the resonators due to fabrication imperfections or over a long time of operation, can cause failure among cascaded logic devices. A DC bias is always applied to the resonator, which gives some level of tunability of the resonance frequency. This can be potentially used to overcome such an issue. Furthermore, it is desired to have low Q devices in order to achieve high speed of operation, i.e., $t_s \propto Q$. This allows for large tolerance in terms of matching frequencies from one resonator to another. However, low Q also means a low signal to noise ratio, which is undesirable.

4.6. Conclusions

M/NEMS based logic devices have the potential to provide ultra-low energy consumption devices, which can be used as multi-functional standalone units or in a cascade to perform computing operations. Such devices can potentially replace transistor-based computing in sensors and devices that require medium operating speeds, such as in microcontrollers and embedded systems, which are wide spread in our daily lives. It can also be particularly useful for applications, such as battery operated sensors installed in remote areas or not easily accessible for battery replacement, i.e., a gas or pressure sensor inside a machine, a weather sensor in a remote location, can have an extended life span through employing the zero-off state and ultra-low energy consumption logic devices. However, the technology is still a long way from being used in practical applications. Although several potential logic techniques, and even cascadability, have been shown experimentally, the use of electronics before and after these devices can result in higher energy consumption than desired. The way forward should be to develop techniques and realize cascadable logic devices using fully mechanical components. M/NEMS resonance-based logic devices have shown promising results so far and can be potentially be a viable alternative computing technology.

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