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Two-dimensional (2D) transition metal dichalcogenide (TMD) layered materials are promising for future electronic and optoelectronic applications. The realization of large-area electronics and circuits strongly relies on wafer-scale, selective growth of quality 2D TMDs. Here, a scalable method, namely metal-guided selective growth (MGSG) is reported. The success of transition metal precursor vapor pressure control, the first concurrent growth of two dissimilar monolayer TMDs is demonstrated in conjunction with lateral or vertical TMD heterojunctions at precisely desired locations over the entire wafer in a single chemical vapor deposition (CVD) process. Owing to the location selectivity, MGSG allows the growth of p- and n-type TMDs with spatial homogeneity and uniform electrical performance for circuit applications. As a demonstration, the first bottom-up complementary metal-oxide-semiconductor (CMOS) inverter based on *p*-type WSe_2 and *n*-type $MoSe_2$ is achieved, which exhibits a high and reproducible voltage gain of 23 with little dependence on position.

Transition metal dichalcogenides (TMDs) such as MoS_2 have been recognized as high on-off ratio semiconductors[1] which are promising for high-quantum yield optoelectronics,[2] next-generation transistors[3] and integrated circuit applications.[4, 5] In addition to the use of a single MoS_2 material, the formation of p-n junctions between two different TMD monolayers (ML) enables device functionalities including current rectifying, light emitting and photon harvesting.[6-9] The realization of modern electronics strongly relies on the integration of both *p*- and *n*-type semiconductors to construct complementary metal oxide semiconductors (CMOS). Ion implantation has been widely adopted for tuning the channel polarity in Si-semiconductors; however, it causes severe damage to 2D TMD materials. Chemical or physical[10, 11] doping may transform one type of TMD to the other, but the associated defects and poor thermal stability make such doping processes unrealistic for

practical applications. Therefore, the concept of using two dissimilar TMDs, one *p*- and one *n*-type TMD, has been recently demonstrated for circuit applications.[12]

Since the demonstration of the vapor phase growth of small MoS_2 monolayer flakes,[13] significant progress has been made including the growth of large-flake,[14, 15] wafer-scale[16, 17] and even roll-to roll[18] ML TMDs. The direct growth of seamless junctions between two dissimilar ML TMDs[19-23] have also been achieved. Besides, it is also demonstrated to grow two types of TMDs by conversion of two metal oxides on separate substrates.[24] These approaches, while encouraging, cannot grow two dissimilar ML TMDs on the same substrate in a highly location-selective manner. Here, we report a bottom-up growth called metal-guided selective growth (MGSG), which allows the precise deposition of specific TMDs onto desired locations controlled by the patterned metal pads. The proposed new method also enables the concurrent growth of two dissimilar ML TMDs on the same substrate; hence, well-defined lateral or vertical p-n heterojunctions can be achieved. More importantly, the first bottom-up CMOS inverter, consisting *p*-type WSe_2 and *n*-type $MoSe_2$ grown by the proposed MGSG, is demonstrated.

The synthesis of typical ML TMDs such as MoS_2, WS_2, $MoSe_2$ or WSe_2 with the proposed MGSG is illustrated in **Figure 1a**, where transition metal (Mo or W) pads with thickness of 50 nm are photolithographically defined on sapphire substrates. Instead of random growth of TMD flakes through the use of metal oxide (WO_3 or MoO_3) powders as the metal sources,[13] the pre-patterned metal pads provide directional diffusion of W or Mo to the local environment for TMD growth. Taking WSe_2 growth as an example, the W metal pads are first heated to the reaction temperature of 900°C under an Ar/H_2 environment at 8 Torr (Ar: H_2= 65 sccm: 5 sccm). During the process, trace amount of oxygen from ambient environment that is known to continuously diffuse to the system

first oxidize the W metal surfaces to form WO_2 (determined through Raman spectra in **Figure S1**) during the heating process. After ramping up the temperature of Se powders, the Se vapors react with the WO_2 species evaporated from the oxidized W pads to form ML WSe_2. The local concentration of WO_2 vapors dominates the growth and hence the triangular ML WSe_2 always initiate at the metal pad edges and in between two adjacent pads. The ML WSe_2 crystals eventually merge as a film when the growth time extends to one hour as shown in **Figure 1b**. Four typical ML TMDs, such as MoS_2, WS_2, $MoSe_2$ and WSe_2, can be easily and controllably grown with the MGSG method. **Figure 1c** shows the photos, Raman and photoluminescence (PL) spectra of obtained ML TMDs. The Raman spectrum shows characteristic phonon modes for MoS_2 at 384 cm^{-1} (E') and 404 cm^{-1} (A'_1), for WS_2 at 354 cm^{-1} (E^1_{2g}) and 417 cm^{-1} (A_{1g}), for $MoSe_2$ at 240 cm^{-1} (degenerated E_{2g} and A_{1g}) and for WSe_2 at 250 cm^{-1} (degenerated E' and A'_1), proving that they are monolayers. The intense PL emission is located at 1.83 eV for MoS_2, 1.97 eV for WS_2, 1.53 eV for $MoSe_2$, 1.63 eV for WSe_2, respectively. Importantly, PL and Raman spectra measured from these four TMDs thin films exhibit characteristic peaks unique only to ML exfoliated standards, regardless of the location of the measurements within the transition metal pads. Since the metal oxide sources (metal pads) are right on the substrate surfaces and the metal edges readily serve as seeds for immediate lateral growth, MGSG can easily achieve the "location-selective growth". The above observation also brings out the remarkable feature of MGSG, the growth of ML TMDs shows less substrate sensitivity. In addition to sapphire, we have verified that the growth can be achieved on arbitrary substrates including silicon dioxide (SiO_2), silicon nitride (Si_3N_4), and hafnium oxide substrates (HfO_2, **Figure S2** in SI). The unique features of location-selective and substrate-insensitive growth of TMDs not only alleviate the

substrate constraints but also allow us to forge ahead with otherwise impossible growth of heterojunctions.

Here, to further demonstrate the utility of MGSG, we show that it is possible to grow a lateral (LHJ) or a vertical heterojunction (VHJ) with MGSG. **Figure 2a** illustrates the one-step growth of a LHJ in between W and Mo metal pads, where the growth of both WSe_2 and $MoSe_2$ were found to confine along W and Mo pads respectively with the presence of Se vapors. LHJ was found to form after the two TMDs join together. **Figure 2b** displays the top view of the HJ after isolation with photolithography, and the PL spectra in **Figure 2c** show that the region adjacent to W (Mo) is covered by WSe_2 ($MoSe_2$) with an alloy region ($W_xMo_{1-x}Se_2$) at the center. Raman mapping recorded in **Figure S3** spatially reveals that the center alloy region is around 40 μm across the distance between two metal pads of 100 μm. Meanwhile, **Figure 2d** schematically depicts the growth of VHJs, where the ML $MoSe_2$ first grown in between two Mo metal pads at 750℃. Then the sample was heated up to a higher temperature (850℃) to trigger the evaporation of WO_2 from an adjacent W pad to complete the growth of a vertically stacked $WSe_2/MoSe_2$. **Figure 2e** displays the top view photo of the area which defines the growth of VHJs, where cross-sectional transmission electron microscopy (TEM) provides a well-defined VHJ comprised of $WSe_2/MoSe_2$ bilayers (details in **Figure S4** in SI). As expected, the intensity of PL measured at the VHJ region (red line in **Figure 2f**) is substantially quenched as a result of interlayer interaction.[25] The Raman spectra also corroborate the success of VHJ growth (**Figure S5** in SI).

The key feature of the MGSG is the capability to grow two ML TMDs concurrently and location-selectively, which is advantageous for constructing a CMOS circuit. **Figure 3a** illustrates the successive diagrams of direct growth of both ML WSe_2 and ML $MoSe_2$ as *p*- and *n*-channel materials,

respectively. Pairs of W and Mo transition metals are patterned on desired locations on a sapphire substrate, followed by the concurrent growth of WSe_2 and $MoSe_2$ using MGSG with the heating profile same as LHJ growth discussed in **Figure 2a**. After an isolation process, location-controlled *p*- and *n*-type ML TMD films are obtained as shown in **Figure 3b**, where the *p*-type WSe_2 and *n*-type $MoSe_2$ films are marked by red and blue dash rectangles. Importantly, this is the first demonstration of a highly location-controlled growth of two ML TMDs in micrometer scale. Raman spectra collected from various sites in regions adjacent WSe_2 and $MoSe_2$ areas (**Figure S6** in SI) uniformly attest to the absence of unwanted alloy structures in each area. In parallel, Raman mapping spatially reveals the uniform distribution of WSe_2 and $MoSe_2$ over the desired area via tracing the characteristic Raman active modes at 250 cm^{-1} assigned to WSe_2 and 240 cm^{-1} assigned to $MoSe_2$. Corresponding PL spectra, in **Figure S6f and S6g**, collected for both areas also mesh well with the Raman mapping, further confirming the success of growing ML WSe_2 and ML $MoSe_2$.

The ability to concurrently grow *p*-type ML WSe_2 and *n*-type ML $MoSe_2$ on the same substrate in a location selective fashion not only neatly sidesteps the time-consuming and laborious multistep transferring process and complex e-beam lithography but also enables the bottom-up construction of CMOS inverter. Note that the metal sources (W and Mo pads) after MGSG become less conductive as a result of metal chalcogenide; thus, new contact metals are deposited to infer the intrinsic output characteristics of CMOS. To form the ohmic contact with *p*-type WSe_2 and *n*-type $MoSe_2$, Palladium (Pd) and Titanium (Ti) are selected as source/drain electrodes.[26, 27] A CMOS inverter can be constructed as shown in the photo and device schematic configuration in **Figure 4a**, where the ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl) imide (EMIM/TFSI) is used as the gate dielectric layer on top. Before adding the ionic liquid, the output currents for WSe_2

and $MoSe_2$ are collected separately. As shown in **Figure S7** in SI, the increase in the output current of $MoSe_2$ suggests its *n*-typed characteristics when the environment changes from air to vacuum, i.e. removal of the oxygen *p*-dopants.[28] In contrast, the output current in WSe_2 decreases, indicating that it is initially *p*-typed. After adding the ionic liquid gate dielectrics, the transfer curves (**Figure 4b**) of the electric double layer transistors (EDLTs) based on $MoSe_2$ show a unipolar n-type behavior with a subthreshold swing (SS) of 98 mV/dec, electron mobility of 10.68 $cm^2V^{-1}s^{-1}$ and the extracted contact resistance by Y-function method is 3.2×10^5 Ω·μm.[29-31] Consistent with the literature,[32] an ambipolar behavior of WSe_2 EDLT with a stronger p field-effect transistor (pFET) feature is observed, where the SS and hole mobility are extracted as 208 mV/dec and 11.49 $cm^2V^{-1}s^{-1}$ with contact resistance of 2.4×10^5 Ω·μm. The contact resistance of devices realized by this MGSG method are comparable with reported conventional contact-exposure lithography method.[28, 33-35] Alternatively, to further streamline the fabrication flow, pre-patterning Pd and Ti pads before the deposition of W and Mo transition metal pads enables the direct integration of a device ready architecture after completing the concurrent and selective growth of dissimilar ML TMDs. More than fifteen WSe_2 and $MoSe_2$ transistors are collected as shown in **Figure 4c**, and the average threshold voltage (V_{th}) of WSe_2 is about -1.5 V and is about 1 V for $MoSe_2$ with compatible on-current at V_g = -3V for WSe_2 and at V_g = 3 V for $MoSe_2$. The combination of a WSe_2 *p*FET and a $MoSe_2$ *n*FET enables the inverter operation. In our experiment, a supply voltage V_{dd} is 1.5 V, the input voltage (V_{in}) = 0 V represents the logic state "0", and V_{in} = 2 V represents the logic state "1". A typical inverter behavior is shown in **Figure 4d**, where the measured output voltage (V_{out}) is close to 1.3 V at logic state "0", and V_{out} is close to zero at the logic state "1". **Figure 4e** presents the output voltage dependence on input voltage, where the transition voltage (V_T) is around 1 V. The V_{out} is close to 1.3 V with a low V_{in} (<

bV_T), and V_{out} is close to 0 V when V_{in} is larger than V_T. Under V_{dd} = l.5 V, a voltage gain of 19.7 (calculated by dV_{out}/dV_{in}) is achieved, and the highest voltage gain of 23 is reached at V_{dd} = 3 V (**Figure S8a** in SI). The histogram of voltage gain collected from sixteen CMOS invertors fabricated by MGSG exhibit a narrow distribution, confirming the low batch variation, uniformity, quality and fidelity of MGSG (**Figure 4f**).

Furthermore, we demonstrate the concurrent-growth of ML WSe_2 and $MoSe_2$ even when the distance between the metal (Mo or W) pairs is one-order smaller (10 μm) as shown in the OM images along with the corresponding Raman spectra and mappings (**Figure S9)**. While the diffusion length of WO_2 or MoO_2 vapor can reach ~100 μm, the precursor from the nearest transition metal source dominates the growth, lateral width of the alloy region is also scaled down accordingly. Besides, this layout with smaller dimensions is realized with less metal source, where the width of the pre-deposited metal pad approaches the limitation of conventional contact-exposure photolithography (~3 μm). Importantly, this is the first CMOS inverter fabricated using location-selective and bottom-up grown TMDs, which are readily scalable and industrially feasible for device fabrication. The performance of our direct grown hetero-TMD CMOS inverter (marked as red pentagon, and star) is comparable to those obtained by using transfer methods or other non-scalable approaches (**Figure S8b** in SI). Whereas all the reported works still leverage the time-consuming and laborious transfer process, MGSG approach enable the location selective construction of complementary inverters over the entire wafer with comparable and reproducible voltage gain, representing a step closer to practical and scalable implementation of 2D atomically thin complementary inverters.

The realization of precursor vapor pressure control also enables the success of wafer scale growth. In conventional CVD process, transition metal oxide powders (MoO_3 or WO_3) are used as precursors and placed at upper stream relative to the substrates. The omnidirectional diffusion of metal vapors in conjunction with a serious vapor concentration drop always give rise to a non-uniform growth distribution when the distance between metal sources and designated substrates increases as illustrated in **Figure 5a**. Hence, it is extremely challenging to enable the wafer-scale growth. **Figure 5b** features a photograph of MoS_2 grown on 2-inch sapphire by conventional CVD process. The as-grown MoS_2 shows a significant gradient distribution along the direction of gas flow. Indeed, a series of optical microscope images (**Figure 5c**) taken along the gas flow crossing whole wafer as marked in red dash line in **Figure 5b** also revealed the non-uniform growth, where more bilayers and particles at the upstream side and isolated flakes at the downstream side are observed. In contrast, our MGSG process pre-defines the transition metal source by pre-patterning metal pads periodically on the whole wafer, creates a uniform and localized precursor vapor over the entire wafer rather than specific precursor-substrate chemistry as shown in **Figure 5d**, and provides a general route for producing spatially continuous, structural and electrical uniform ML TMD over the entire area of wafer. To this end, we follow the same drill: The photolithographically defined transition metal pads are pre-annealed in air to form metal oxide at the surface, thus establishing the foundation for facilitating MGSG. **Figure 5e and 5f** present the growth of ML MoS_2 on a 2" sapphire wafer and show wafer-scale homogeneity, device ready architecture for batch device fabrication at technological relevant scale, structural continuity and maintained uniformity over the entire film. The apparent color uniformity of the ML MoS_2 film by MGSG suggests that the MoS_2 grown region is uniform over the whole substrate in stark contrast to the conventional CVD grown MoS_2 that only provides limited

control over the average layer number and produces spatially inhomogeneous mixture of ML, multi-layer, islands, and no-growth regions. Further, the PL spectra measured from MGSG MoS_2 film show characteristics unique to ML MoS_2. All of the PL spectra collected at different spots of the MGSG MoS_2 film in a 4 x 4 grid fashion display the same peak positions as in exfoliated monolayered samples, regardless of the location of the measurements within our films as shown in **Figure S10**.

In addition to the directional flow of metal vapor, to realize the concurrent-growth of dissimilar TMDs also lies in the dedicated control of the pre-annealing process that is known to vary the degree of oxidation of metals and thus the subsequent epitaxial growth of TMDs. Here, as suggested in **Figure S11**, the substrates with different patterned metal pads are separately pre-annealed at 400℃ in air (high P_{H_2O}/P_{H_2}) and at 700℃ in vacuum with 65 sccm Ar/ 5 sccm H_2 (low P_{H_2O}/P_{H_2}). The metal pads annealed in air become metal trioxide (MoO_3 and WO_3), and those annealed in vacuum transform into metal dioxide (MoO_2 and WO_2). As a result, after MGSG process, only Mo related TMDs (MoS_2 or $MoSe_2$) are found to grow on substrates that are pre-annealed in air while concurrent growth of TMDs with dissimilar metals carries out when the substrates are pre-annealed in vacuum. The stark contrast in growth kinetics is found to strongly tie with the vapor pressure of metal oxides. As shown in **Figure S11b**, MoO_3 has much higher vapor pressure than WO_3. Thus, the WO_3 vapor is largely suppressed during MGSG process (Region 1), leading to predominate growth of Mo-related TMDs. On the other hand, after annealing in vacuum, the metal dioxide pads (MoO_2 and WO_2) show compatible vapor pressure, which allows to grow two different TMDs concurrently (Region 2).

In conclusion, we report a new method, MGSG, to realize the location-selective and simultaneous growth of two dissimilar TMDs in a one-step CVD process over the entire wafer. This method offers a

new perspective to control delivery sequence of different precursors, capable of growing various structures including lateral and vertical HJs, and two types of FETs concurrently. Indeed, the challenging growth of wafer-scale 2D TMDs required by the top-down device fabrication is not necessary anymore because MGSG exhibits the IC-compatible and bottom-up growth features, which not only advance the knowledge and technology for the growth, patterning, and integration of high quality ML 2D materials with different semiconducting nature on a single wafer but represent a step towards the realization of atomically thin integrated circuitry and electronic device applications.

Experimental Section

Raman and Photoluminescence (PL) spectroscopies: Optical spectroscopy is taken under a Witec alpha 300R confocal Raman microscopic system. Gratings of 1800 meshes/mm and 300 meshes/mm are selected for high resolution Raman spectrum and wide range PL spectrum respectively. The TMDs are excited by 532 nm laser with power of 1 mW and spot size of 0.5 μm, and emitted Raman signal is collected by 100x objective (N.A = 0.9) from a Carl Zeiss Microscopy. Raman spatial mapping is acquired with spatial resolution of 0.33 μm.

Metal-Guided Selective Growth (MGSG) Process: C-plane sapphire is cleaned by piranha (H_2SO_4: H_2O = 7:4) and deionized (DI) water. 50 nm thick transition metals (Mo, W or both) are then deposited and patterned by the photolithography, sputtering and lift-off process. The MGSG process is carried out by a modified CVD system. The patterned substrate is placed at the center of furnace, and the quartz boat filled with chalcogen (S or Se) powders are placed at the upper stream side. System is first pumped down to base pressure of 0.1 mTorr and then maintains at a constant pressure of 8 Torr by a constant flow of 65 sccm argon and 5 sccm hydrogen. After purging for five minutes, the

furnace is heated up to 900 ^{o}C at a ramping rate of 25 ^{o}C/min., and chalcogen quartz boat starts to be heated up and maintained at 250 ^{o}C by another heating unit when the furnace temperature reaches 700 ^{o}C. Furnace is kept at 900 ^{o}C for 15 minutes to 1 hour, then cooled down naturally to room temperature. Different coverage of ML TMDs is grown between pads depending on the growth time.

For growing LHJs, temperature of MGSG process is modulated between 800-900^{o}C to adjust the equivalent vapor pressure from W and Mo. In contrast, to grow VHJs, the temperature profile of MGSG process is divided into two steps: first step is to grow $MoSe_2$ at lower temperature (700-750 ^{o}C), at which WO_2 evaporation is prohibited; second step is to grow WSe_2 at higher temperature (800-900 ^{o}C) to form VHJs.

Fabrication of CMOS inverter based on MGSG WSe_2-$MoSe_2$: Contact aligner (EVG 6200NT), photoresist AZ3027 and developer AZ326 are used for the photolithography process. After achieving WSe_2-$MoSe_2$ selective area growth, substrate is first isolated by remote ion etching (RIE) process, operated under 200 W inductively coupled plasma (ICP) and 50 W radio frequency (RF) with 20 sccm O_2 and 5 sccm Ar. 20 nm Pd/50 nm Au and 20 nm Ti/50 nm Au are selected as contact electrodes for WSe_2 and $MoSe_2$ respectively. Both electrodes are deposited by E-beam evaporation and lift-off processes. CMOS inverter is finally achieved after dropping ionic liquid on both WSe_2 and $MoSe_2$ channels as a gate dielectric layer.

Electrical measurement: The electrical measurement is carried out in a probe station and Keithley 4200 mounted with Pre-Amplifier. EDLT measurement is taken under vacuum chamber pumped by Agilent TPS V84FS turbo pumping system.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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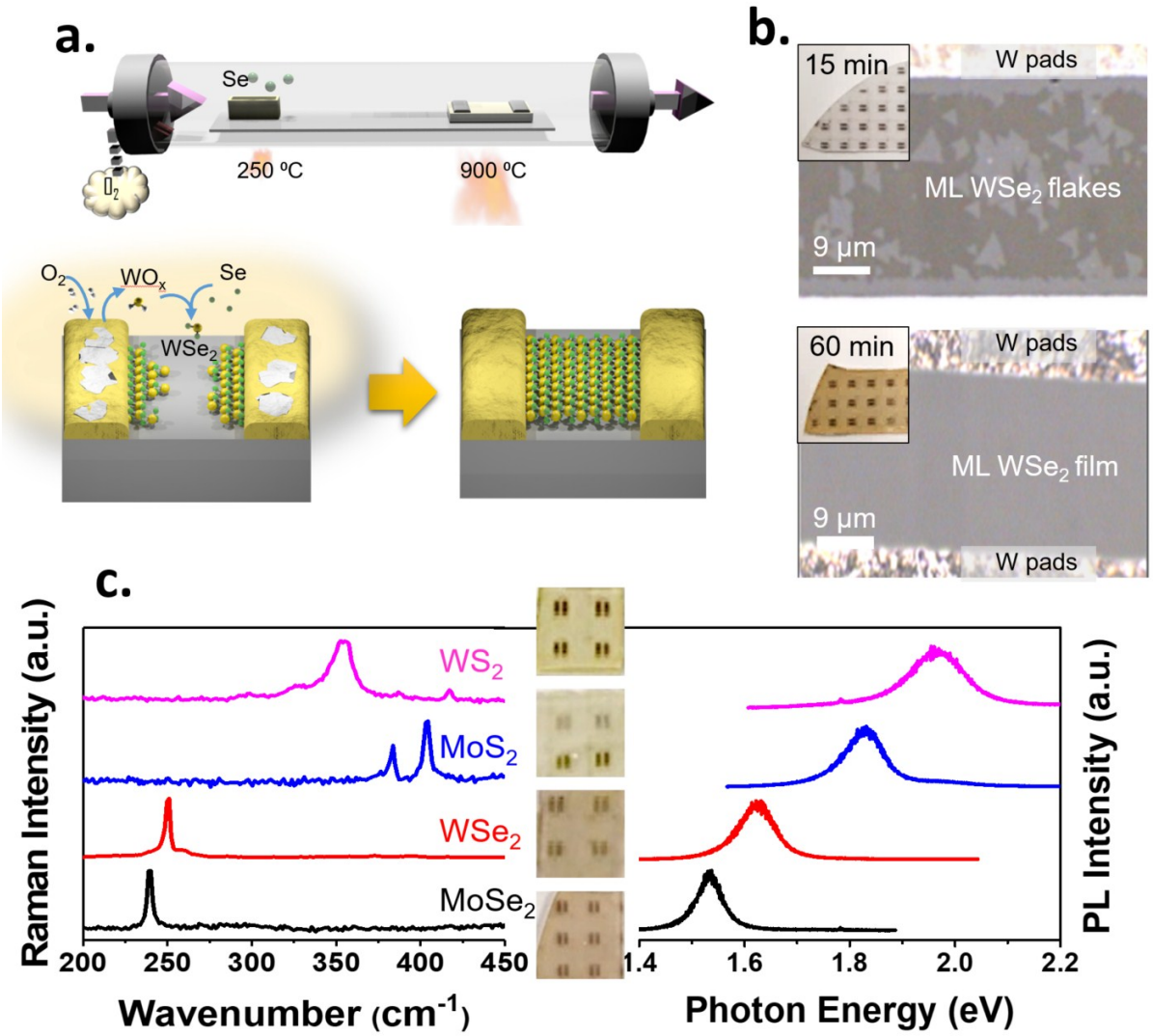

Figure 1. Metal-Guided Selective Growth of TMD Films. (a) Schematic illustration of the growth system and the metal-guided selective growth in a tube finance. (b) Top panel is the OM image showing the growth initiates at the metal pad edges and in between two adjacent pads (growth time: 15min). The WSe_2 monolayer crystals eventually merge as a film when the growth time extends to 60 min (bottom panel). (c) The photos (center), Raman (left) and PL spectra (right) of four different ML TMD films grown by the MGSG method.

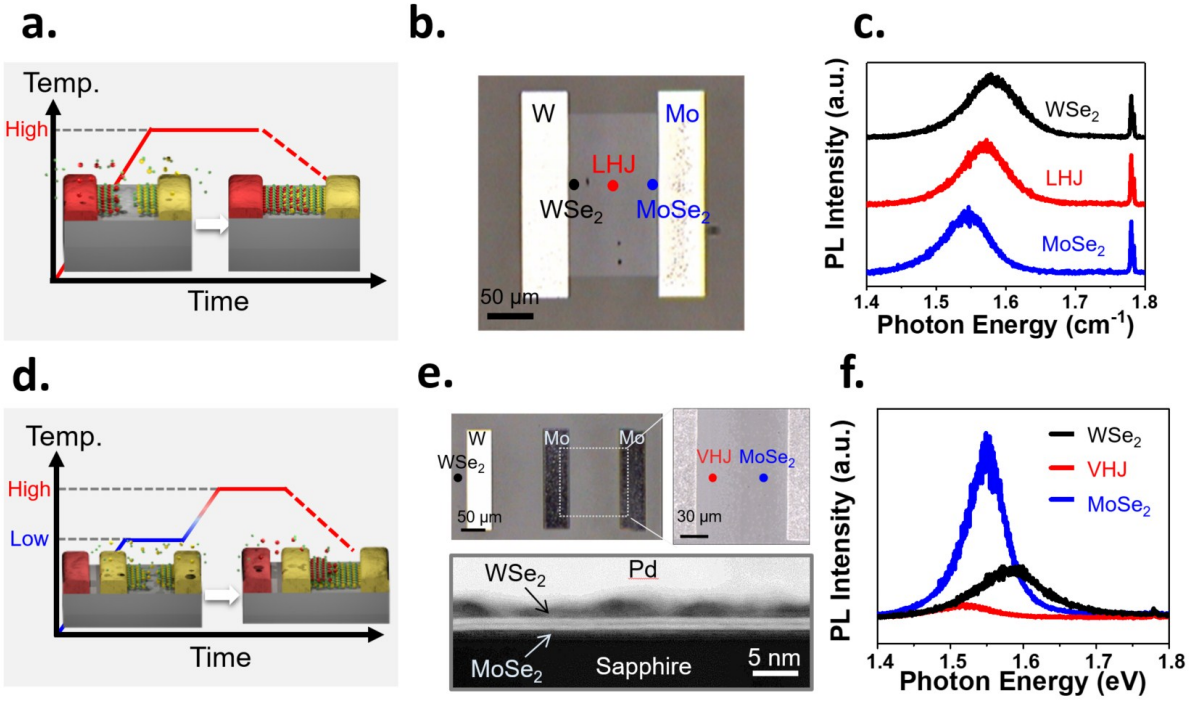

Figure 2. Formation of WSe_2-$MoSe_2$ Heterojunctions in both lateral and vertical fashions through MGSG. (a) Schematic illustration depicts the one-step growth of a WSe_2-$MoSe_2$ LHJ through MGSG. (b, c) Both optical microscope image and PL spectra collectively confirm the formation of ML WSe_2-$MoSe_2$ LHJ between W and Mo metal pads. Meanwhile, the utility of MGSG can be further extended to the growth of ML WSe_2-$MoSe_2$ VHJ through manipulation of growth temperatures as suggested in (d). (e) Optical microscope image along with the cross-sectional STEM image shows the vertical stacking of ML WSe_2 on top of the ML $MoSe_2$. (f) PL spectra taken at the VHJ (red dot at the brighter area in optical microscope image) show substantially quenched intensity accompanied with a red shit in terms of PL peak position as a result of layer-layer interaction.

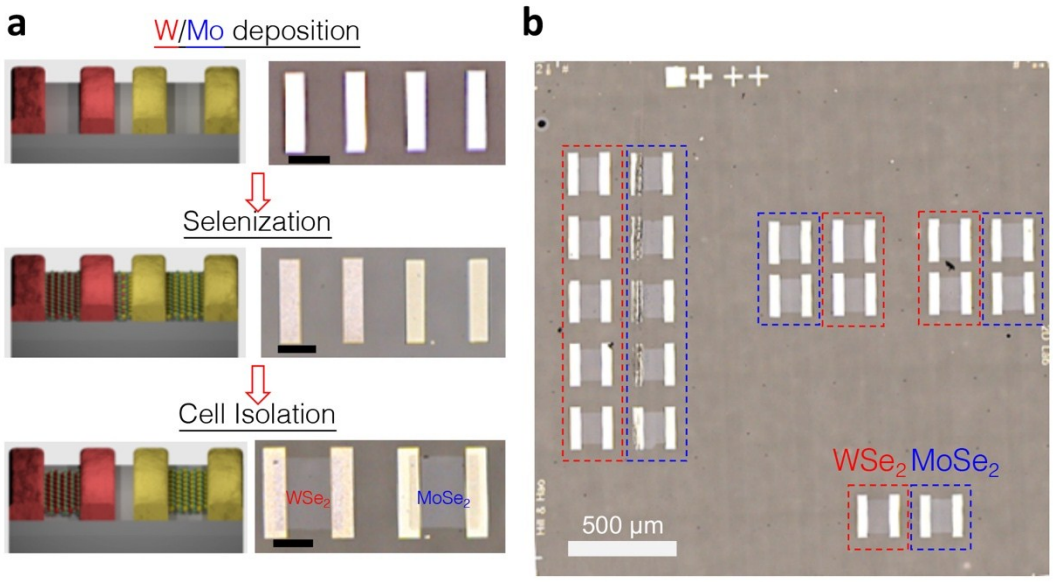

Figure 3. Large-area, location-selective growth of ML TMDs with different metals. (a) Schematic illustrations show the proposed steps for location-selective growth enabled by MGSG. W and Mo metals are photolithographically patterned on desired locations on a sapphire substrate, followed by the concurrent growth of WSe_2 and $MoSe_2$ using MGSG. The cell isolation process was then performed to define the active areas. (b) A representative optical microscope image features an array of well-defined WSe_2 and MoS_2 films grown on sapphire.

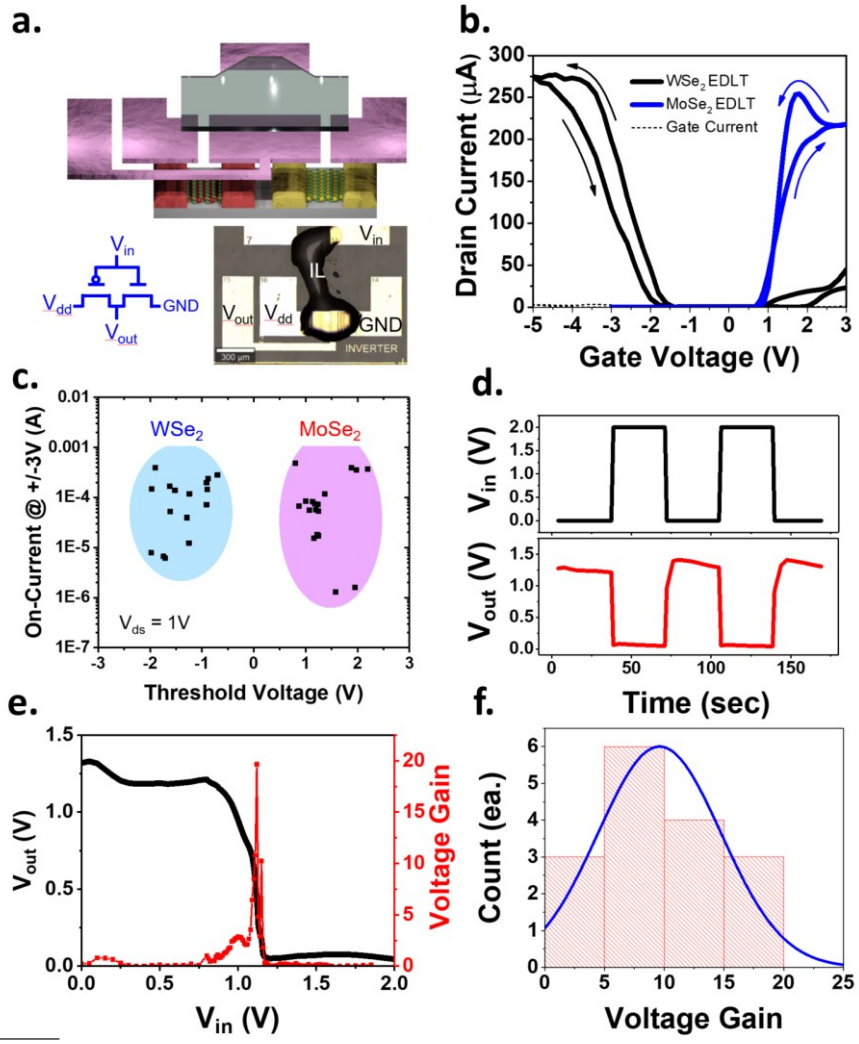

Figure 4. Demonstration of a CMOS inverter. (a) Schematic illustration along with corresponding optical microscope image shows the design layouts of the CMOS inverter built up on ML WSe_2 and $MoSe_2$ grown by MGSG. (b) The transfer curves of electric double layer transistors (EDLTs) of the ML WSe_2 and $MoSe_2$. (c) Statistical plot of ML WSe_2 and $MoSe_2$ transistors with threshold voltage (V_{th}) in x-axis and on-current (V_g = +3 V for $MoSe_2$ and -3 V for WSe_2) in y-axis. (d) A typical inverter characteristic is obtained with V_{in}= 1.5 V, where the measured V_{out} is larger than 1 V at logic state "0", and V_{out} is close to zero at logic state "1". (e) The output voltage dependence on input voltage. A high voltage gain of 19.7 is achieved. (f) Histogram of voltage gain of sixteen CMOS inverters shows a narrow distribution of voltage gain as a result of spatial homogeneity and uniform quality of dissimilar ML TMDs enabled by MGSG. The red curve is the voltage gain distribution probability.

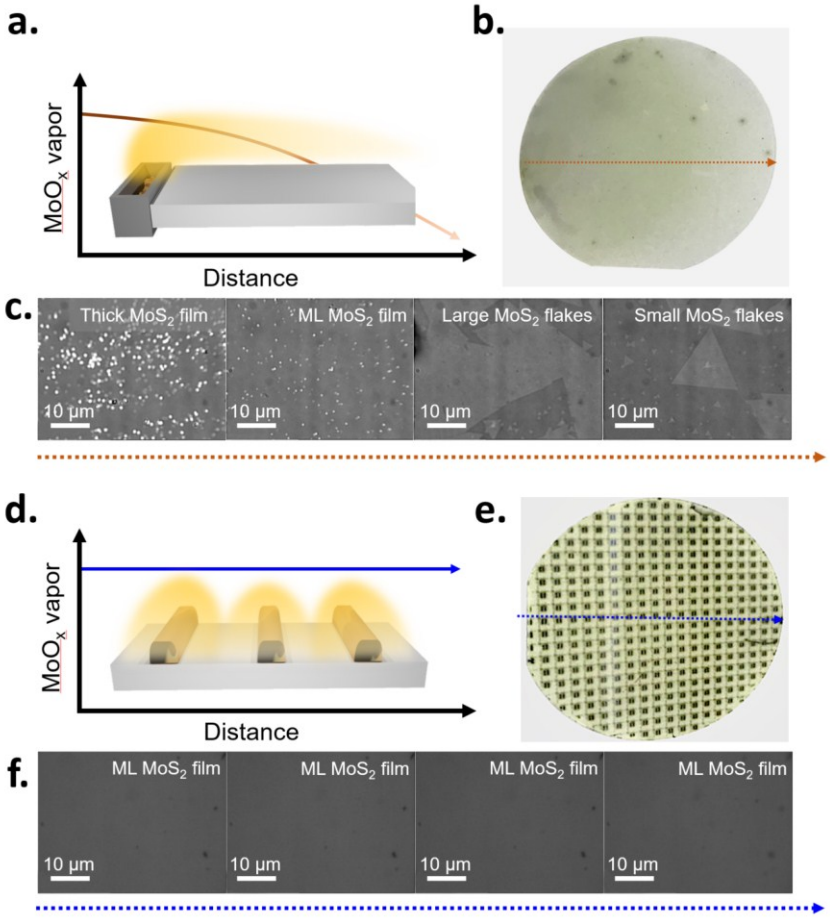

Figure 5. Demonstration of wafer scale growth. (a) Schematic illustration of the conventional CVD process exhibits the decreasing gradient of MoO_2 vapor diffusion with increasing propagation distance. (b) Photograph of MoS_2 films grown on 2-inch sapphire by conventional CVD process. c) A series of optical micrograph images taken along the orange-dash line in (b) reveal thick films, random and isolated flakes of MoS_2. (d) In contrast, MGSG process exhibits a constant diffusion profile of MoO_2 vapor regardless of diffusion distance. (e) Photograph of 2-inch with ML MoS_2 film grown on sapphire by means of MGSG process. f) Corresponding optical microscope images snapped along the blue-dash line in (e) show a uniform and full coverage of ML MoS_2 over the entire area of growth.

Table of Contents

A method to concurrently and location-selectively grow dissimilar transition metal dichalcogenides (TMDs) is revealed. The precise control of transition metal precursor vapor pressure renders the success of lateral and vertical heterojunction growth as well as *p*- and *n*-typed TMDs growth at desired locations, which provides new synthetic strategy for future (opto)electronic applications.

Keyword: transition metal dichalcogenides, two-dimensional materials, tungsten diselenide, molybdenum diselenide, heterojunction, selective growth, chemical vapor deposition

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