Modeling and Simulation of A MEMS Resonator Based Reprogrammable Logic Gate Using Partial Electrodes

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***Abstract*— In this work, we present a reprogrammable micro-resonator logic gate designed with an industrial standard process. The device operation is based on altering the resonance frequency of the beam using DC digital inputs. The proposed design methodology reduces design complexity by 4 to 10 times compared to traditional CMOS design techniques and has great potential for improving energy efficiency. The proposed device has been simulated by MEMS+ software provided by Coventor using XMB10_M30 process design kit (PDK) and then exported into Cadence for further simulations and layout creation following XMB10 process provided by X-FAB.**

Keywords—Electromechanical computation, clamped-clamped beam resonator, electrostatic softening effect, logic gates.

I. Introduction

Micro and Nano-electromechanical systems (M/NEMS) have gained much interest recently after the advancements in micro-fabrication techniques. Although MEMS devices were mainly used in sensors and actuators, mechanical computation using MEMS/NEMS devices has drawn increasing attention in recent years due to their low energy consumption compared to the complementary metal oxide semiconductor (CMOS) based designs [1, 2]. M/NEMS relays are good candidates for ultralow energy consumption due to their zero off-state current. They have been used to implement simple logic gates, complex digital circuits, and I/O interface circuits as well [3-5]. However, they suffer from high contact resistance [6], stiction, and wearing because physical contact is required for closing the switch. The operation of M/NEMS resonators as switches, on the other hand, depends on the amplitude of the vibrating resonator where the 'ON' ('OFF') output state is defined as the on-resonance (off-resonance) signal. Simple logic gates and memory devices have been demonstrated using micro/nano-resonators. One of the interesting aspects of micro-resonator based logic gates is that they are reprogrammable, which means that the same device can be used to perform different functions. For example, a reprogrammable gate that can perform OR and XOR functions was implemented by choosing the vibration mode of the resonator [7, 8]. Other ways have been explored to achieve re-programmability such as tuning the resonance frequency by modulating the stiffness of a resonator beam using direct current flowing through the beam. This technique has been used to implement OR/NOR, XOR/XNOR, AND/NAND, and an inverter using one device [9]. The same technique was used to implement a parity checker and a multiplexer using two devices [10, 11]. However, these devices consume a considerable amount of energy due to the static DC. Therefore, a more energy-efficient way for resonance frequency modulation is to use applying DC voltages on partial electrodes. This technique does not only reduce energy consumption, but it also allows for direct application of the digital signal to the electrodes, thereby eliminating the required switches for the technique used in [9-11].

However, moving forward and building systems based on MEM devices require a standard fabrication process and a package that starts from device modeling, co-simulation with CMOS circuits, building a layout from a drawn schematic, automatic routing, and parasitic extraction. In addition, a standard cell library that consists of micro-resonator gates and blocks must be built. That will create more reliable devices with repeatable characteristics and paves the way for building more complicated systems. In particular, building multi-stage resonator-based circuits is a challenging task as interface circuitry between different resonators is required [8]. These circuits may include amplifiers, buffers, feedthrough signal cancellation circuits, AC to DC converters…etc. In order to implement these interface circuits, it is critical to have a deeper understanding of the electric characteristics of the MEMS resonator. Towards achieving this goal, we used Coventor MEMS+ software [12] to build and simulate the MEMS resonator device using XMB10_M30 PDK. Next, the MEMS+ model is exported into Cadence for further device optimizations, circuit simulations, layout creation, parasitic extraction, and post-layout simulation using XMB10 process [13].

This work is supported by King Abdullah University of Science and Technology (KAUST) office of sponsored research (OSR) under Award No. OSR-2016-CRG5-3001.

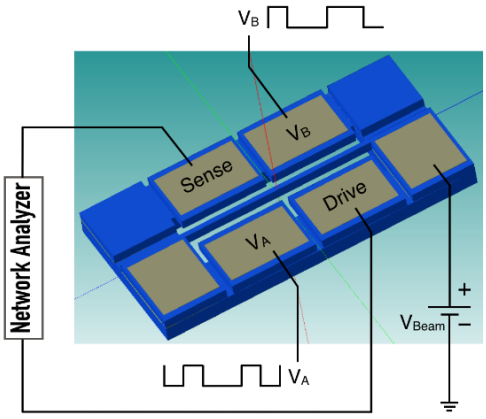

Fig. 1: MEMS+ 3D model for the micro-resonator beam with partial electrodes.

II. Device Structure and Operation

The device consists of a silicon in-plane clamped-clamped micro-beam resonator and two partial electrodes on each side of the beam as shown in Fig. 1. An AC signal is applied to the drive electrode to electrostatically actuate the beam. When the resonance frequency of the beam and the frequency of the applied signal match, the beam resonates, and a relatively high output current is capacitively detected at the sense electrode. The other two electrodes are used for applying the digital DC inputs.

The operation of the device depends on tuning the resonance frequency of the beam by the digital inputs (DC voltages) using the electrostatic softening effect. For the device shown in Fig. 1 with equal air gaps between the beam and the side electrodes, three different frequencies (f_1, f_2, f_3) can be obtained by applying digital inputs "00", "01/10", and "11" respectively with V_A and V_B. If the frequency of the drive signal is fixed to f_1, only the "00" input combination leads to a match between the resonance frequency of the beam and the drive signal frequency, which correspondingly causes resonance, and a 'high' output signal is detected. The rest of the cases will result in a 'low' output. Hence, the resonator, in this case, works as a NOR gate. Similarly, by applying f_2, the resonator works as an XOR gate, and applying f_3 reprograms the resonator work as an AND gate.

The concept was analytically modeled and experimentally verified in [14] with a device built using surface micromachining techniques in KAUST nanofabrication facilities; however, the device was not sealed. Thus, all the testing had to be performed in a vacuum chamber, which leads to a constraint on the number of input/output ports that can be used, limiting the testing to a single device. In contrast, XMB10 process creates an industrial level, vacuum sealed devices that can be tested in the air without restrictions on the number of I/O ports. In addition, a large, deep cavity under the moving beam is included, which is expected to significantly decrease the feedthrough signal from the drive to the sense electrode; hence it maximizes the signal to noise ratio (SNR), which is a major challenge of this type of resonators.

III. Device Simulating in MEMS+

The device was simulated in MEMS+ using XMB10_M30 PDK. To build our device, the beam is created using a beam component with Timoshenko model. The partial electrodes were constructed using four side-gap components. In order to define the beam's anchors and the cavity dimensions under the beam (which allows the beam to move), solid frame components were used. In addition, metal contacts were used on the electrodes and the anchors of the beam in order to provide electrical connectivity. The created MEMS+ device is shown in Fig. 1. After that, mechanical and electrical connectors were connected. Different simulations were carried out in MEMS+. First, a modal analysis was done to identify the resonance frequency of the beam for the four different input combinations, where the digital '1' voltage is 25V and digital '0' voltage is 0V. Next, AC responses using frequency sweeps around the identified resonance frequencies were done as shown in Fig. 2. The "00" case resulted in a resonance frequency at 167 kHz (NOR gate frequency of operation). The "01" and "10" cases resulted in a higher frequency at 173.4 kHz, while the "11" case resulted in 182 kHz resonance frequency. The separation between these frequencies depends on the beam DC bias, digital "1" and digital "0" values, and the stiffness of the beam.

In addition, pull-in analysis was carried out for the four different combinations as shown in Fig. 3. The values for digital '1' and digital '0' were fixed to 25V and 0V respectively, and only the beam bias was varied. The beam does not pull-in if "00" or "11" combinations are applied

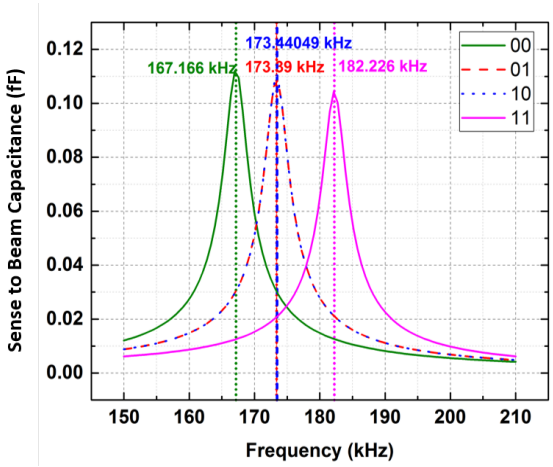

Fig. 2: The frequency response of the micro-resonator for different input combinations. The beam length, width and beam/electrode air gaps of the optimized device are 300 µm, 2 µm, and 2 µm. Digital '1' is 25 V, digital '0' is 0V, and the beam is biased with 30V.

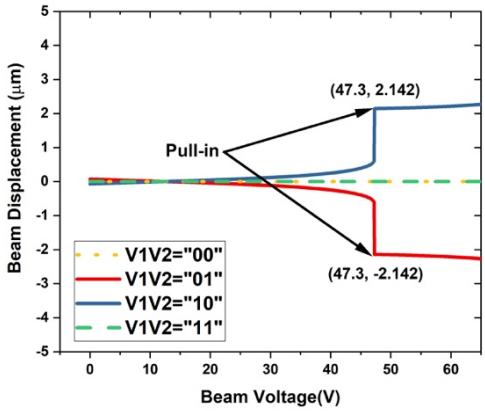

Fig. 3: The pull-in analysis for the micro-beam resonator under different input combinations.

since these combinations create equal and opposite forces from both sides of the beam. However, pull-in occurs for the beam towards the electrode with lower potential, i.e., where '0' is applied, for the "01" and "10" cases, due to the higher electrostatic force between the beam and that electrode.

IV. Device Simulation in Cadence Virtuoso

A. Device Dimensions Optimization

After creating a model for the micro-resonator device in MEMS+, the model is exported into Cadence for further simulations and layout finishing. First, a test bench is created using the imported resonator model, as shown in Fig. 4. The device dimensions were optimized, using the AC frequency response, to get the maximum separation between the different peaks. First, the beam length was fixed to 300 µm, digital '1' to 25V and the beam bias to 30V. The beam width was then varied between 4, 3 and 2 µm. As shown in Fig. 5, the resonance frequency decreases and the separation between the peaks for the different input combinations increases for smaller beam widths (due to lower beam stiffness). Therefore, the beam width is chosen to have the minimum allowed size, which is 2 µm according to XMB10 design rules. After that, the air gap between the beam and the partial electrodes is varied while fixing the beam's width to 2 µm. Fig. 6 shows that smaller beam/electrodes air gaps result in larger frequency separations between the different peaks due to the higher electrostatic filed (stronger electrostatic softening effect). In addition, a higher output voltage is detected for smaller air gaps as the electromechanical coupling coefficient increases for smaller air gaps. By minimizing the beam width

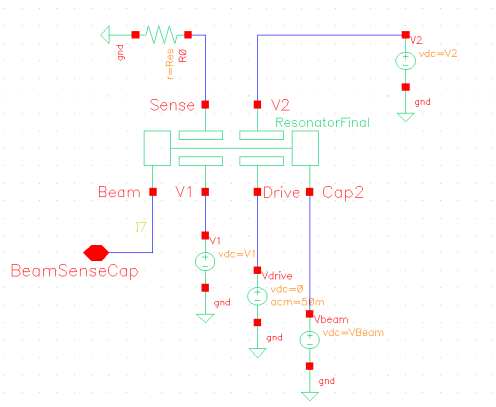

Fig. 4: Test bench for the resonator in Cadence Virtuoso using the micro-resonator model imported from MEMS+.

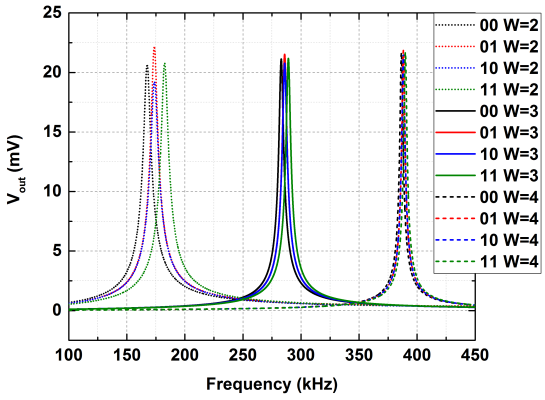

Fig. 5: The effect of varying the beam width on the frequency separation between the different peaks.

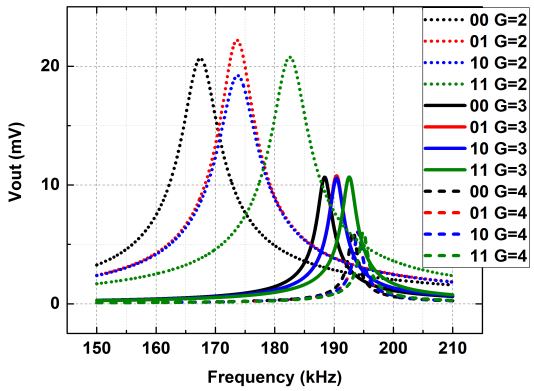

Fig. 6: The effect of varying the air gap between the beam and the partial electrodes on the frequency separation between the different peaks.

and the air gap, higher separations between the different peaks are obtained, which is important to ensure the correct functionality of the device as a reprogrammable logic gate. Also, this gives more room for reducing the used voltages, which leads to lower energy consumption.

B. Transient Analysis:

A transient analysis was performed to verify the functionality of the device. The drive signal frequency was fixed at the frequency of the AND gate (182.226 kHz from Fig. 2) while varying the inputs A and B. As shown in Fig. 7, the amplitude of the sense signal (yellow) is relatively large (digital '1') when both inputs A (red) and B (green) are '1' while the rest of the cases gives a relatively lower output (digital '0'). The functions of NOR and XOR were also verified by fixing the frequency of the drive signal to 167 kHz and 173.4 kHz respectively, but not shown here for brevity.

V. Layout Creation and Post-Layout Simulation in Cadence Virtuoso

After finalizing the dimensions, the layout is created using XMB10 utilities in Cadence Virtuoso Layout Suite starting from the initial layout imported from the MEMS+ model. XMB10 technology provides pre-built components that can be instantiated directly and the dimensions can be adjusted automatically, which helps in minimizing design rule errors when creating the MEMS device layout.

The final double chip layout that is compatible with the XMB10 technology is shown in Fig. 8. Next, the coupled parasitic capacitances are extracted to study their effect on the resonator's output. Among those parasitic capacitances, the one between the drive and sense electrodes has the most significant impact on the resonator's output. Due to the lossy nature of these resonators, the output signal that results from resonance (motional signal) is usually much smaller than the

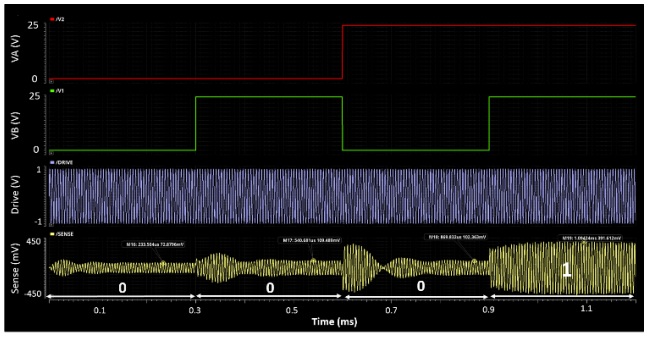

Fig. 7: Transient analysis of the AND gate where V_A and V_B are the DC inputs, the drive signal is a sine wave with frequency fixed at 182.226 kHz.

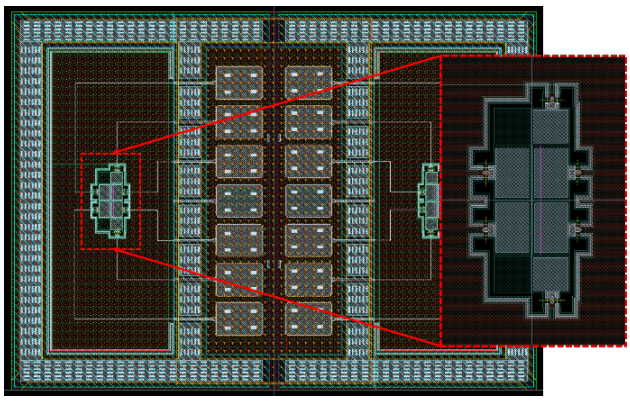

Fig. 8: The double chip layout created in Cadence using XMB10 process.

feedthrough signal from the drive to the sense electrodes that it could be totally masked out. However, XMB10 process provides a deep, wide cavity under the beam which, to our knowledge and as the layout extraction tool suggests, will help in minimizing the capacitances between the drive and sense electrodes. In addition, the diagonal configurations of drive and sense electrodes plays a role in minimizing the feedthrough signal. After finishing the layout, we could access the parasitic capacitances of each electrode. However, due to the inexistence of universal power supply V_{DD} in the resonator design, as well as the non-detectable parametrized cell (Pcell) on the sealed layout, CMOS alike parasitic extraction is not supported by the PDK in this case.

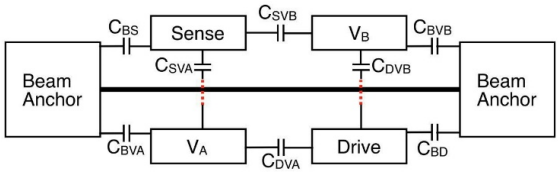

Fig. 9: A circuit schematic showing the parasitic capacitances' locations in the resonator.

TABLE 1. EXTRACTED CAPACITANCE VALUES

Capacitance Name	Value	Capacitance Name	Value
Beam to Drive (C_{BD})	9.594 fF	Drive to V_A (C_{DVA})	2.21 fF
Beam to Sense (C_{BS})	6.329 fF	Drive to V_B (C_{DVB})	1.172 fF
Beam to V_A (C_{BVA})	9.594 fF	Sense to V_A (C_{SVA})	1.172 fF
Beam to V_B (C_{BVB})	6.329 fF	Sense to V_B (C_{SVB})	2.216 fF

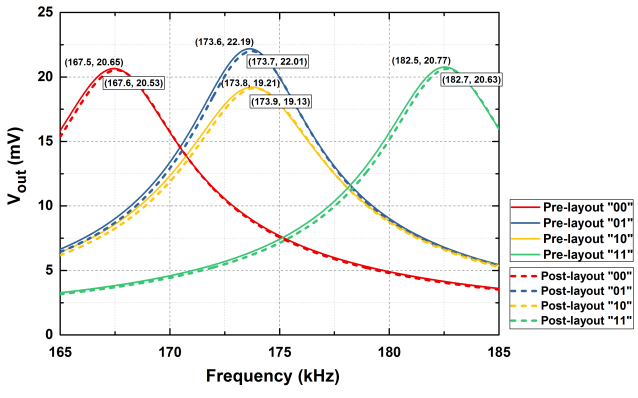

Fig. 10: The pre-layout and post-layout output comparison.

Therefore, we used a pseudo-schematic to make the layer versus schematic (LVS) run and assigned the beam, which connects to a fixed DC source, as the reference. Subsequently, additional capacitors with values obtained from Quantus QRC extraction are added to the schematic for post-layout simulation. The schematic, shown in Fig. 9, shows the existing parasitic capacitances in the resonator devices and table 1 shows their extracted values. Fig. 10 compares the pre-layout and post-layout frequency responses. The resonance frequencies slightly shifted due to coupled capacitance; however, the shift is not significant and can be ignored. There is no extracted value for the capacitance between the drive and sense as the extraction happens between the metal interconnects only, without considering the leakage through the substrate. The resonator model could be adjusted to account for this based on further measurement results.

VI. DISCUSSION

Designing logic gates and circuits based on micro- or nano-resonators have some appealing aspects but also some trade-offs. The attractive aspects include run-time re-programmability, reduced complexity, and potentially low energy consuming logic circuits compared to its CMOS counterpart. Some of the limitations are speed and the required signal conditioning circuits.

Run-time re-programmability allows using the same hardware to implement different functions, which can lead to minimizing the overall footprint of the system when using nano-scale resonators. Table 2 compares the number of required CMOS transistors and resonators to implement NOR gate, AND gate, and a full adder [15]. Using electromechanical resonators can reduce digital design complexity by 4 to 14 times compared to traditional CMOS designs. Regarding area consumption, the dimensions of the device determine the overall area. Although micro-scale resonators are bulky in general, nano-resonators can reduce area consumption. For example, the nano-resonator based full adder in [15, 16] is 45 times smaller than a CMOS mirror adder in 65nm Technology. In addition to reduced complexity, the proposed micro-resonator based gates are expected to have lower energy consumption due to the absence of direct currents, only switching energy, and AC activation energy are involved as discussed in details in [14].

The switching speed of micro-resonators is critical to circuit operations. In general, the speed of any device that involves mechanical motion is much lower than the speed of electronic devices. MEM resonators are not designed to compete with CMOS in this regard. However, they fit the applications that require low energy consumption and low-to-moderate speeds like the internet of things (IoT) devices [17]. The required transition time (ts) for a resonator to switch between two states depends on the quality factor Q and the resonance frequency fs (ts= Q /fs) [18].

TABLE 2. COMPARISON BETWEEN THE NUMBER OF REQUIRED DEVICES USING CMOS TECHNOLOGY AND M/NEM-RESONATORS.

Technology	NOR		AND		Full Adder
	2 bit	*4 bit*	*2 bit*	*4 bit*	
CMOS Transistors	4	8	6	10	28
M/NEM Resonators	1	1 [15]	1	1 [15]	2 [15]

From the transient analysis in Fig. 7, the transition time is around 0.1ms, which corresponds to Q of 27 and speed of 10 kHz. The simulation was done at a pressure of 800 Pa. The quality factor is determined by the losses in the system that include viscous losses, anchor losses and material losses [19]. Viscous losses (air damping) is a function of the device dimensions, the separation between the moving part and the fixed part(s), and air (fluid) pressure. At low pressure, viscous losses are minimized, and other kinds of losses take over. Indeed, by simulating our resonator at different pressures starting from 800 Pa down to 1 Pa, no considerable difference is noticed in the value of Q. In general, increasing the speed of the resonator can be achieved by designing the resonator to work at high frequency and moderate quality factor. There are many factors to be considered for the appropriate value of Q. One of them is the separation between the different peaks. For high Q resonator, the frequency separation can be minimized which reflects lower energy consumption as the digital '1' voltage does not have to be big. However, that also leads to lower switching speed. On the other hand, if Q is low, the device will switch faster, but higher voltages (both the beam bias and the voltage value for a digital '1') will be required to make sure that the frequency separation between the different peaks is enough for correct operation and also to increase the signal to noise ratio. Therefore, micro-resonator logic gates should be designed, and the operating conditions should be optimized based on the application.

Another important aspect is the required signal conditioning circuit for micro-resonator based logic circuits. In the proposed device, the digital inputs are DC voltages while the output is an AC signal. Therefore, a circuit is required to rectify the output signal and amplify it to prepare it for the next stage. Rectification can be eliminated by unifying the input and output signal types [8]. The amount of required amplification can be minimized by using termination resistors with values close to the motional resistance of the resonator as discussed in [8]. Other aspects like frequency stability and temperature stability have been studied in [14].

VII. Conclusion:

Modeling, simulation, and layout creation of a micro-resonator based reprogrammable logic gate in a standard XMB10 process were done using Coventor MEMS+ and Cadence Virtuoso. The final device layout was created in Cadence using XMB10 utilities provided by X-FAB. This work paves the way for design and simulation of hybrid/integrated MEMS and CMOS circuits in the future.

Acknowledgment

The authors would like to acknowledge the technical support from Coventor, Cadence, and X-FAB during MEMS Design Contest 2018. The authors would like to thank Saad Ilyas and Mohammad Younis from the Physical Sciences and Engineering division (PSE) at KAUST for their feedback.

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