A Wideband Fully Planar Vivaldi Antenna for WPAN Applications

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***Abstract*— The availability of large bandwidth in the ISM band around 60 GHz is very useful for data hungry applications such as WPAN. Being allocated as an ISM band, several research papers have been published on completely integrated RF systems using CMOS technology. Although the circuits for these implementations have been realized on silicon, the antennas are usually done off-chip. The reason is the lossy nature of the silicon substrate for RF frequencies. Instead of using resonant antennas, if travelling wave antennas are used for such an application then a better efficiency can be achieved from such designs. In this work, a fully planar Vivaldi antenna is reported on 65 nm CMOS stack up. For the first time, the feed of the antenna is integrated on the same conductor layer as the antenna itself. Using this design technique the problem of thin gap between the metal layers have been mitigated. The final simulations show that the antenna covers the complete ISM band and works well from 57 GHz to 66 GHz. The gain of the antenna is -3dBi. The results show that the design is quite suitable for integration in a millimeter range transceiver for short range wireless communication.**

Keywords—Vivaldi, CMOS, TSA, WPAN

I. Introduction

Growing interest in Wireless Personal Area Network (WPAN) applications is due to its ability to support high data rates. However, higher data rates require radio frequency (RF) components that are wideband. For this purpose, the unlicensed band around 60 GHz has been used by the researchers to demonstrate various microwave antennas that show large impedance bandwidth [1-3]. A popular candidate for WPAN application is Vivaldi or Tapered Slot Antenna (TSA) [4], [5]. The reason being the ability of such an antenna to provide large impedance bandwidth while maintaining excellent gain and efficiency performance. However, all these designs have been reported on package or in other words off-chip.

The challenge in designing Vivaldi or TSA antenna on Complementary Metal Oxide Semiconductor (CMOS) is the requirement of two different metal layers with certain spacing between them. To understand this, let's consider the two most commonly used methods for the design of these antennas: 1) antipodal antenna design which needs two conductor layers for each antenna arm 2) single layer antenna design which has both arms on one conductor layer but needs a bottom conductor layer for the microstrip feed line. The two feed implementations are shown in Fig. 1. For both these designs there should be a certain gap between the top layer and the bottom layer to excite the proper traveling mode of the antenna. Thus a certain thickness of substrate is required. However, in CMOS process the gaps between successive metal layers is quite small (usually 1-3 μm) [6]. This value of thickness is not appropriate for any of the two designs shown in the above figure.

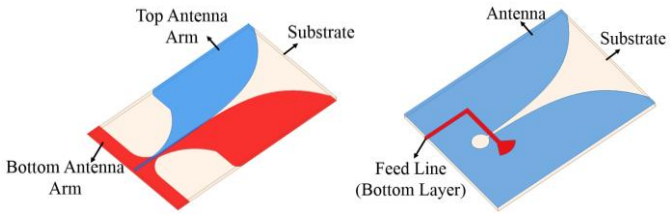

Fig. 1 Vivaldi antenna (a) antipodal design (b) single layer design

To resolve the problem, a fully planar TSA antenna is presented in this work on 65 nm CMOS stack up. To achieve this, the transition of coplanar waveguide (CPW) feed line to an aperture/slot is employed herein [7]. Initially, the transition is simulated in a back-to-back configuration to improve the impedance match and the insertion loss for the desired frequency band. The feed transition is then integrated with the non-linearly tapered antenna. The final simulated antenna shows an impedance bandwidth of 9 GHz (57 GHz to 66 GHz) with a maximum gain of -3 dBi. The antenna results thus obtained show that the design is highly suitable for integration in a CMOS transceiver design for WPAN applications.

II. CMOS Stack Up

CMOS process used for the design of the antenna is provided by TSMC in 65nm technology. The stack up is shown in Fig. 2. It can be seen that the process consists of 9 metal layers with variable thicknesses and dielectric constant of the insulating layer. The gap between metal layers M1 and M9 is approximately 5μm. This is the maximum distance that can be used between the two layers of the Vivaldi or TSA antenna shown in Fig. 1. When the antennas are simulated using this gap (in Ansys HFSS), it is seen that the travelling mode cannot be excited properly. As a result the antenna does not provide a good end-fire radiation. Thus, it can be concluded that for such a stack up a fully planar antenna is required.

III. CPW to SLOT Transition

Due to the limitation of the available gaps between the metal layers of a CMOS process, it is required that the feed line of the

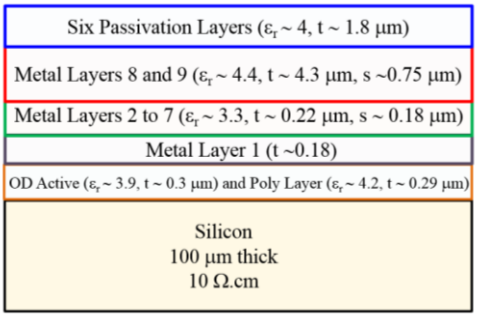

Fig. 2. CMOS Stack up for TSMC 65 nm technology

antenna should be integrated in the same conductor/metal layer as the antenna itself. To accomplish this a transition from CPW to slot is needed. CPW feed line is chosen because of its single layer implementation. One such transition is shown in Fig. 3 [7]. The transition consists of a CPW feed line which excites a slot that makes a right angle with the feed line. Interestingly, the feed line is extended beyond the slot for a quarter-wavelength. The edge of the feed line is left open due to which near the slot a short circuit impedance is established (quarter wave transformation). This allows for maximum coupling of RF signal from the CPW feed into the slot. To further improve the matching of the transition, a slot matching stub is placed at the back of the point where short circuit is established. The transition is simulated around the center frequency of 60 GHz. The impedance of the CPW line is 50 ohm, while the width and the length of the slot can be optimized for best possible RF response. The simulated feed transition provides a 9 GHz bandwidth around center frequency of 61.5 GHz with an insertion loss of 1.1 dB. Considering the lossy nature of silicon, this value of insertion loss is more than acceptable. Once the feed transition has been optimized it can now be integrated to the antenna.

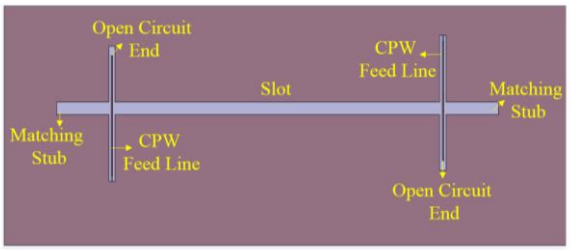

Fig. 3. Back-to-back CPW to slot transition

IV. Antenna Desin

Using one half of the transition explained in the last section, the Vivaldi antenna is excited as shown in Fig. 4. The design is completely planar which means there is no need of two different metal layers. Both the antenna and the CPW feed are implemented on the same metal layer, i.e. M9. It is worth mentioning here that the width of the slot in the case of the antenna is not uniform as opposed to the feed transition. To cater for this mismatch, the slot matching stub at the back of the antenna is used. It helps to improve the impedance matching of the antenna and at the same provides a better front-to-back ratio. The complete antenna design occupies a space of 1.73 mm × 1.75 mm. The antenna demonstrates a maximum gain of -3 dBi. The low gain and the efficiency of the design is due to the loss of the silicon substrate. This value of the antenna gain is in acceptable range. Furthermore, the WPAN application is usually employed in short range wireless communications (~1-2 m). The simulated 3D radiation pattern and the impedance performance of the antenna are shown in Fig. 5 and Fig. 6 respectively. A directional radiation performance can be observed from the results with excellent matching conditions in the required frequency band.

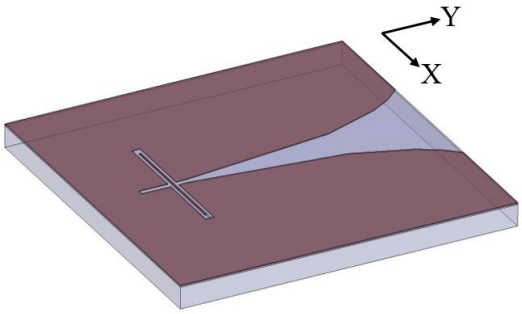

Fig. 4. Fully planar Vivaldi antenna with CPW to slot transition.

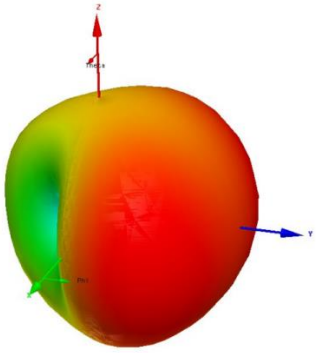

Fig. 5. Simulated 3D radiation pattern of the antenna

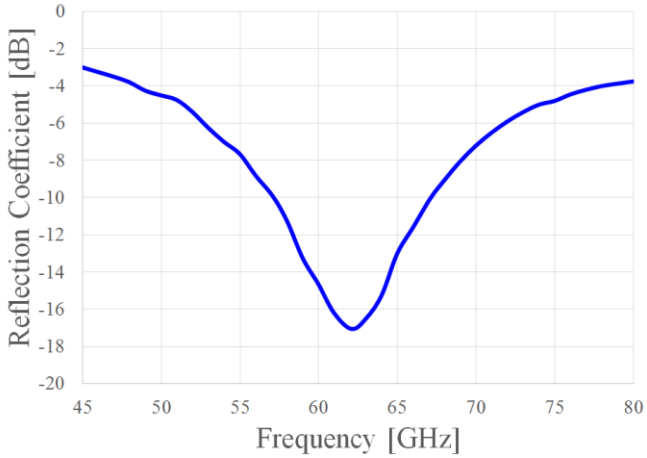

Fig. 6. Simulated impedance performance of the antenna

Conclusion

The paper presents the design of a completely planar Vivaldi/TSA antenna on silicon substrate. The simulated results show that the design can easily cover the bandwidth requirements of the WPAN applications. The gain of the antenna is on the lower side but considering the range requirement of these applications its efficiency can be considered acceptable. The impedance and radiation performance of the antenna make it easily integrable with millimeter wave circuits realized using the CMOS technology.

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