

StrongARM Latch Comparator Performance Enhancement by Implementing Clocked Forward Body Biasing

Abdullah Alshehri*, Mohammed Al-Qadasi, Abdullah S. Almansouri, Talal Al-Attar and Hossein Fariborzi
 Computer, Electrical and Mathematical Science & Engineering Division
 King Abdullah University of Science and Technology (KAUST), Thuwal, Saudi Arabia
 * Email: abdullah.alshrhi@kaust.edu.sa

Abstract—In this paper, we propose a forward body biasing technique to enhance the performance of the StrongARM comparators. We apply this technique, which is mainly based on clocked tuning of the threshold voltage of the NMOS cross-coupled transistors, to different architectures, namely: Kobayashi, Razavi, and Improved StrongARM comparators. The circuits are simulated in the standard 65nm CMOS technology and performance improvement of up to 20.8% has been achieved while maintaining the same energy loss.

Keywords—StrongARM, Forward body biasing (FBB), comparator, high-speed latch, threshold voltage.

I. INTRODUCTION

With the growing demand for wearable electronics and personal communication systems, increasing the performance of the electronic circuits while reducing the power consumption have become a significant need for the integrated circuit (IC) design. One way to lower the power consumption is achieved by lowering the supply voltage, however, this will degrade the overall performance of the circuit [1].

In order to overcome this issue and boost the performance of the circuit, transistors with lower threshold voltage are used [2]. However, by lowering the threshold voltage, the transistors off-state leakage current increases. In general, the minimum value of the threshold voltage is set by the amount of off-state leakage current that can be tolerated [3].

Forward Body Biasing (FBB) is a standard technique that is used to lower the threshold voltage of a transistor during operation and improve the switching speed. An example application of FBB is the Dynamic Threshold-Voltage MOSFET (DTMOS) as shown in Fig. 1(a). In this example, the threshold voltage is a function of its gate voltage, as the gate voltage increases the NMOS threshold voltage (V_{thn}) drops, and as the gate voltage decreases the PMOS threshold voltage (V_{thp}) drops resulting in a much higher current drive than standard MOSFET for low power supply voltage [4]. Another FBB example is the Swapped-Body Biasing (SBB) configuration. In this configuration, shown in Fig. 1(b), the body of NMOS is connected to V_{DD} terminal and the body of PMOS is connected to ground terminal. Therefore, the body terminal voltages of the NMOS and the PMOS are $V_{bn} = V_{DD}$ and $V_{bp} = 0$, respectively, so that both transistors are constantly forward biased [5].

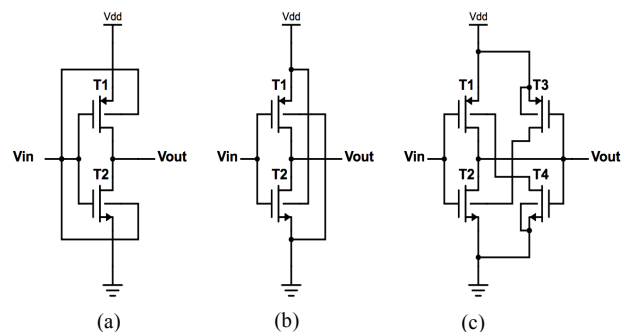


Fig. 1. Forward Body Biasing (FBB) inverters. (a) DTMOS [4] (b) SBB [5] (c) Novel FBB [6]

Another FBB example is introduced in [6], this technique achieved by dynamically lower the threshold voltage of a transistor as shown in Fig. 1(c). The bodies of PMOS (T1) and NMOS (T2) are biased by the drain voltages of the minimum sized auxiliary PMOS (T3) and NMOS (T4), respectively. When the input voltage is high, the output voltage is low, therefore T3 is on and reduces the threshold voltage of T2. On the other hand, when the input voltage is low, the output voltage is high, therefore T4 is on and reduces the threshold voltage of T1. These techniques effectively improve the performance, suppresses short channel effects, and limits the threshold voltage variation [7, 8]. However, they are limited to low power application.

Analog to digital converters (ADCs) are essential blocks in integrated systems. The StrongARM latch is one of the most popular dynamic comparators used in the ADCs as it consumes virtually zero static power and hence is an energy efficient solution. Also, it directly provides a rail to rail output, has small input referred offset and has high input impedance [10]. The basic configuration of the StrongARM was introduced by Kobayashi back in 1993 [9] and eventually got improved by [10, 11].

In this paper, we apply a clocked forward body biasing (CFBB) technique to dynamically change the threshold voltage of the critical transistors of the StrongARM. This way, the performance of the StrongARM design is boosted without significant impact on its energy efficiency. Three major StrongARM topologies are enhanced with our CFBB technique and their overall performance and power dissipation are evaluated before and after the enhancement.

II. CONVENTIONAL TOPOLOGY

The original StrongARM has 9 transistors as shown in Fig. 2. It consists of NMOS and PMOS cross-coupled transistors (T1, T2, T3, and T4), differential input pair (T5 and T6), two charging transistors (CT1 and CT2) and a tail transistor (T7). The StrongARM operates in three main phases: Reset, Amplification, and Regeneration, as illustrated in Fig. 3. In the Reset phase, the clock goes low, turning CT1 and CT2 on to charge nodes A and A' to V_{DD} , while T7 is turned off. In the Amplification phase, the clock goes high, turning CT1 and CT2 off and turning T7 on. Since T5 and T6 are biased by a constant common mode voltage (V_{CM}), the nodes A and A' will discharge through T7. Due to the small difference between the gate voltages of T5 and T6 (V_{diff}), one of the nodes A or A' will discharge faster (in this case node A, assuming $V_{diff} > 0$). When the voltage at node A drops below ($V_{DD} - V_{thp}$), T2 will turn on, forcing T1 to turn off while T3 is on. This is effectively the onset of the Regeneration phase. After some time, node A will go below V_{thn} causing the T4 to turn off. Eventually, node A will reach zero and node A' will reach V_{DD} . This scenario is reversed if the V_{diff} is negative.

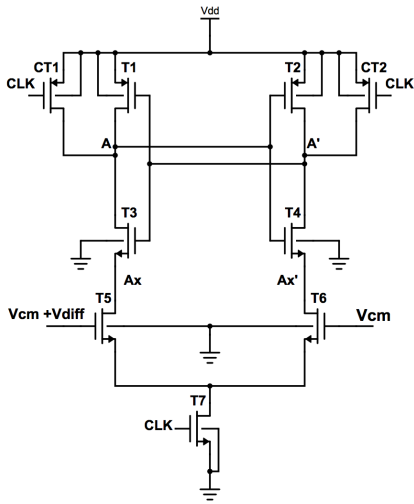


Fig. 2. The Kobayashi original StrongARM latch [9]

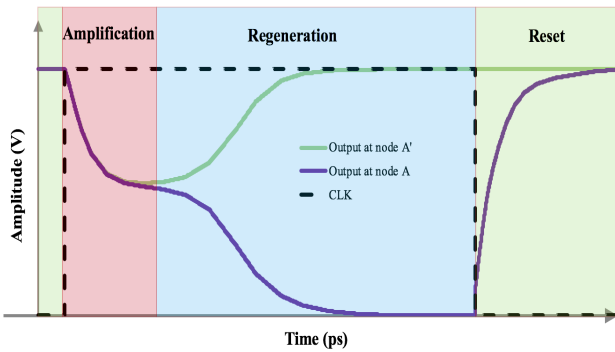


Fig. 3. The three different operation phases for the StrongARM; Amplification, Regeneration and Reset phases. [11]

III. PROPOSED DESIGN

In the proposed design, a clock-driven FBB PMOS transistor is used to connect the body terminals of the NMOS cross-coupled transistors (T3 and T4) to V_{DD} , as shown in Figs. 4-6. When the clock is low, the CFBB transistor is turned on, hence, the bodies of T3 and T4 will be charged to V_{DD} . This voltage reduces the threshold voltage of both transistors and makes the operation faster. When the clock goes high, the CFBB transistor turns off and the body voltage will experience capacitive voltage divider mostly into the internal capacitors of T3, T4, and T8. The optimum body voltage value during the regeneration phase can be achieved by carefully selecting the dimensions of T3, T4, and T8. The transistor sizes were design to ensure that the source-body voltage (V_{bs}) does not exceed 0.6V in order to avoid the latch up issue and current leaking which affects the circuit operation [12]. Fig. 7 shows the V_{bs} of T3 and T4 for Razavi and Kobayashi StrongARMs with CFBB transistor.

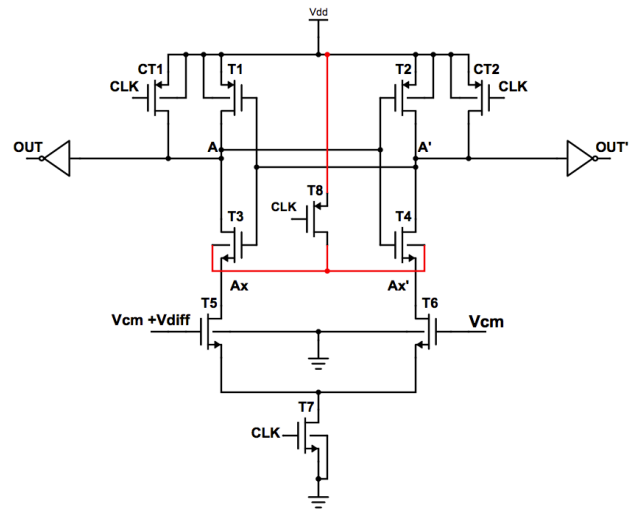


Fig. 4. CFBB transistor connected to the Kobayashi StrongARM latch [9]

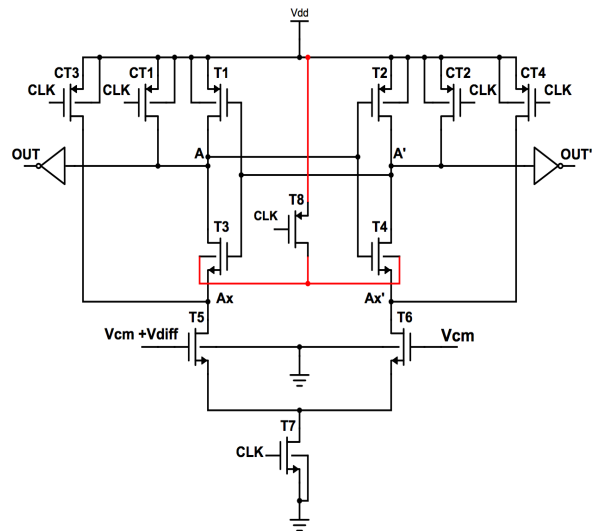


Fig. 5. CFBB transistor connected to the Razavi StrongARM latch [10]

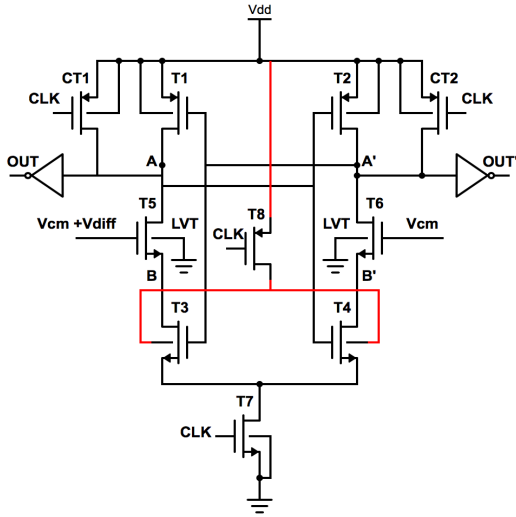


Fig. 6. CFBB transistor connected to the Improved StrongARM latch [11]

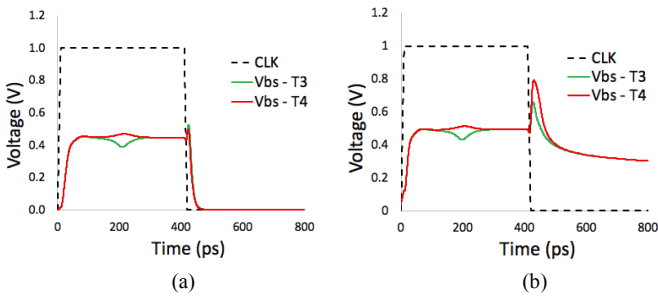


Fig. 7. The Source-Body Voltage (V_{bs}) for T3 and T4. (a) Razavi StrongARM (b) Kobayashi StrongARM

It is worth mentioning that during the amplification and reset phases the risk of latch-up will be very low since the voltage of nodes A_x and A_x' is relatively high. Unlike most of the FBB approaches in the literature, in the proposed design the threshold voltage is independent of input and outputs.

IV. RESULTS AND DISCUSSION

Fig. 8 and 9 show the performance simulation results for Kobayashi and Razavi StrongARM comparators, respectively, with and without utilizing the CFBB technique in 65nm CMOS technology. The differential voltage (V_{diff}) are 1 mV and 10 mV respectively, and the common mode voltage (V_{CM}) is 0.7 V. When the clock is low, the body voltages of the NMOS (T3 and T4) are charged to V_{DD} through the CFBB transistor (T8) which provides strong V_{DD} . As soon as the clock goes high, the clock-feedthrough introduces a spike in the body that enhances the performance of the NMOS transistors. Eventually, T8 will switch off and the body voltage drops to around 0.5V and 0.45V. During this time, the body voltage of T3 and T4 will be at the maximum and will speed-up the amplification phase. The most critical interval which decides the performance of the comparator extends from the beginning of the clock until the splitting of nodes A and A'.

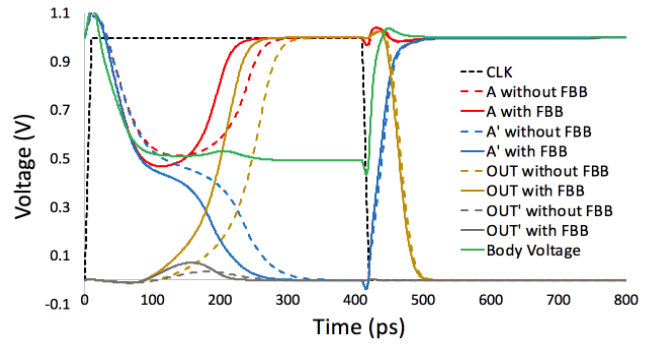


Fig. 8. Time Response for Kobayashi StrongARM with and without CFBB.

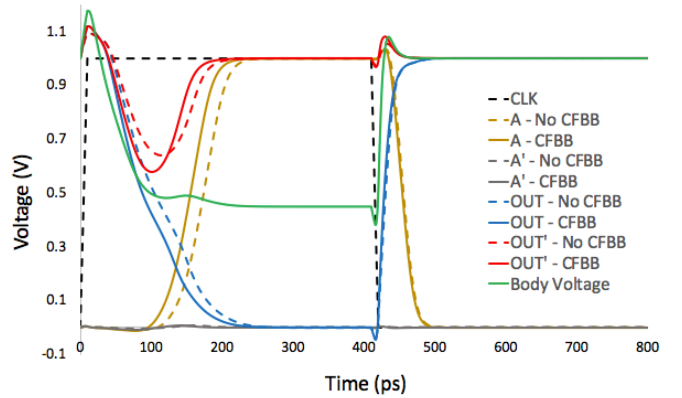


Fig. 9. Time Response for Razavi StrongARM latch with and without CFBB.

In Fig. 10, the input differential voltage is swept between 1 mV and 100 mV for all different topologies with and without the CFBB transistor. Not surprisingly, the performance of all StrongARM comparators is enhanced when the input differential voltage increases. The CFBB technique has a significantly higher impact on the speed when the input differential voltage is small. While all three topologies benefit from the CFBB scheme, Kobayashi StrongARM experiences the highest performance enhancement for the whole range of V_{diff} .

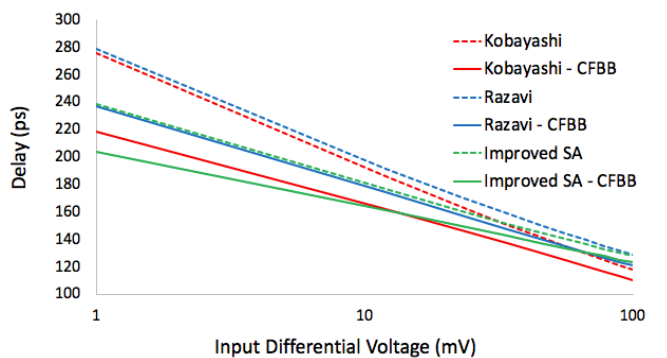


Fig. 10. StrongARM latch speed with and without the CFBB scheme

V. CONCLUSION

In this work Clocked Forward Body Biasing (CFBB) technique is implemented to improve the performance of three different StrongARM architectures by lowering the threshold voltage of the NMOS transistors in the cross-coupled inverters during the critical operation phase of the circuit. We show that the performances of the Kobayashi, Razavi and Improved SA comparators are improved by 20.8%, 14.9%, and 14.7%, respectively, without significant adverse effect on the power consumption.

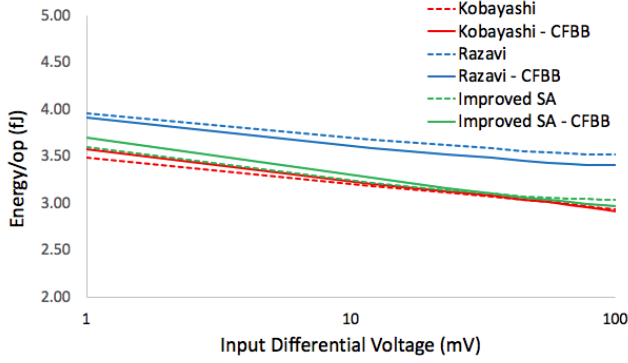


Fig. 11. StrongARM latch Energy consumption with and without the CFBB scheme

Fig. 11 shows the energy consumption per operation for all topologies with and without the CFBB technique. The energy has insignificant impact when applying the CFBB technique over the entire period.

Table I and Table II show the performance and energy consumption for the three StrongARM comparator topologies when V_{diff} is 1 mV and 10 mV, respectively. In general, the proposed CFBB technique enhances the performance of the StrongARM by up to 20.8% while the increase in the energy consumption is insignificant.

TABLE I. SPEED AND ENERGY COMPARISON WITH AND WITHOUT THE CFBB TRANSISTOR ($V_{DIFF} = 1$ MILLIVOLT)

		<i>Original</i>	<i>With CFBB</i>	<i>Improvement (%)</i>
Kobayashi StrongARM [9]	Speed (ps)	275.6	218.3	20.8%
	Energy (fJ)	3.489	3.574	-2.4%
Razavi StrongARM [10]	Speed (ps)	278.7	237.2	14.9%
	Energy (fJ)	3.958	3.911	1.2%
Improved StrongARM [11]	Speed (ps)	238.8	203.8	14.7%
	Energy (fJ)	3.596	3.706	-2.9%

TABLE II. SPEED AND ENERGY COMPARISON WITH AND WITHOUT THE CFBB TRANSISTOR ($V_{DIFF} = 10$ MILLIVOLT)

		<i>Original</i>	<i>With CFBB</i>	<i>Improvement (%)</i>
Kobayashi StrongARM [9]	Speed (ps)	192.5	166.3	13.6%
	Energy (fJ)	3.199	3.232	-1%
Razavi StrongARM [10]	Speed (ps)	204.8	185.6	9.4%
	Energy (fJ)	3.698	3.606	2.5%
Improved StrongARM [11]	Speed (ps)	180.9	164.1	9.3%
	Energy (fJ)	3.246	3.304	-1.7%

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