A Self-Biased Schmitt Trigger for Low Power Applications

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***Abstract*—In this paper, a novel technique for enhancement of hysteresis comparators is proposed. This work is based on an improved version of hysteresis comparators that used NMOS current mirrors, a PMOS load stage and a PMOS tail transistor to reduce the static power. By using an internal biasing technique for the tail transistor, we eliminated the need for one of the biasing circuits while achieving 65% lower power consumption in 0.18µm CMOS technology, without much impact on the trip values of the hysteresis comparator.**

Keywords— Comparator; hystersis; Schmitt trigger; low power circuits; positive feedback; bistable characteristics.

I. INTRODUCTION

Placing a comparator in a noisy environment might cause the output to fluctuate between two bistability values, leading to higher power consumption due to dynamic and short circuit currents. Introducing hysteresis increases the immunity of a comparator to noise. Such comparators have also been referred to as Schmitt triggers in which two switching thresholds are set in order to help with noise rejection [1].

Positive feedback is the most popular scheme for setting the positive and negative trip points (V^{+}_{TRP}, V^{-}_{TRP}), in which one of them gets effective based on the value of the output [2]. Hysteresis can be obtained by implementing positive feedback either internally or externally, which can also be tuned internally or externally as well by many techniques based on the targeted application and the tolerance to noise [4, 5]; It is worth noting that hysteresis might not be favorable in some applications, such as ADC converters, in which different outputs might result due to the varying threshold levels [6].

This paper discusses a new method for enhancement of a low supply voltage hysteresis comparator with internal positive feedback, designed for low power applications [3]. Section II is an overview of the previous designs of the hysteresis comparator with internal positive feedback. Section III discusses the proposed design. The simulation results are presented in section IV, followed by the concluding remarks.

II. CONVENTIONAL DESIGNS

One of the most commonly used hysteresis comparators is shown in Fig. 1. It can be seen from that configuration that there is a current-series negative feedback due to the tail transistor at the common source node of $T_{5,6}$ and another voltage-shunt positive feedback due to the Cross Coupled Pair (XCP) $T_{8,9}$. The ratio $(W/L)_{8,9}/(W/L)_{7,10}$ should be greater than one for hysteresis to happen [2].

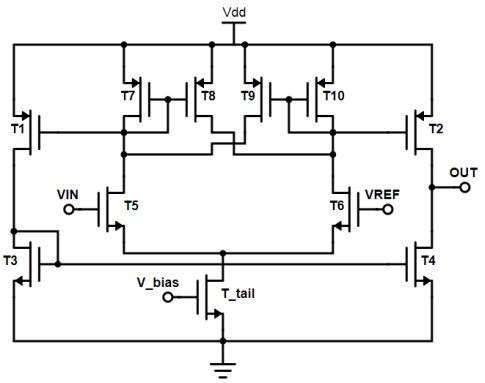

Fig. 1. Conventional Hystersis Comparator toplogy [2]

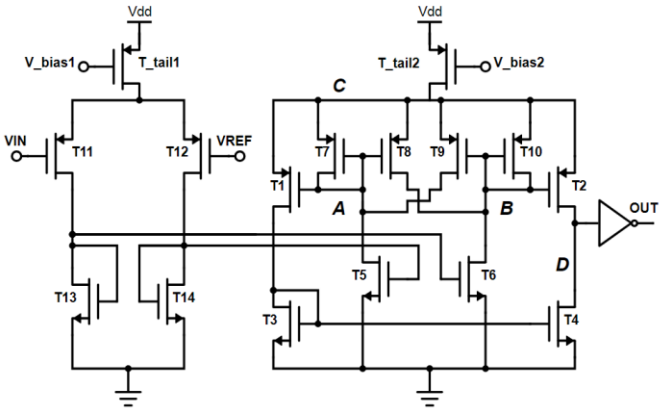

Fig. 2. Improved Hystersis Comparator [3]

Even though this topology is simple and has found its way in many different applications, reducing the supply voltage to have lower power consumption would push some of the transistors away from the saturation region and introduce noise to the circuit. An improvement to the hysteresis comparator has been proposed in [3] as shown in Fig. 2.

This topology comprises of an input stage, from which the currents are mirrored to a load stage where positive feedback creates hysteresis. The input stage is a complementary differential amplifier that has a PMOS tail transistor and a differential pair ($T_{11,12}$) and is loaded with diode-connected NMOS transistors $T_{13,14}$. Currents in the input stage are mirrored to the load stage via transistors $T_{5,6}$. The NMOS tail transistor is replaced by a PMOS tail transistor.

III. PROPOSED DESIGN

The main objective of this paper is to reduce the power consumption of the hysteresis comparator. Even though the low power comparator proposed in [3] showed some improvements, it added a PMOS tail transistor that would require an additional biasing circuit.

Self-biasing has been introduced in the literature to enhance the performance of complementary differential amplifiers that have either limited or wide Input Common Mode Range (ICMR) [7]; these were denoted as Complementary Self-biased Differential Amplifiers (CSDA) and Very-wide Common mode Differential Amplifiers (VCDA) respectively [8][9]. Another commonly observed practice of using an internal node is the level restorer in the Lean Integration with Pass Transistors (LEAP) logic design scheme; a PMOS restorer is used to pull up the input voltage to V_{DD} to reduce the static current in an inverter due to the partially conducting PMOS transistor [10].

Since the load stage of the low power hysteresis comparator [3] has a PMOS tail transistor, it can be biased by one of the circuit nodes, in such a way that the voltage change in node C doesn't impede the operation of the circuit. Fig. 3 illustrates the proposed modification in which the trans-conductivity of the load stage's tail transistor is controlled by the voltage of node B.

When $V_{IN} << V_{REF}$, T_6 will allow more current to flow than T_5, which turns $T_{9,10}$ ON and $T_{7,8}$ OFF. The secondary gain stage, represented by a PMOS differential transistors ($T_{1,2}$) and an NMOS active load ($T_{3,4}$), amplifies the differential voltage V_{AB} and returns a single ended output voltage at node D. Since $V_A > V_B$, the voltage at node D will be high, and the output will be low as a consequence. The current passing through T10 is approximately equal to that of the PMOS tail current, I_{tail2}.

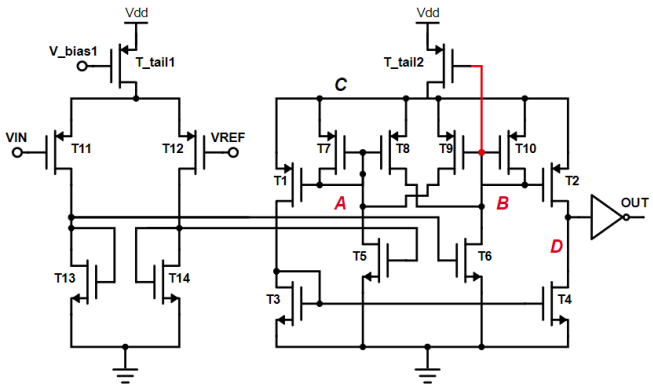

Fig. 3. Proposed Hysteresis Comparator Topology

When $V_{IN} >> V_{REF}$, I_5 exceeds I_6 turning transistors $T_{7,8}$ ON and $T_{9,10}$ OFF. Hence, the voltage at node A will be less than node B. This pulls node D to the negative rail potential, which yields a high voltage at the output. I_7, in this case, is approximately equal to I_{tail2}.

In the self-biasing scheme, node B is used to control the conductivity of the tail transistor. When $V_{IN} < V_{REF}$, the tail transistor will be biased by the low voltage of node B and the circuit will be operating as in [3]. The lower the voltage at node B (gate of T_{tail2}), the higher the voltage at nodes C. Since node B also drives the gates of T_2 and T_9, nodes A and D can reach voltages as high as that of node C. Node B will roughly take a minimum value of $V_{DD} - |V_{OD\_tail2}| - |V_{th10}|$, where V_{OD} represents the overdrive voltage of the transistor. Node A, on the other hand, reaches a maximum voltage of $V_{DD} - |V_{OD\_tail2}|$.

When $V_{IN} > V_{REF}$, the voltage at node B increases, which reduces the conductivity of the tail transistor and lowers the voltage at node C. Since node A has lower potential than node B, the drop in voltage at node C won't have any negative impact. The connection of nodes B and C to each other via T_8 forms a negative feedback that ensures that the tail transistor won't go totally OFF by the rise of voltage across node B, and that node C will be high enough to drive the NMOS transistors of the circuits in the circuit. This would, ideally speaking, form a diode-connected bias transistor (T_{tail2}) with gate and drain (nodes B, C) voltages of $V_{DD} - |V_{th,tail2}|$. Therefore, node A will attain a low voltage value that reaches $V_{DD} - |V_{th\_tail2}| - |V_{th7}|$.

To ensure the circuit is still working fine, $V_{DD} - |V_{th,tail2}|$ should be higher than V_{th3}. In other terms, the minimum value that V_{DD} can be used while ensuring the circuit will keep operating in the safe regime is:

$$V_{DD} \geq V_{th3} + |V_{th\_tail2}| = V_{th\_nmos} + |V_{th\_pmos}| \qquad (1)$$

As the mere purpose behind this type of comparator is to reduce the output fluctuations that would be experienced in single threshold comparators, a minimal shift in the trip voltage due to the introduced gate capacitance (C_{g_tail2}) at node B might not be much of a concern in Schmitt triggers since the trip values are meant to be set apart to account for noise changes. In some applications, the imbalance is set intentionally in order to create various reference voltages as desired; this might be in the form

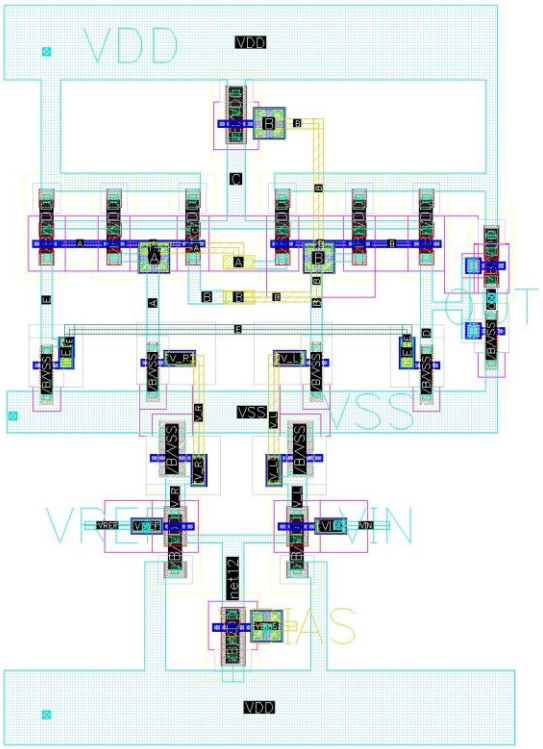

Fig. 4. Layout of the proposed hysteresis comparator.

of external capacitors to provide offset calibration or as variances in transistor dimensions that satisfy Threshold Modified Comparator Circuits (TMCCs) in flash ADC applications [11-13]. The shift in the trip voltage is directly proportional to the capacitance as follows:

$$\Delta V_{trp} \propto H(\Delta C_B/C_B) \quad (2)$$

where H is a function of the branch current, ΔC_B is the extra capacitance introduced by self-biasing the PMOS tail transistor to node B, C_B is the overall capacitance seen in node B.

IV. Simulation Results

The low power hysteresis comparator [3] and its self-biased version (this work) are simulated using TSMC 0.18µm Process Design Kit [14]. Fig. 5 shows the simulation waveforms of the hysteresis comparator output signals for V_{ref}=0.4V, with internal (this work) and external [3] biasing.

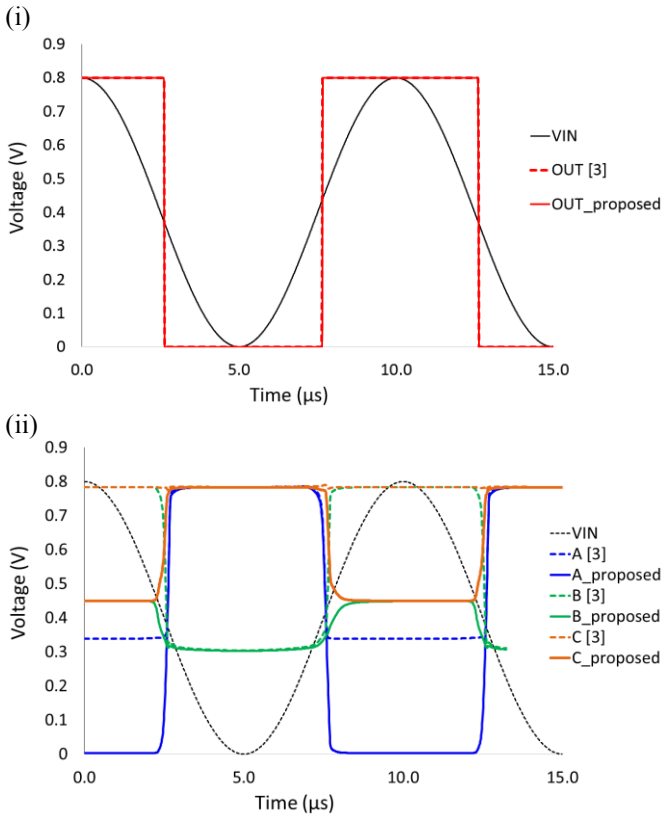

Fig. 5. Simulation waveforms for a fixed-biased and self-biased hysteresis

When node B goes high, T_2 turns off. Since the voltage of node C, which is the effective supply voltage for the circuit, is lower than V_{DD} during the high state of node B, we expect lower power consumption compared to the externally biased scheme. It can be observed in the self-biased scheme that node B rises to a value that doesn't exceed V_{DD}-$|V_{th\_tail2}|$.

Even though this voltage might seem low enough to turn T_2 on, the gate to source voltage of T_2 goes to zero since node B and C approach each other. As long as node C doesn't drop lower than V_{th3}, the transistors $T_{3,4}$ will be on and provide node D with a strong ground signal.

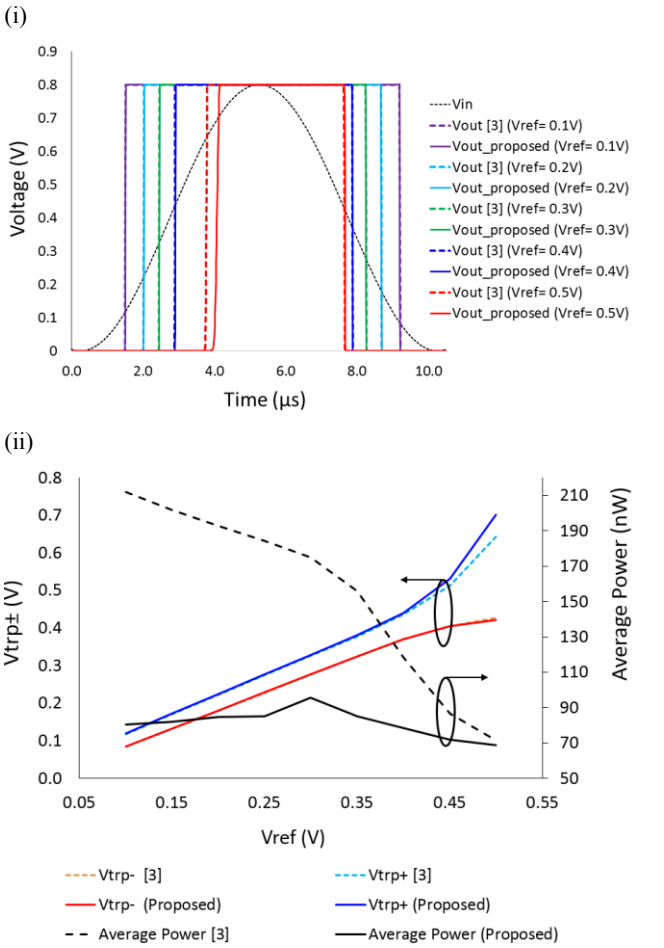

Fig. 6. (i) Input and Output waveforms of fixed and self-biased hysteresis comparator V_{ref}={0.1,0.2,0.3,0.4,0.5}, (ii) (V_{trp+}, V_{trp-}, and Average power)

The upper and lower trip voltages for fixed and self-biased schemes are shown in Fig. 6. It can be easily noticed that there is a little shift in both the upper and lower trip values. ΔV_{trp-} is, however, less than ΔV_{trp+} because ΔC_B varies with the variance of voltage at node B. As V_{IN} increases, the voltage at nodes B also increases and should drive the introduced C_{g_tail2}, which causes the positive shift in V_{trp+}. As node B approaches node C, C_{gd_tail2} gets shorted out which reduces the effective ΔC_B. This facilitates the transition of node B from high to low, causing a little shift in V_{trp-}.

While lowering the voltage at node C is desirable for achieving low energy consumption, increasing it is required for driving the output inverter. Self-biasing manages to do both of them without compromising the operation of the circuit. The waveforms of the internal nodes are shown in Fig. 6(i, ii) for a couple of reference voltages. Increasing V_{bias2} beyond 0.35V reduces the power consumption of the hysteresis comparator, but the trip voltages diverge from the reference voltage. Increasing V_{ref} beyond 0.45V reduces the trans-conductance of the differential pair transistor and pushes them into the linear region, in addition to widening the threshold voltage window.

The minimum percent of power reduction observed by the self-biasing scheme is 9.66% (V_{bias2} = 0.35V, V_{ref}= 0.45V) and

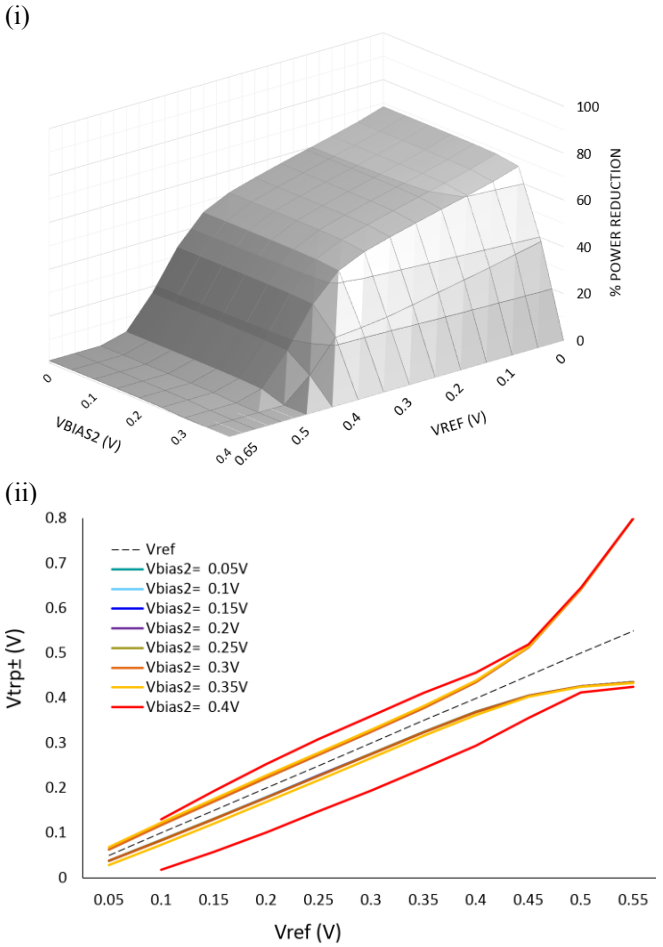

Fig. 7. (i) Percent improvement in average consumed power with respect to V_{ref} and V_{bias2}, (ii) Widening of the hysteretic window for $V_{bias2} > 0.35V$.

increases all the way up to 64.96% ($V_{bias2} = 0.05V$, $V_{ref} = 0.05V$) as can be seen in Fig.7. Table I shows a comparison of the proposed scheme with some other hysteretic comparators that were reported in the literature.

TABLE I. COMPARISON OF HYSTERETIC COMPARATORS IN 0.18 MICROMETER CMOS TECHNOLOGY

	Supply (V)	***Average Power Consumption (W)***
This Work	0.8	78.33n
[3]	0.8	240n
[15]	1.8	180u
[16]	1.8	145u

CONCLUSION

An improved configuration for a low power hysteresis comparator is presented. We have eliminated one of the external biasing circuits by relying on one of the internal nodes. By carefully designing and controlling the voltage variations of the internal node, we minimized the power consumption by 65% in the 0.18µm CMOS technology.

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