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Analysis of Scalar PWM Approach with Optimal Common-Mode Voltage Reduction Technique for Five-Phase Inverters

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***Abstract*—Research on Common-Mode-Voltage (CMV) reduction in multiphase drive systems has recently met an intensified interest in the available literature. This paper first explores two existing space-vector-based CMV reduction schemes for five-phase Voltage Source Inverters (VSIs), denoted as CMVR1 and CMVR2, which reduce the CMV by 40% and 80%, respectively. Moreover, a new space-vector-based CMV reduction scheme, termed as CMVR3, is proposed that not only minimizes the CMV but also reduces the overall switching losses when compared with the other schemes. The optimal duty cycles and the switching sequence of all scheme are introduced. Since the implementation of space-vector-based schemes using look-up tables is a relatively complex and time-consuming process, this paper proposes a simpler scalar PWM approach. This approach can easily be implemented using embedded PWM modules of most commercial Digital Signal Processors (DSPs). To evaluate the performance of the presented CMV reduction schemes, a detailed evaluation study is presented. The optimal CMVR scheme over the full modulation index range is also highlighted. The theoretical findings are verified using a prototype five-phase induction machine through simulations and experimentally.**

***Index Terms*—Common-mode voltage, five-phase inverters, scalar PWM technique, space vector modulation, induction motor drives.**

I. INTRODUCTION

RECENT accelerated development in multiphase drive systems has called for a persistent improvement in the adopted modulation and control techniques to optimize the quality of the power converter output [1]. Such systems are predominantly fed from traditional Voltage Source Inverters (VSIs) [2]. Conventional Pulse Width Modulation (PWM) techniques for two-level VSIs including continuous [3], [4] and discontinuous [5]-[7] PWM techniques provided a satisfactory operation in terms of input/output current ripples and average switching frequency requirements [7]-[12]. However, most of these techniques correspond to a relatively high Common-Mode Voltage (CMV) and high rates of dv/dt, which are the source of serious impacts on drive systems. The main impacts are faster degradation of the motor bearings due to leakage currents, failure of winding insulation, fault activation of current detection circuits, undesirable electromagnetic interference (EMI) and even mechanical vibration [13],[14]. Typically, 10% of the CMV appears between the motor shaft and frame, allowing leakage currents in the bearings [15]. The output voltage dv/dt generates displacement bearing currents, which may damage the motor bearings [16]. Hence, it is necessary to reduce the CMV magnitude as well as the output voltage dv/dt. The CMV of the two-level inverters can be minimized using additional hardware components such as extra inverter legs and passive CMV filters at the output of the drive, while the most popular and cost-effective approach is the suitable design of PWM techniques that minimize the CMV. Therefore, a body of research in the available literature has been devoted to provide efficient CMV Reduction (CMVR) techniques using new and modified modulation and control approaches [13]-[24]. For five-phase VSI drives, the literature demonstrated different CMVR techniques based on Space Vector PWM (SVPWM) [15]-[17], Carrier-Based PWM (CBPWM) [18]-[20], and Model Predictive Control (MPC) [21]-[23] techniques.

The conventional space vector-based CMVR technique for five-phase VSI is developed in [15] for Linear Mode (LM) and in [16] for Overmodulation Mode (OM). The technique in [16] reduces the CMV in the OM region by 40% while the low order voltage harmonics were controlled using the four-active vectors. In [15], an SVPWM scheme is proposed to reduce the CMV by 80% in the LM region. A significant distortion in the inverter output waveform is observed in this technique due to the utilization of six-neighboring large active vectors. A generalized space vector-based CMVR approach for an odd-phase VSI is introduced in [17]. An extension of the Phase-Shifted Sinusoidal PWM (PS-SPWM) method commonly applied in three-phase systems is introduced in [18] for both five- and six-phase VSIs. An alternative CMVR approach based on carrier-based PWM technique is presented in [19], [20] for five-phase VSI and coupled inductor inverter. Modified Model-Predictive Control (MPC) algorithms have also been introduced to reduce CMV in the five-phase VSI drives with sinusoidal output waveforms [21], [22] and with third-harmonic current injection [23].

Despite the work provided in this topic, the detailed analyses of switching characteristics and performance have not met the same interest. To this end, this paper firstly reviews the two space-vectors-based CMVR switching strategies, which reduce the CMV by 40% and 80%, based on the space vector approaches in LM, which are presented in [15], [17], [19]. These schemes are denoted as CMVR1 and CMVR2 in this study. A new space vector-based scheme is then proposed to reduce the CMV and denoted as CMVR3. This technique extends the near-state PWM technique

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initially proposed for three-phase VSIs [24]. This scheme not only reduces the CMV by 80% but also diminishes the switching transition by 20% in each sampling period (sub-cycle), which reduces the switching losses by only utilizing the five-neighboring large active-vectors. A generalized scalar PWM approach for five-phase VSIs, which has a full equivalence and correlation with the space vector algorithm, is proposed to simplify the implementation of space vector-based CMVR technique using commercial Digital Signal Processors (DSPs). A detailed evaluation study to different CMVR techniques is also introduced, including the voltage linear region, closed-form solutions for CMV and the switching losses, the input current stresses, and the output current harmonics in term of harmonic flux analysis. Finally, both simulation and experimental verifications are provided using a five-phase prototype system.

The paper is organized as follows. Section II introduces the operating principles, space vector model and corresponding CMV of the five-phase VSI. Section III reviews the known space vector-based CMVR schemes. Section IV establishes the proposed CMVR3 scheme. Section V gives the generalized scalar PWM approach for the adopted space vector PWM schemes. The performance analysis and comparisons of the four PWM schemes are introduced in Section VI. Section VII details the simulation and experimental results.

II. Inverter Space Vector Model and CMV Analysis

A. Operational Principles

Five-phase two-level inverter, shown in Fig. 1, has 2^5=32 different switching combinations. The switching function of the inverter leg-p $(p = a, b, c, d, e)$ is determined by $S_p \in \{0, 1\}$. The inverter switching vector, $\underline{S}$, is then given by

$$\underline{S} = [S_a \quad S_b \quad S_c \quad S_d \quad S_e]. \tag{1}$$

The inverter pole voltages, v_{pN}, is defined as

$$v_{pN} = S_p V_{dc} \tag{2}$$

where V_{dc} is the dc-link voltage.

Assuming a star-connected load with an isolated neutral, the phase voltage is given by

$$v_p = \frac{4}{5} v_{pN} - \frac{1}{5} \sum_{\substack{q=a \\ q \neq p}}^{e} v_{qN}. \tag{3}$$

The inverter modulation index, M, in LM is defined by

$$M = 2\hat{V}^*/V_{dc} \tag{4}$$

where $\hat{V}^*$ is the peak value of the fundamental output voltage.

For a simple representation in the subsequent analysis, the following constants, K_h, L_h and J_h are defined;

$$K_h = \sin(h\pi/5); \quad L_h = \cos(h\pi/5); \quad J_h = 2L_h - 1. \tag{5}$$

where $h = 1, 2$.

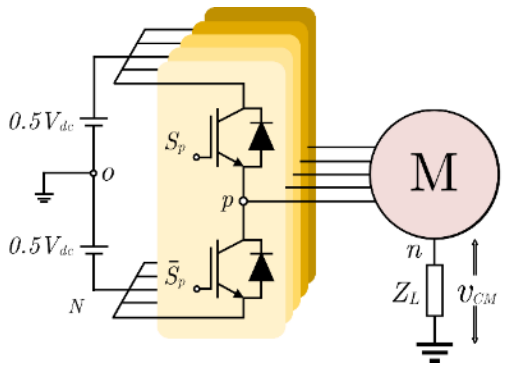

Fig. 1. Power circuit topology of five-phase VSI.

B. Space Vector Model

According to the possible switching vector combinations, the space vector model of the phase voltages in $\alpha\beta$ and xy subspaces is determined by applying Clarke's transformation to (3) as follows [5]

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_x \\ v_y \end{bmatrix} = \frac{2}{5} \begin{bmatrix} 1 & \cos(\gamma) & \cos(2\gamma) & \cos(3\gamma) & \cos(4\gamma) \\ 0 & \sin(\gamma) & \sin(2\gamma) & \sin(3\gamma) & \sin(4\gamma) \\ 1 & \cos(2\gamma) & \cos(4\gamma) & \cos(6\gamma) & \cos(8\gamma) \\ 0 & \sin(2\gamma) & \sin(4\gamma) & \sin(6\gamma) & \sin(8\gamma) \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \\ v_d \\ v_e \end{bmatrix} \tag{6}$$

where $\gamma = 2\pi/5$. The obtained voltage space vectors are therefore classified into thirty active and two zero vectors, as shown in Fig. 2 [6]. The active vectors belong to three different groups based on their vector length, which are namely; small ($|v_s| = 4/5\, L_2 V_{dc}$), medium ($|v_m| = 2/5\, V_{dc}$) and large ($|v_l| = 4/5\, L_1 V_{dc}$) vectors in both $\alpha\beta$ and xy subspaces, where L_h's are defined as given by (5). Thus $\alpha\beta$ and xy subspaces can be considered as three different and concentric decagons. From Fig. 2, the large space vectors in the $\alpha\beta$ subspace of Fig. 2(a) are the small vectors in the xy subspace of Fig. 2(b) and vice versa.

In the five-phase system, the fundamental and harmonic components of the order $(10n + 1)$ with $n \in \{0, 1, 2, \dots\}$ are mapped to the $\alpha\beta$ subspace, while, the harmonic components of the order $(10n + 3)$ are mapped to the secondary xy subspac. Consequently, the $\alpha\beta$ subspace is responsible for fundamental torque production. However, third harmonic injection in the xy subspace can be utilized for torque enhancement [1]. Moreover, the xy subspace can be utilized to operate the five-phase inverters in the overmodulation region [16]. Therefore, in these applications, the VSI has to generate nonzero voltage references in both planes. However, the study in this paper attempts to develop SVPWM and scalar PWM technique with reduced CMV reduction for sinusoidal output voltage generation. Therefore, in all presented modulation techniques, zero reference xy voltage and current components will be assumed. Moreover, two sector classes are utilized for the $\alpha\beta$ subspace, namely, class-A and class-B, as shown in Fig. 2. Class-A is used with the classical CMV reduction techniques, while Class-B will be used with the proposed scheme. In Class-B, all sectors are rotated by $\pi/10$.

C. Common-mode Voltage Analysis

The common mode voltage in a five-phase system can be expressed as follows [15]:

$$v_{CM} = V_{dc}/5 \sum_{q=a}^{e} S_q - V_{dc}/2. \tag{7}$$

According to (6) along with the available switching vectors of the five-phase VSI, six different levels of v_{CM} can be distinguished: large ($\pm 0.5 V_{dc}$), medium ($\pm 0.3 V_{dc}$) and small ($\pm 0.1\, V_{dc}$) CMV. The switching vectors can be classified according to the peak magnitude of the CMV to three groups as follows [16]:

- Large CMV group: generated by the zero space vectors with all switches ON or OFF states, referred as (0-5);
- Medium CMV group: generated by the medium space vectors with one switch ON and four switches OFF or vice versa, denoted as (1-4);
- Small CMV group: obtained by the long and short space vectors with two switches ON and three switches OFF, and vice versa, referred as (2-3).

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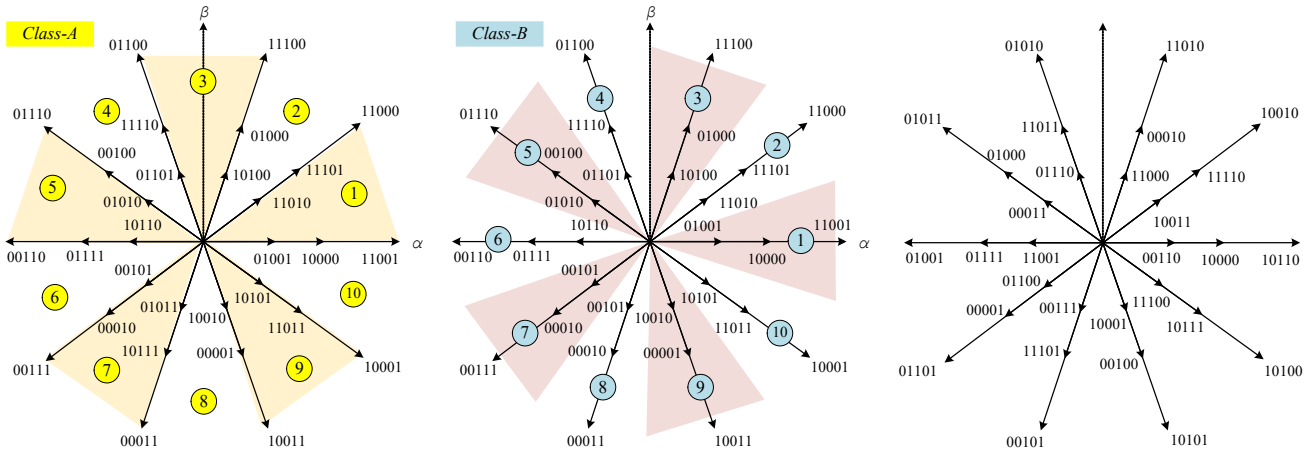

(a) $\alpha\beta$-subspace for class A and B sectors (b) xy-subspace

Fig. 2. Five-phase inverter space vector modeling in $\alpha\beta$ and xy subspaces.

III. Review of Common-Mode Voltage Reduction Schemes Based On SVPWM Techniques

The standard SVPWM and space vector-based CMVR schemes of five-phase VSIs for LM mode are thoroughly described in the literature [15], [17]. However, the main details of these schemes will be summarized in this section. Based on these concepts, a new CMVR scheme based on SVPWM is then proposed in the next section. Table I lists the switching vectors for all sectors in $\alpha\beta$ plane and the corresponding CMV of all existing schemes.

A. Standard SVPWM Scheme

The standard SVPWM method utilizes four (usually two large and two medium) active vectors from $\alpha\beta$ subspace in addition to the zero vectors to generate sinusoidal output voltage [11]. Suppose that the reference vector is in sector A1, the available active vectors will then be {10000, 11000, 11001, and 11101}, as shown in Fig. 3(a). Based on the volt-second balance concept, the reference voltage vector $\left(\vec{v}^* = Me^{j\theta}\right)$ is determined by

$$\begin{cases} \vec{v}^* = \delta_1\vec{v}_1 + \delta_2\vec{v}_2 + \delta_3\vec{v}_3 + \delta_4\vec{v}_4 + \delta_0\vec{v}_0 + \delta_{31}\vec{v}_{31} \\ \delta_0 + \delta_1 + \delta_2 + \delta_3 + \delta_4 + \delta_{31} = 1 \end{cases} \quad (8)$$

where δ_i is the duty cycle and the subscripts $1 \rightarrow 4$ refer to the four active-vectors ($1 \equiv 10000$, $2 \equiv 11000$, $3 \equiv 11001$, $4 \equiv 11101$ in sector-A1) and the subscripts 0 and 31 refer to the zero vectors {00000} and {11111}, respectively.

To generate sinusoidal output voltages, the duty cycles of the selected vectors in an arbitrary sector, s are governed by [6]

$$\begin{cases} \delta_1 = MK_1 \sin\left(s\frac{\pi}{5} - \theta\right) \\ \delta_2 = MK_2 \sin\left(\theta - (s-1)\frac{\pi}{5}\right) \\ \delta_3 = MK_2 \sin\left(s\frac{\pi}{5} - \theta\right) \\ \delta_4 = MK_1 \sin\left(\theta - (s-1)\frac{\pi}{5}\right) \\ \delta_0 = \delta_{31} = \frac{1}{2}\left[1 - K_2 M \cos\left((2s-1)\frac{\pi}{10} - \theta\right)\right] \end{cases} \quad (9)$$

where K_h's are defined as given by (5) and s is the sector number.

The maximum voltage-gain of the five-phase VSI based on this scheme equals $(1/(2K_2)$=0.5257) in the LM region [3].

The switching pattern of this scheme in sector-A1 as well as the corresponding CMV is shown in Fig. 4(a), where a peak CMV with a magnitude of $\pm 0.5V_{dc}$ is obtained.

B. SVPWM schemes with CMVR

According to [15], two CMVR techniques (CMVR1 and CMVR2) were proposed. CMVR1 scheme was able to reduce the peak CMV to $\pm 0.3V_{dc}$ by avoiding the zero vectors in CMVR1 scheme, while the CMVR2 scheme reduces the peak CMV down to $\pm 0.1V_{dc}$ by selecting appropriate large voltage vectors.

1) SVPWM — CMVR 1 Scheme

In this scheme, instead of using the zero vectors, two opposite small active vectors in $\alpha\beta$ subspace, having the same duty cycles given for the zero vectors by (9), are utilized. For example, and assuming sector A1, the selected two opposite vectors are {01101} and {10010}, as shown in Fig. 3(b) and listed in Table I. The peak CMV will then be reduced to $0.3V_{dc}$ [see Fig. 4 (b)].

2) SVPWM — CMVR 2 Scheme

A further CMV reduction can be obtained by utilizing the six neighboring large vectors to the reference vector instead of the employed two large, two medium, and two small vectors in the first scheme. For example, if $\vec{v}^*$ is in sector-A1, the selected vectors are {01100, 11100, 11000, 11001, 10001, and 10011} as shown in Fig. 3(c) and listed in Table I.

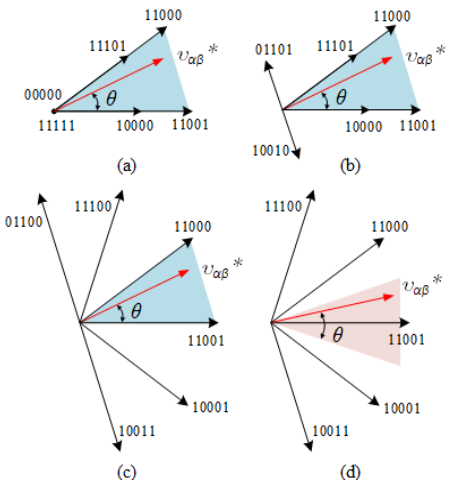

Fig. 3. Selected voltage vectors in sector 1 for (a) Standard SVPWM. (b) CMVR 1. (c) CMVR 2. (d) Proposed CMVR scheme, CMVR 3.

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TABLE I. SWITCHING VECTORS OF THE CONVENTIONAL SVPWM AND CMVR SCHEMES FOR ALL THE 10 SECTORS IN $\alpha\beta$-SUBSPACE PLANE.

Scheme \ Sector	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	Group	Peak CMV
Standard SVPWM	{00000}	{00000}	{00000}	{00000}	{00000}	{00000}	{00000}	{00000}	{00000}	{00000}	(0-5)	$\pm 0.5V_{dc}$
	{10000}	{01000}	{01000}	{00100}	{00100}	{00010}	{00010}	{00001}	{00001}	{10000}	(1-4)	
	{11000}	{11000}	{01100}	{01100}	{00110}	{00110}	{00011}	{00011}	{10001}	{10001}	(2-3)	
	{11001}	{11100}	{11100}	{01110}	{01110}	{00111}	{00111}	{10011}	{10011}	{11001}	(2-3)	
	{11101}	{11101}	{11110}	{11110}	{01111}	{01111}	{10111}	{10111}	{11011}	{11011}	(1-4)	
	{11111}	{11111}	{11111}	{11111}	{11111}	{11111}	{11111}	{11111}	{11111}	{11111}	(0-5)	
CMVR 1	{10010}	{01010}	{01001}	{00101}	{10100}	{10010}	{01010}	{01001}	{00101}	{10100}	(2-3)	$\pm 0.3V_{dc}$
	{10000}	{01000}	{01000}	{00100}	{00100}	{00010}	{00010}	{00001}	{00001}	{10000}	(1-4)	
	{11000}	{11000}	{01100}	{01100}	{00110}	{00110}	{00011}	{00011}	{10001}	{10001}	(2-3)	
	{11001}	{11100}	{11100}	{01110}	{01110}	{00111}	{00111}	{10011}	{10011}	{11001}	(2-3)	
	{11101}	{11101}	{11110}	{11110}	{01111}	{01111}	{10111}	{10111}	{11011}	{11011}	(1-4)	
	{01101}	{10101}	{10110}	{11010}	{01011}	{01101}	{10101}	{10110}	{11010}	{01011}	(2-3)	
CMVR 2	{01100}	{10001}	{00110}	{11000}	{00011}	{01100}	{10001}	{00110}	{11000}	{00011}	(2-3)	$\pm 0.1V_{dc}$
	{11100}	{11001}	{01110}	{11100}	{00111}	{01110}	{10011}	{00111}	{11001}	{10011}	(2-3)	
	{11000}	{11000}	{01100}	{01100}	{00110}	{00110}	{00011}	{00011}	{10001}	{10001}	(2-3)	
	{11001}	{11100}	{11100}	{01110}	{01110}	{00111}	{00111}	{10011}	{10011}	{11001}	(2-3)	
	{10001}	{01100}	{11000}	{00110}	{01100}	{00011}	{00110}	{10001}	{00011}	{11000}	(2-3)	
	{10011}	{01110}	{11001}	{00111}	{11100}	{10011}	{01110}	{11001}	{00111}	{11100}	(2-3)	
Scheme \ Sector	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	Group	Peak CMV
CMVR 3	{11100}	{01100}	{01110}	{00110}	{00111}	{00011}	{10011}	{10001}	{11001}	{11000}	(2-3)	$\pm 0.1V_{dc}$
	{11000}	{11100}	{01100}	{01110}	{00110}	{00111}	{00011}	{10011}	{10001}	{11001}	(2-3)	
	{11001}	{11000}	{11100}	{01100}	{01110}	{00110}	{00111}	{00011}	{10011}	{10001}	(2-3)	
	{10001}	{11001}	{11000}	{11100}	{01100}	{01110}	{00110}	{00111}	{00011}	{10011}	(2-3)	
	{10011}	{10001}	{11001}	{11000}	{11100}	{01100}	{01110}	{00110}	{00111}	{00011}	(2-3)	

Although this scheme reduces the CMV to $0.1V_{dc}$ as shown in the switching pattern in Fig. 4(c), a significant distortion in the output waveform was observed in [15]. This distortion is obtained due to the selection of the six largest vectors, where four of them are outside the sector. This leads to higher error voltage magnitude. The optimal duty cycles that nullify the x-y voltage components are found as in (10), while the detailed derivation is given in Appendix-A.

$$\begin{cases} \hat{\delta}_1 = 1/2\,(1 - MK_2 \sin\vartheta) \\ \hat{\delta}_2 = MK_1(L_2 \sin\vartheta - K_2 \cos\vartheta) \\ \hat{\delta}_3 = MK_2L_2(\sin\vartheta + 4K_1L_2 \cos\vartheta) \\ \hat{\delta}_4 = MK_2L_2(\sin\vartheta - 4K_1L_2 \cos\vartheta) \\ \hat{\delta}_5 = MK_1(L_2 \sin\vartheta + K_2 \cos\vartheta) \\ \hat{\delta}_6 = 1/2\,(1 - MK_2 \sin\vartheta) \end{cases} \tag{10}$$

where L_2 and K_h's are defined as given by (5), $\vartheta = \theta - (s-3)\,\pi/5$, and s is the sector number.

Equation (10) gives a valid solution over the whole LM range, and therefore sinusoidal output waveforms will be obtained.

IV. PROPOSED SPACE VECTOR-BASED CMVR3

A new space vector-based CMVR scheme is proposed in this section and is denoted as CMVR3. This scheme extends the near-state PWM technique introduced in [24] for three-phase VSIs to the five-phase case. Another sector classification called B1-B10 shown in Fig. 2 will, therefore, be utilized. In this scheme, the five neighboring large vectors from $\alpha\beta$ subspace are used to generate the reference output voltage vector. For example, if the reference vector is in sector B1, the selected vectors are (11100, 11000, 11001, 10001, and 10011), as depicted in Fig. 3(d). The mapping of these vectors to the xy subspace can similarly be obtained from Fig. 2(b). These five vectors are selected based on the voltage vectors closest to the reference vector. Hence;

$$\begin{cases} \vec{v}^* = \tilde{\delta}_1\vec{v}_1 + \tilde{\delta}_2\vec{v}_2 + \tilde{\delta}_3\vec{v}_3 + \tilde{\delta}_4\vec{v}_4 + \tilde{\delta}_5\vec{v}_5 \\ \tilde{\delta}_1 + \tilde{\delta}_2 + \tilde{\delta}_3 + \tilde{\delta}_4 + \tilde{\delta}_5 = 1. \end{cases} \tag{11}$$

By solving (11), the duty cycles of this scheme are derived in Appendix B and given by

$$\begin{cases} \tilde{\delta}_1 = 1 - 2ML_2(K_1 + K_2)\sin\vartheta \\ \tilde{\delta}_2 = M(L_2(3K_1 + 2K_2)\sin\vartheta + K_1K_2\cos\vartheta) - 1 \\ \tilde{\delta}_3 = 1 - M(L_2(2K_1 + K_2)\sin\vartheta + J_2K_1K_2\cos\vartheta) \\ \tilde{\delta}_4 = M(L_2(2K_1 + 3K_2)\sin\vartheta - J_2K_1K_2\cos\vartheta) - 1 \\ \tilde{\delta}_5 = 1 - M(L_2(K_1 + 2K_2)\sin\vartheta - K_1K_2\cos\vartheta) \end{cases} \tag{12}$$

where $\vartheta = \theta - (s-3)\,\pi/5$ and s is the sector number.

Since five large vectors are only utilized, (12) yields a valid solution only for a modulation index M between 0.882 $(= [L_2(3K_1 + 2K_2)]^{-1})$ and 1.0515 $(= K_2^{-1})$. These values represent the limits of the LM range of the proposed scheme. Fig. 5 shows the variation of duty cycles based on (12) over a complete fundamental period at these two boundaries of LM region. Clearly, a symmetrical distribution of the duty cycles with positive values is achieved.

The selected vectors in each sector are reordered as listed in Table I to minimize the switching commutations in a switching cycle and switching transitions from one sector to the next. Since five large vectors are used in this scheme, one phase voltage out of the five phases will be clamped to the positive or negative dc-link rail in each sector. This reduces the switching transitions by 20%, which represents the most salient merit of this scheme over the CMVR2 scheme, as shown in Fig. 4(d).

From a practical implementation perspective, the scalar approach will be favored due to its simplicity. Hence, the next step of this work is to present a generalized scalar PWM approach, which employs five-phase modulating signals and carrier waveforms, while the same performance of the presented space vector-based CMVR schemes is achieved.

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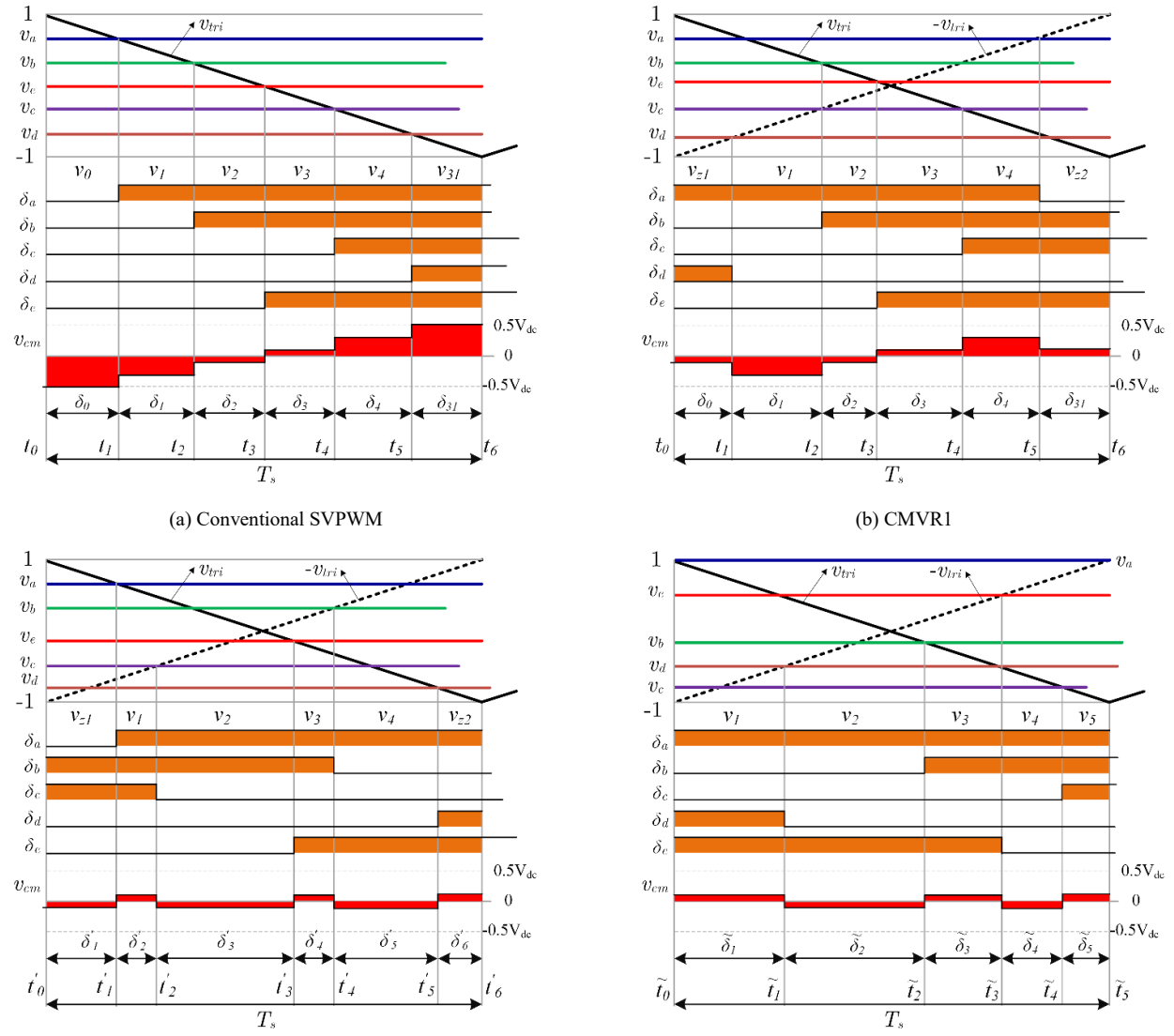

Fig. 4. Single-edge carrier waves, equivalent switching pattern and the corresponding CMV for the analyzed PWM schemes.

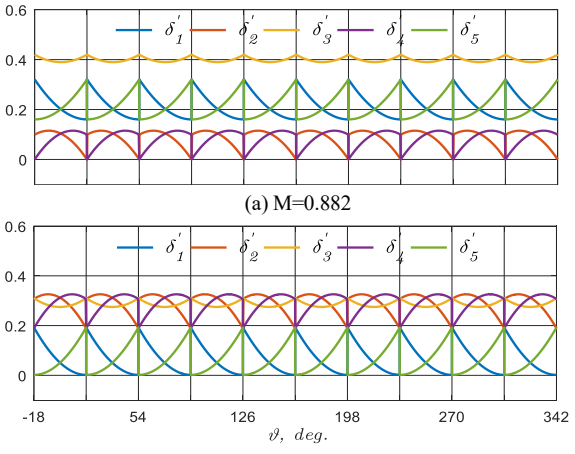

Fig. 5. Duty cycles variation of the proposed CMVR3 at the LM limits.

V. GENERALIZED SCALAR PWM APPROACH

A. Basic Concepts

In the proposed scalar PWM approach, the switching pulses for the power switches are obtained by comparing the modulation signals with a high-frequency triangular carrier wave. A high switching-state is obtained when the modulating signal is higher than the carrier. Due to the switching pattern symmetry, a single-edge from the triangular carrier waves, modulating signals, and the obtained switching pulses are shown in Fig. 4 when the reference voltage vector lays in sector-1. In general, the modulating signals for the leg-p can be defined by

$$v_p = v_p^* + v_{zs} = M\cos\theta_p + v_{zs} \qquad (13)$$

where $\theta_p = \omega t - 2\pi(k-1)/5$, ω is the frequency in rad/s, k =1, 2, …, 5 and v_{zs} is a Zero Sequence Signal (ZSS). The ZSS represents an additional degree of freedom that is used to obtain the modulating signals for the analyzed PWM schemes.

B. Scalar PWM Implementation

1) Scalar - SVPWM

The scalar implementation of the SVPWM is widely addressed in the literature [25]. The modulating signals are sinusoidal with min-max ZSS, which is expressed by

$$v_{zs,(SVPWM,CMVR1,2)} = -1/2\,(v_{\max}^* + v_{\min}^*) \qquad (14)$$

where $v_{\max}^* = \max(v_p^*)$ and $v_{\min}^* = \min(v_p^*)$. The modulating signals that employ ZSS are shown in Fig. 6(a).

On the other hand, in the implementation of CMVR schemes, two phase-shifted carriers (180° shift of the carrier cycle), rather than a single carrier, are utilized [25]. The

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choice of the carrier waveform is also a sector-dependent or phase order-dependent. Table II lists the selected carrier waves for implementing CMVR1, CMVR2 and CMVR3 with the scalar approach, where positive (+) and negative (-) signs denote referencing to the original and the 180° shifted carrier waves, respectively.

2) Scalar - CMVR1

This scheme can be easily adopted here by utilizing a phase-shifted carrier for the minimum and maximum of the modulating signals in each sector based on class-A sectors with the same standard modulating signals shown in Fig. 6. For example, the modulating signals of phases a and d in sector-1 (which have the maximum and minimum magnitude, respectively [see Fig. 6(a)]) are compared with the phase-shifted carrier as shown in Fig. 4(b).

3) Scalar - CMVR2

Using the same approach, the phase-shifted carrier is utilized here for only the second and the fourth order modulating signals in the odd sectors of Class-A. While in the even sectors, the phase-shifted carrier is used for the first, third, and fifth order modulating signals. For example, in Sector-A1, the phase-shifted carrier is used for phase-b and phase-c, while for sector-A2, it is used for phase-b, phase-c, and phase-d, respectively as given in Table II and shown in Fig. 4(c). This results in, (10000, 11101) in sector-1 are replaced by (10001, 11100), and the zero-vectors in the SVPWM method are replaced by (01100, 10011), which minimizes the peak CMV.

4) Scalar - CMVR3

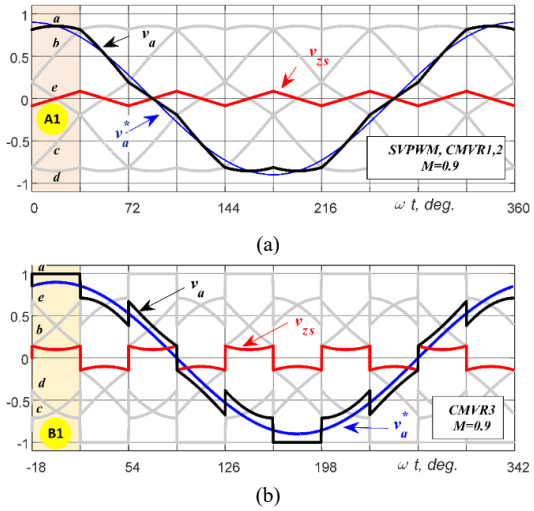
In the scalar implementation of the proposed SVM-CMVR3 method, different modulating signals are utilized. The required modulation signals, in this case, are exactly the same of discontinuous PWM, DPWM1 technique, which has the zero-sequence signal obtained by employing the maximum magnitude test [6]

$$\begin{cases} v_{zs,(CMVR3)} = (2\mu - 1) - \mu v^*_{\max} - (1-\mu)v^*_{\min} \\ \mu = 1/2\,(1 + \text{sign}(\cos(5\omega t))). \end{cases} \quad (15)$$

Although the same modulating signals of DPWM1 are utilized, the implementation of CMVR3 requires two phase-shifted carriers, which are determined from Table II according to Class-B sectors. The modulating and zero sequence signals of this scheme are shown in Fig. 6(b). It can be observed that the clamped phase modulating signal is alternated throughout the fundamental period, where the phase modulating signal, which has the maximum magnitude is clamped to the dc rail with the same polarity. For example, in sector B1, phase-a, which has the maximum magnitude is clamped to the positive dc bus as shown in Fig. 6(b). The switching pulses generation process in this method and the corresponding CMV are shown in Fig. 4(d) when the reference vector is in sector B1. It can be observed that a minimum CMV of magnitude $\pm 0.1V_{dc}$ is obtained. Moreover, the same PWM pattern is observed with the five switching vectors (11100, 11000, 11001, 10001, and 10011).

C. Correlation Between Space Vector Based schemes and Scalar PWM Implementation

In order to verify the correlation among space vector based PWM schemes in sections III and IV and the scalar PWM implementation approach, some salient points have to be considered.



(a)

(b)

Fig. 6. Modulating signals employing ZS signal of scalar PWM.

- The modulating signals in scalar PWM approach of Fig. 6 divide the fundamental period of five-phase references into ten sectors (A1-10 for SVPWM, CMVR1,2, and B1-10 for CMVR3) similar to the SVPWM schemes [Fig. 2].
- If the switching frequency is assumed high enough, the modulating signals of the scalar PWM approach of Fig. 6 can be assumed constant during the sampling interval, T_s as shown in Fig. 4.
- The intersection of the modulating signals of Fig. 4 with the carrier waves defines 1) the duty cycle of each phase (upper switch), δ_p (where $p \in \{a, b, \dots, e\}$), and 2) the duty cycles of each sub-cycle δ_j (where $j \in \{I, II, III, \dots, N\}$ and N is the number of sub-cycles in the switching periods shown in Fig. 4).

Now, and by applying the volt-second balance concept [3], [5], [25] on the switching sequences of Fig. 4, the duty cycle of each phase, δ_p, can easily be determined in the scalar approach for all PWM schemes from

$$\delta_p = 1/2\,(v_p + 1), \quad \text{for } p \in \{a, b, \dots, e\} \quad (16)$$

Moreover, relationships between per-phase duty cycles, δ_p and duty cycles of each sub-cycle, δ_j for sector-1 can be obtained from Fig. 4, and the results are listed in Table-III.

TABLE II. DEPENDENT CARRIER WAVES OF THE SCALAR IMPLEMENTATION OF SPACE VECTOR BASED PWM SCHEMES

	Sector	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
CMVR1	*a*	-	+	+	+	-	-	+	+	+	-
	b	+	-	-	+	+	+	-	-	+	+
	c	+	+	+	-	-	+	+	+	-	-
	d	-	-	+	+	+	-	-	+	+	+
	e	+	+	-	-	+	+	+	-	-	+
CMVR2	*a*	+	+	+	+	+	-	-	-	-	-
	b	-	-	+	+	+	+	+	-	-	-
	c	-	-	-	-	+	+	+	+	+	-
	d	+	-	-	-	-	-	+	+	+	+
	e	+	+	+	-	-	-	-	-	+	+
	Sector	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
CMVR3	*a*	+	-	-	-	-	-	+	+	+	+
	b	+	+	+	-	-	-	-	-	+	+
	c	+	+	+	+	+	-	-	-	-	-
	d	-	-	+	+	+	+	+	-	-	-
	e	-	-	-	-	+	+	+	+	+	-

(+) sign denotes v_{tri} while (-) sign denotes phase-shifted carrier of v_{tri}

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TABLE III. PER-PHASE DUTY CYCLES, δ_p AND SUB-CYCLE DUTY CYCLES RELASHIONSHIPS FOR SECTOR-1.

δ_p	SVPWM	CMVR1	CMVR2	CMVR3
δ_a	$1-\delta_0$	$1-\delta_{31}$	$1-\hat{\delta}_1$	1
δ_b	$1-(\delta_0+\delta_1)$	$1-(\delta_0+\delta_1)$	$1-(\hat{\delta}_5+\hat{\delta}_6)$	$\tilde{\delta}_3+\tilde{\delta}_4+\tilde{\delta}_5$
δ_c	$\delta_4+\delta_{31}$	$\delta_4+\delta_{31}$	$\hat{\delta}_1+\hat{\delta}_2$	$\tilde{\delta}_5$
δ_d	δ_{31}	δ_0	$\hat{\delta}_6$	$\tilde{\delta}_1$
δ_e	$\delta_3+\delta_4+\delta_{31}$	$\delta_3+\delta_4+\delta_{31}$	$\hat{\delta}_4+\hat{\delta}_5+\hat{\delta}_6$	$1-(\tilde{\delta}_4+\tilde{\delta}_5)$

Using (13)-(16) and the relationships given in Table III, it is easy to find the duty cycle of each sub-cycle δ_j for sector-1 in the scalar PWM approach that are equivalent to those calculated in (9), (10), and (12) for the SVPWM schemes. The corresponding results for different schemes are listed in Table IV.

TABLE IV. CALCULATION OF THE DUTY CYCLES δ_j WITH THE SCALAR APPROACH FOR SECTOR-1.

$2\delta_j$	SVPWM	CMVR1	CMVR2	CMVR3
$2\delta_I$	$2\delta_0=1-v_a$	$2\delta_0=1+v_d$	$2\hat{\delta}_1=1-v_a$	$2\tilde{\delta}_1=1+v_d$
$2\delta_{II}$	$2\delta_1=v_a-v_b$	$2\delta_1=-v_b-v_d$	$2\hat{\delta}_2=v_a+v_c$	$2\tilde{\delta}_2=-v_b-v_d$
$2\delta_{III}$	$2\delta_2=v_b-v_e$	$2\delta_2=v_b-v_e$	$2\hat{\delta}_3=-v_c-v_e$	$2\tilde{\delta}_3=v_b+v_e$
$2\delta_{IV}$	$2\delta_3=v_e-v_c$	$2\delta_3=v_e-v_c$	$2\hat{\delta}_4=v_b+v_e$	$2\tilde{\delta}_4=-v_c-v_e$
$2\delta_V$	$2\delta_4=v_c-v_d$	$2\delta_4=v_a+v_c$	$2\hat{\delta}_5=-v_b-v_d$	$2\tilde{\delta}_5=1+v_c$
$2\delta_{VI}$	$2\delta_{31}=1+v_d$	$2\delta_{31}=1-v_a$	$2\hat{\delta}_6=1+v_d$	-

VI. PERFORMANCE ANALYSIS AND COMPARISONS

A. Linear Operating Region

The linear operating region generally determines the output voltage magnitude versus the inverter modulation index and therefore, the dc-bus utilization [3]. In conventional SVPWM, CMVR1, and CMVR2 schemes introduced in section III, their voltage linearity regions will be the same; where it is limited to $M \leq 1.0515$. This can be proved from the duty cycle relations given by (9) and (10). On the other hand, the linearity region of the CMVR3 scheme is limited to $0.882 \leq M \leq 1.0515$, as concluded from (12).

B. Normalized Root-Mean-Square CMV

As far as the CMV magnitude is concerned, the instantaneous CMV, v_{cm} is investigated in every sub-interval over one switching period for different PWM schemes. The focus will be given for the first sector shown in Fig. 4. It can be observed that v_{cm} exhibits a staircase waveform. In order to analyze the CMV under each PWM scheme, the mean squared value of the CMV over one switching period, v^2_{cm-MS} (microscopic analysis) can be determined as follows

$$v^2_{cm-MS}(M,\theta) = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} v^2_{cm}\,dt. \qquad (17)$$

where T_s is the sampling time.

By applying (17) on the switching patterns of the considered PWM schemes [Fig. 4], v^2_{cm-MS} normalized to $V^2_{dc}/100$ is given as

$$\begin{cases} v^2_{cm-MS(SVPWM)} = 25(\delta_0+\delta_{31}) + 9(\delta_1+\delta_4) + \delta_2 + \delta_3 \\ v^2_{cm-MS(CMVR1)} = 9(\delta_1+\delta_4) + \delta_0 + \delta_{31} + \delta_2 + \delta_3 \\ v^2_{cm-MS(CMVR2,3)} = 1. \end{cases} \qquad (18)$$

Fig. 7 illustrates the normalized Root-Mean-Square (RMS) CMV profile in the first sector, which is simply the square root of (17), for all presented PWM schemes. Clearly, all CMVR schemes give lower CMV than SVPWM scheme, while the RMS-CMV value of both CMVR2 and CMVR3 schemes are equal, constant for any modulation index in their linear region limits and have the minimum CMV magnitude.

Since the v_{cm-MS} has tenfold space symmetry, therefore, the mean-square CMV per fundamental period, V^2_{cmf-MS} (macroscopic analysis) can be determined as follows

$$V^2_{cmf-MS}(M) = \frac{5}{\pi}\int_0^{\pi/5} v^2_{cm-MS}(M,\theta)\,d\theta. \qquad (19)$$

As a result of (19), a closed-form polynomial function is obtained and written as follows

$$V^2_{cmf-MS}(M) = CMF\,V^2_{dc} = (a_m M + b_m)V^2_{dc} \qquad (20)$$

where CMF is the CMV Function of the modulation index with unique coefficients a_m and b_m for each PWM scheme. After some tedious derivation steps, the CMF over the entire range of M for each of the considered PWM schemes can be given by

$$\begin{cases} \mathrm{CMF}_{SVPWM} = \frac{1}{\pi}\left[\left(\frac{9}{20}-\frac{17}{10}K_2^2\right)K_1 + \frac{1}{40}K_2\right]M + \frac{1}{4} \\ \mathrm{CMF}_{CMVR1} = \frac{1}{\pi}\left[\left(\frac{9}{20}+\frac{7}{10}K_2^2\right)K_1 - \frac{23}{40}K_2\right]M + \frac{1}{10^2} \\ \mathrm{CMF}_{CMVR2,3} = \frac{1}{10^2}. \end{cases} \qquad (21)$$

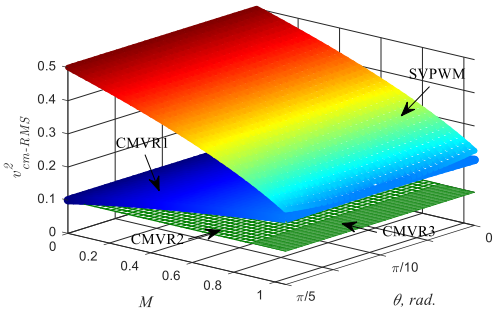

Fig. 7. Normalized per sub-cycle RMS-CMV in sector-1.

Plots of the normalized RMS-CMV against modulation index are given in Fig. 8. As can be seen, CMVR schemes show better performance compared to the conventional SVPWM scheme especially for the lower range of the modulation index. Over the whole modulation index range, CMVR2 and CMVR3 schemes have the best performance.

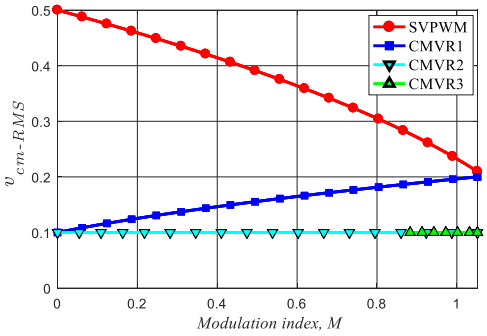

Fig. 8. Normalized RMS value of the per-fundamental CMV versus M.

C. Switching Loss

As widely known, the losses of the power converters are divided into conduction and switching losses. Practically, the conduction losses are the same for different PWM techniques, and typically lower than the switching losses [26]. To obtain a fair comparison between the analyzed PWM schemes in terms of the switching losses, the same average switching frequency is assumed. Firstly, the normalized per-phase switching loss in a sub-cycle, P_{sub-p}, which depends on the dc-voltage, switching times of the device, number of switching, n_p, sub-cycle duration, T, and the per-phase load

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current, i_p, is introduced. If the dc-voltage and the device switching times are assumed constant, P_{sub-p} can then be determined by [26]

$$P_{sub-p} = n_p \left| \frac{i_p}{\sqrt{2} I_1} \right| k_f \tag{22}$$

where I_1 is the amplitude of the fundamental current component and $k_f (= T/T_s)$ is the normalized sub-cycle duration. Based on Fig. 4, the normalized sub-cycle duration, k_f is unity for SVPWM, CMVR1 and CMVR2, while it is 1.25 for CMVR3. Since the effect of load current ripple on the switching losses can be neglected [26], the phase currents can be simply assumed sinusoidal as;

$$i_p = \sqrt{2} I_1 \cos(\theta_p - \phi) \tag{23}$$

where ϕ is the power factor angle.

For the sake of illustration, the normalized switching loss of phase-a (i.e. P_{sub-a}) over a complete period is shown in Fig. 9 for different loading power factors. It can be observed that, P_{sub-a} is a rectified cosine shape with unit peak amplitude for SVPWM, CMVR1, CMVR2 schemes. This is due to one switching transition of phase-a exists in every sub-cycle as shown in Figs. 4 (a)-(c). When CMVR3 is employed, phase-a is clamped for sectors B1 and B6, as illustrated in Fig. 6(b) which implies that n_p= 0. Thus, P_{sub-a} equals zero in these regions. However, in the remaining regions, where n_p=1, it is 1.25 times that of SVPWM and CMVR1, 2 due to the reduction in the sub-cycle duration. The aforementioned illustration can be extended to the remaining phases and the same observation can be obtained. Consequently, the normalized total switching loss in a complete period can then be determined by [26]

$$P_{sub}(\theta, \phi) = \sum_{p=a}^{e} P_{sub-p}. \tag{24}$$

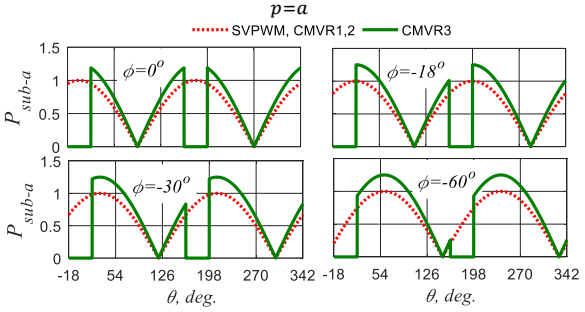

Fig. 9. Normalized switching power loss of phase-a over a complete period at different power factor angles.

Fig. 10 shows a comparison between the analyzed modulation schemes in terms of the normalized sub-cycle total switching loss over a sector under different power factor angles. For further illustration, the comparison is obtained for two sectors. It can be concluded that the best PWM scheme is CMVR3, which has lower total losses at $\phi = 0, -18^{\circ}, -30^{\circ}$, while the SVPWM, CMVR1 and CMVR2 schemes are the best at $\phi = -60^{o}$, as shown in Fig. 10. It can be noted that the average value of P_{sub} for the SVPWM, CMVR1 and CMVR2 schemes is independent of the power factor and equals $10/\pi$. However, in the case of CMVR3 scheme, it depends on the load power factor as shown in Fig. 10. Moreover, the ratio (or the normalized value) of the total switching loss, P_{SW} for CMVR3 to that of the SVPWM over one sector can be calculated from;

$$P_{SW}(\phi) = \frac{1}{2} \int_0^{\pi/5} P_{Sub}(\theta, \phi)\, d\theta. \tag{25}$$

As a result of (25), a closed-form function is obtained and written as follows

$$P_{SW}(\phi) = \frac{10}{\pi} SLF(\phi) \tag{26}$$

where SLF is the switching loss function, which equals one for SVPWM, CMVR1, 2, while for CMVR3 it is represented by

$$SLF = \begin{cases} k_f(1 - L_2 \cos\phi) & \text{for } 0 < |\phi| < 2\pi/5 \\ k_f K_2 \cos\phi & \text{for } 2\pi/5 < |\phi| < \pi/2. \end{cases} \tag{27}$$

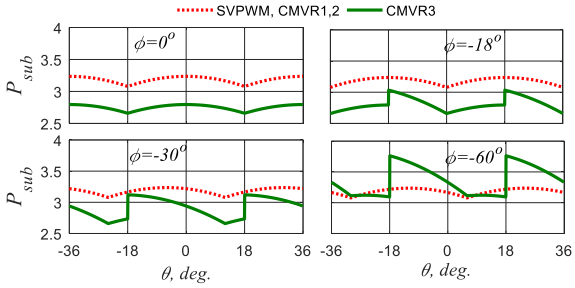

Fig. 10. Normalized total switching power loss over a sub-cycle at different power factor angles.

Fig. 11 shows the SLF variation calculated using (26) against power factor. It is evident that SLF is unity for the SVPWM, CMVR1, and CMVR2 schemes, while in CMVR3 scheme, it is a function of power factor; CMVR3 will be better for $|\phi| \leq 50^{\circ}$ (i.e. load power factor $\geq 1/(5L_2) = 0.6472$). This operating region of the power factor represents a common operating region of the drive systems. It can be concluded that, the switching losses reduction is up to 15% at unity power factor operation under CMVR3 scheme. Hence, in order to minimize both CMV and switching loss over a wide range of power factor, a combination of the CMVR2 and CMVR3 schemes should be adopted.

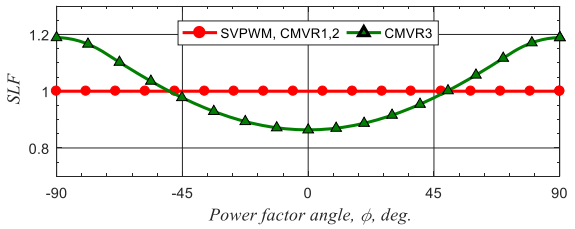

Fig. 11. Normalized switching power loss against power factor angle.

D. Input Current Ripple

Since the inverter dc-link current ripple highly affects the dc-link capacitor sizing [10], this subsection studies the effect of the adopted PWM schemes on the dc-link current ripple. For simplicity, the following analysis neglects the switches' dead-time interval and the reverse recovery current of the inverter freewheeling diodes. Based on these assumptions, the input dc-link current can be determined as follows

$$i_{dc} = \sum_{p=a}^{e} S_p i_p. \tag{28}$$

For the sake of illustration, the dc input current in case of CMVR2 scheme is taken as an example, which can be determined based on the switching pattern of Fig. 4(c) as follows

$$i_{dc} = \begin{cases} (i_b + i_c), & t_0 \leq t \leq t_1 \\ -(i_d + i_e), & t_1 \leq t \leq t_2 \\ (i_a + i_b), & t_2 \leq t \leq t_3 \\ -(i_c + i_d), & t_3 \leq t \leq t_4 \\ (i_a + i_e), & t_4 \leq t \leq t_5 \\ -(i_b + i_c), & t_5 \leq t \leq t_6. \end{cases} \tag{29}$$

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The same can be written for other PWM schemes.

Due to the PWM nature, the dc-link current, i_{dc} is divided into two components, namely, average component, $\bar{\imath}_{dc}$, and ripple component, $\tilde{\imath}_{dc}$, as follows

$$i_{dc} = \bar{\imath}_{dc} + \tilde{\imath}_{dc}. \tag{30}$$

The average dc-current, $\bar{\imath}_{dc}$, can be determined from (31) based on the power invariant concept between the input and output sides.

$$\bar{\imath}_{dc} = 5MI_1 \cos\phi/\left(2\sqrt{2}\right) \tag{31}$$

where I_1 is the effective fundamental current.

The mean-square value of the dc-current, i_{dc}^2 over a sub-cycle can therefore be obtained by

$$i_{dc,MS}^2(M,\theta,\phi) = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} i_{dc}^2\, dt. \tag{32}$$

Substituting (29) into (32) and performing the integration, $i_{dc,MS}^2$ is deduced as in (33) [at the end of this page] for the analyzed schemes where the constant C_k is defined as

$$C_{k-1} = \cos(\omega t - (k-1)\gamma - \phi) \tag{34}$$

where $\gamma = 2\pi/5$ and $k \in \{1,2,\dots,5\}$. Hence, the per-fundamental period mean-square dc-current, $I_{dcf,MS}^2$ is given by;

$$I_{dcf,MS}^2(M,\phi) = \frac{5}{\pi}\int_0^{\pi/5} i_{dc,MS}^2\, d\theta. \tag{35}$$

The effective value of the ripple component of the input current, which represents the capacitor ripple current, $\tilde{I}_{dc}$ is

$$\tilde{I}_{dc}(M,\phi) = \sqrt{I_{dcf,MS}^2 - \bar{\imath}_{dc}^2}. \tag{36}$$

Since, the ratio between the mean-square ripple component of the dc-current obtained from (36) and the output current is defined by the capacitor-current stress factor, K_{dc} [10]. The smaller the value of K_{dc} is, the lower the dc-link capacitor size with a longer life-time. Figs. 12 and 13 show the variation of K_{dc} against the operating parameters ϕ and M for all schemes where the following points can be concluded:

- For SVPWM and CMVR1 schemes, the maximum ripple occurs at ϕ=0 and at $M \approx 1/\sqrt{3}$.
- The dc-link current ripple of both CMVR2 and CMVR3 schemes is highly dependent on both M and ϕ. It decreases when either M or $\cos\phi$ increases. The CMVR2 and CMVR3 schemes have a superior dc-link current characteristic compared to the other schemes at lower values of the power factor angle. Yet, it is also fair to highlight that CMVR2 has lower dc-link current characteristics than CMVR3.

In order to obtain a full vision of the dc-current ripples, Fig. 14 shows the contour plots of K_{dc} over a wide range of M and ϕ for all schemes. It can be observed that, CMVR schemes highly affect the shape and the value of the dc-current ripple, which is owed to zero vectors cancellation. Based on Fig. 13, it is obvious that CMVR2 and CMVR3 schemes have higher K_{dc} than SVPWM and CMVR1. However, the two CMVR schemes have superior dc current-ripple characteristics at high power factor and high M operating conditions.

E. Harmonic Flux Analysis

Due to the discrete nature of the PWM techniques, an error voltage vector, $\Delta\bar{v}$ is generated between the reference voltage vector, $\bar{v}^*$ and the actual inverter output voltage vector, $\bar{v}$ at any arbitrary time instant [8], [11]. This error voltage leads to a corresponding load current ripple, $\Delta\bar{\imath}$, which increases the torque ripple and harmonic losses in case of a motor load. In three-phase systems, the load current ripple can be directly derived from the harmonic flux vector, $\Delta\bar{\lambda}$ (the integral of error voltage vector) by dividing it by the machine equivalent inductance [12]. However, in the multiphase systems, the load current ripple analysis will be more challenging since the harmonic flux in each subspace ($\alpha\beta$ and xy) yields a corresponding current ripple based on the equivalent inductance of each subspace. Hence, for the sake of simplicity, the harmonic flux analysis will be alternatively used [8].

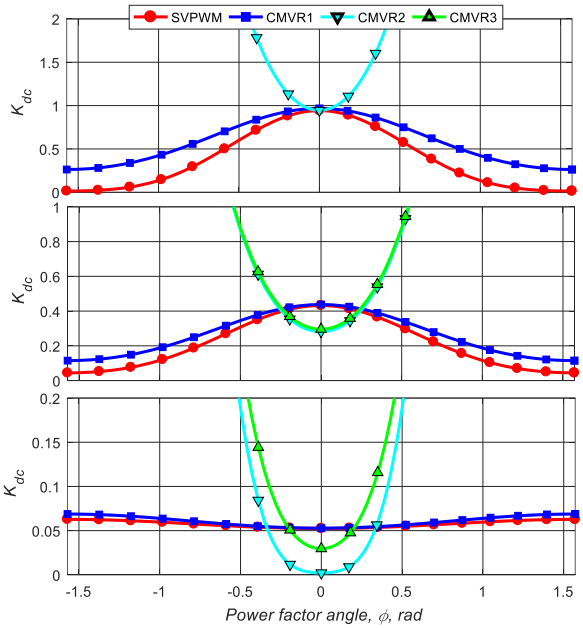

Fig. 12. K_{dc} verses ϕ at (a) M=0.5, (b) M=0.882 and (c) M=1.0515.

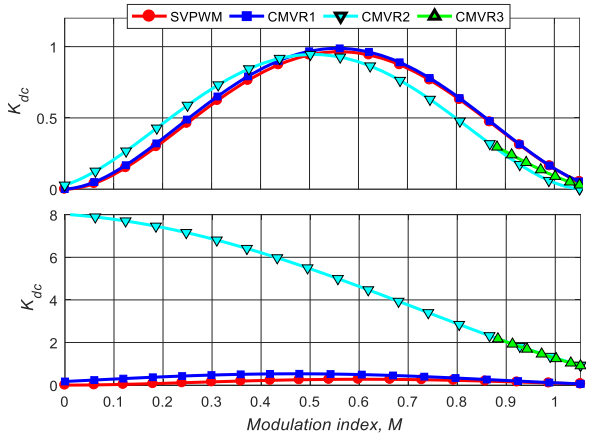

Fig. 13. K_{dc} versus modulation index at (a) ϕ=0 and (b) ϕ=-36.87°.

$$\begin{cases} i_{dc,MS-SVPWM}^2 = I_1^2(C_0^2\delta_1 + (C_0+C_1)^2\delta_2 + (C_2+C_3)^2\delta_3 + C_3^2\delta_4) \\ i_{dc,MS-CMVR1}^2 = I_1^2((C_0+C_3)^2\delta_0 + C_0^2\delta_1 + (C_0+C_1)^2\delta_2 + (C_2+C_3)^2\delta_3 + C_3^2\delta_4 + (C_0+C_3)^2\delta_{31}) \\ i_{dc,MS-CMVR2}^2 = I_1^2\left((C_1+C_2)^2\hat{\delta}_1 + (C_3+C_4)^2\hat{\delta}_2 + (C_0+C_1)^2\hat{\delta}_3 + (C_2+C_3)^2\hat{\delta}_4 + (C_0+C_4)^2\hat{\delta}_5 + (C_1+C_2)^2\hat{\delta}_6\right) \\ i_{dc,MS-CMVR3}^2 = I_1^2\left((C_1+C_2)^2\tilde{\delta}_1 + (C_0+C_4)^2\tilde{\delta}_2 + (C_2+C_3)^2\tilde{\delta}_3 + (C_0+C_1)^2\tilde{\delta}_4 + (C_3+C_4)^2\tilde{\delta}_5\right). \end{cases} \tag{33}$$

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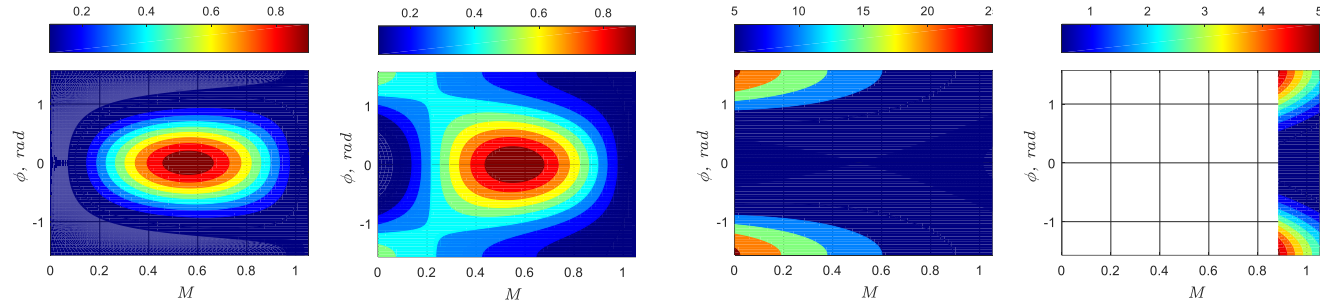

(a) SVPWM (b) CMVR1 (c) CMVR2 (d) CMVR3

Fig. 14. Contour of K_{dc} at the possible modulation indexes range and power factor angle for the analyzed PWM schemes.

Due to the fact that the analyzed PWM schemes differ in the selected voltage vectors and therefore, their sequence, the harmonic flux of each scheme is unique. The harmonic flux vector, $\Delta\bar{\lambda}$, can be evaluated from (37), by considering zero reference space vector in the xy subspace to ensure a sinusoidal output [11].

$$\Delta\bar{\lambda}(M,\theta) = \int_0^1 (\bar{v} - \bar{v}^*)d\delta. \tag{37}$$

where $\bar{v}$ is an arbitrary voltage vector and $\bar{v}^*$ is the reference voltage vector.

Since there are different orders and vector sequences for the analyzed PWM schemes, the harmonic flux of each scheme is unique.

Equation (38) is a generalized equation that can be used to determine the harmonic flux during a segment j (where $j \in \{I, II, III, \dots, N\}$ and N is the number of segments in the switching intervals shown in Fig. 4), by only considering the respective voltage vectors ordering.

$$\Delta\bar{\lambda}_j = \delta \cdot (v_j - v^*) - \sum_{m=1}^{j} \delta_m \cdot (v_j - v_m) \tag{38}$$

where δ_m and v_m are the duty cycle and voltage vector, respectively, during a segment m, and $\delta = t/T_s$ and $t_{j-1} \leq t \leq t_j$ (i.e. t for each interval is governed by its boundaries, as shown in Fig. 4).

Based on (38) and after normalizing the space vector magnitude with $V_{dc}/2$, the mean-square value of the harmonic flux characteristics in $\alpha\beta$ and xy planes for all five phases over a switching period ($0 \leq \delta \leq 1$) is

$$\begin{cases} \Delta\bar{\lambda}^2_{abcde-MS}(M,\theta) = \int_0^1 \Delta\bar{\lambda}_j^2 \, d\delta \\ \Delta\bar{\lambda}^2_{abcde} = \left[\Delta\lambda_\alpha^2 + \Delta\lambda_\beta^2 + \Delta\lambda_x^2 + \Delta\lambda_y^2\right]. \end{cases} \tag{39}$$

Hence the per-fundamental cycle mean-square harmonic flux for the five-phase, $\Delta\lambda^2_{abcde-MSf}$ is given by

$$\Delta\lambda^2_{abcde-MSf}(M) = \frac{5}{\pi}\int_0^{\pi/5} \Delta\lambda^2_{abcde-MS}\, d\delta. \tag{40}$$

Due to symmetry, the same conclusions can be observed from (39) and (40). Figs. 15 and 16 show the mean-square harmonic flux characteristics for the different schemes and the following conclusions can be made:

- The mean-square value of the harmonic flux is highly dependent on the modulation index and PWM scheme.
- The harmonic flux of CMVR schemes is significantly higher than that of the SVPWM method in $\alpha\beta$-plane due to the absence of zero vectors.
- The harmonic flux is zero in both planes for the SVPWM scheme at $M = 0$. This is owed to the zero-modulation index leading to zero error voltage vectors. However, regarding to CMVR1 and CMVR2 schemes, when $M = 0$, the error voltage vectors are non-zeros due to the replacement of the actual zero vectors with two opposite active vectors. These error voltage vectors lead to non-zero harmonic fluxes at $M = 0$ as shown in Figs. 15 and 16.
- In all planes, the harmonic flux content of the CMVR1 scheme equals that of SVPWM at $M = 1.05$, which represents the LM limit, as expected.
- Based on Fig. 16, the harmonic flux content is the same for both CMVR2 and CMVR3 schemes in their common operating region. Therefore, the same harmonic current will be expected. Based on the switching losses characteristics, the proposed CMVR3 scheme is therefore recommended in the region of $0.882 \leq M \leq 1.05$.
- In xy-plane, the harmonic flux of SVPWM scheme increases with the modulation index, while for both CMVR2 and CMVR3 schemes, it will be much lower for higher modulation indices.

Finally, Table V summarizes a comparison between the analyzed PWM schemes according to the presented performance criteria. In conclusion, the proposed CMVR3 scheme has the same characteristics as CMVR2 scheme in the operating region ($0.882 \leq M \leq 1.05$), while the salient benefit is in the reduced switching losses.

Outside of this region of modulation index, CMVR2 scheme with the duty cycles calculated from (10) is the optimum, while in all operating region SVPWM has the superior dc-current and harmonic flux characteristics. Therefore, a hybrid CMV reduction technique should be utilized between CMVR2 and CMVR3 methods in order to effectively reduce the CMV with a wide operating region range. In addition, as concluded from [14] in the case of three-phase VSIs, without changing the CMV reduction strategies, the use of high frequency Silicon Carbide (SiC) devices instead of the traditional Silicon devices in the implementation of the power circuit improve the inverter switching characteristics and input/output waveform quality, especially when the CMV reduction strategies are applied.

VII. Simulation and Experimental Results

In this section, the main conclusions given in previous sections are verified using simulation models with the aid of MATLAB/SIMULINK, and experimentally using the prototype system shown in Fig. 17. In the experimental implementation, a custom-made five-phase VSI circuit is built using ten IRFP460 MOSFETs and SEMIKRON SKHI22A drivers to fed a 5.5 kW, 2-pole, 30 slots, five-phase induction machine (IM). The machine parameters are given in Appendix C.

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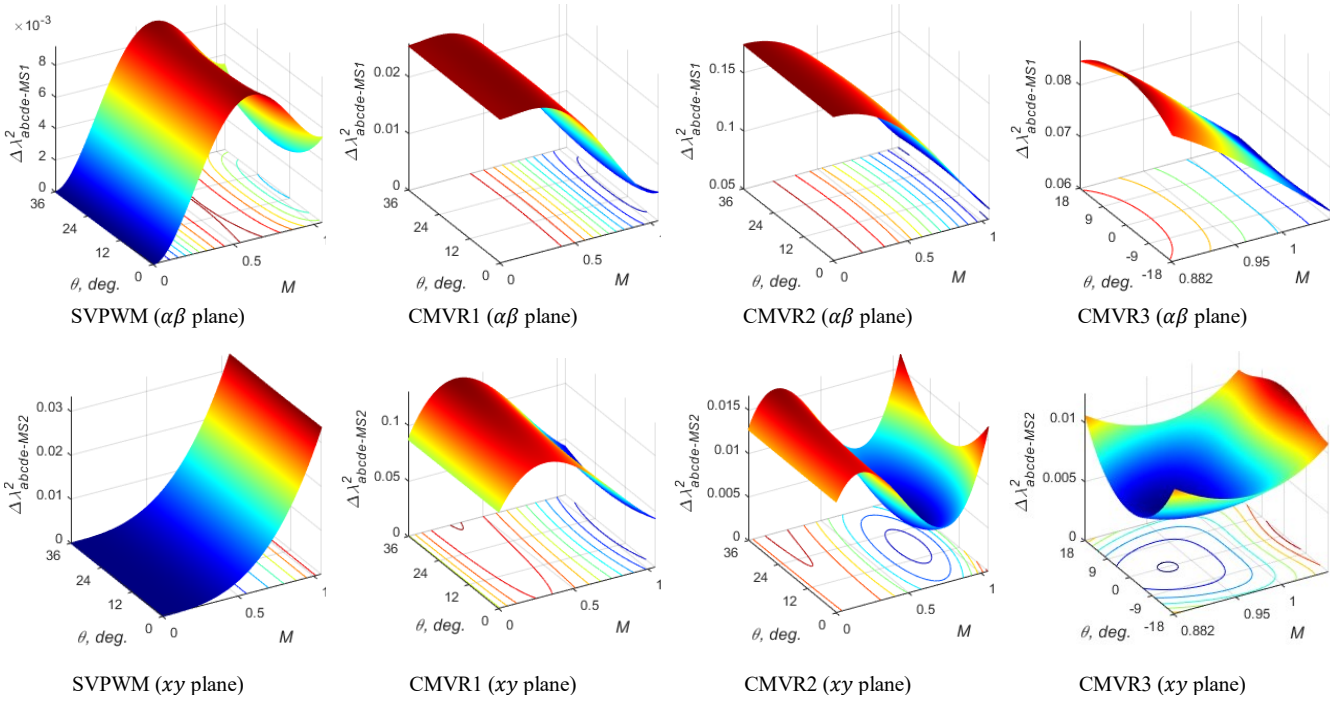
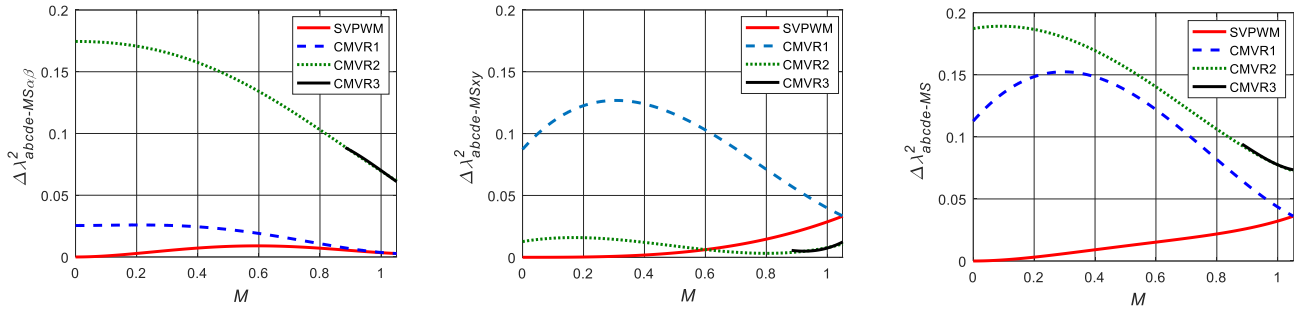


Fig. 15. Mean-square harmonic flux characteristics in sector-1 for the analyzed PWM schemes.



(a) $\alpha\beta$ plane (b) xy plane (c) Complete solution

Fig. 16. Mean-square harmonic flux characteristics at the middle of sector-1 for the analyzed PWM schemes.

TABLE V. COMPARISON BETWEEN THE PRESENTED PWM SCHEMES

Scheme	CMV	Linear region	Switching losses compared with SVPWM	Input current ripple	Flux harmonics
SVPWM	High	$0 \le M \le 1.05$	-	Superior	Superior
CMVR1	Medium	$0 \le M \le 1.05$	The same	Low	High for low modulation index
CMVR2	Small	$0 \le M \le 1.05$	The same	Superior for low power factor operating region but it is low for high power factor region.	Worse
CMVR3	Small	$0.882 \le M \le 1.05$	Lower for power factor ≥ 0.6472	Superior for low power factor operating region, but it is worse for high power factor region.	Worse

A Texas Instrument DSP (TMS320f28335) is used to implement the scalar PWM approach and control the inverter switches [27]. It has six enhanced PWM (ePWM) modules. Five of them will be used in the implementation. The implementation steps of the scalar PWM approach with this DSP is given in [25] and [27].

In both simulation and experimental studies, dc-link voltage is adjusted at 100V and the dc-link filter inductor and capacitor are taken to be 5 mH and 1500μF. The output frequency is set to 25Hz. To obtain a fair PWM ripple performance comparison, the carrier frequency of CMVR3 is set 5/4 (k_f=1.25) times the carrier frequency of other schemes (5 kHz). Thus, the same average switching frequency will be obtained for all schemes.

A. Results for Inverter Output Side

The simulation results of the CMV waveforms of the analyzed PWM schemes are shown in Fig. 18. Due to the utilization of zero vectors, the conventional SVPWM generates a CMV with a peak value of 50 V = 100V/2. After substituting the zero vectors by active-vectors in CMVR1 scheme, the peak value of the CMV is reduced to 30 V. Under the CMVR2 and CMVR3 schemes; the peak CMV is reduced to only 10 V.

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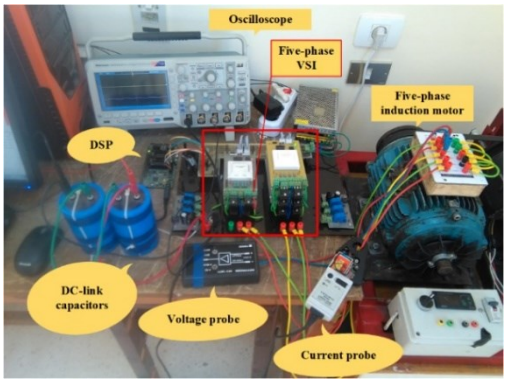

Fig. 17. Photograph of the laboratory experimental setup.

Fig. 19 compares the analytical closed-form expressions given in (19) with the experimental results of the RMS CMV value versus the modulation index under different schemes. The agreement between the calculated and measured values verifies the provided analysis. Clearly, the proposed CMVR schemes (2 and 3) provide the lower RMS CMV at all measured values.

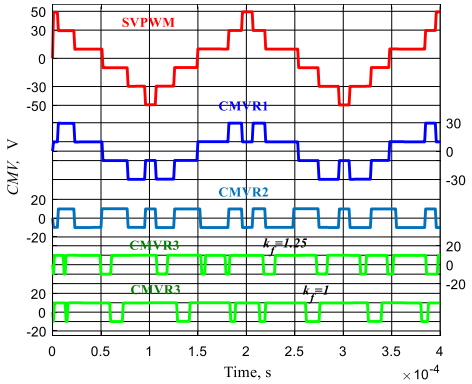

Fig. 18. Simulation results of CMV waveforms for all schemes at M=0.9.

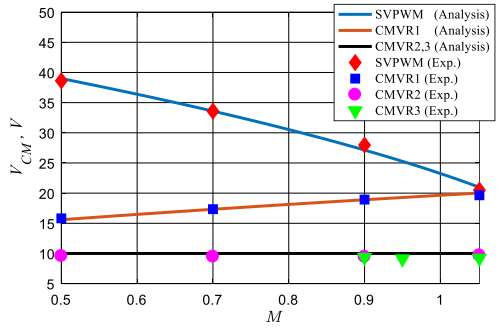

Fig. 19. Comparison of the analytical RMS value of the CMV curves (continuous lines) and experimental results of effective CMV values.

Fig. 20 shows the experimental waveforms for the phase voltage and the CMV for the conventional SVPWM and the three CMVR schemes, which perfectly match the simulation results. For the conventional SVPWM technique, the peak-to-peak CMV is about 100V and decreases to about 60V under the CMVR1 scheme and about 20V for both CMVR2 and CMVR3 schemes, respectively. It can be observed from Fig. 20 that; some voltage spikes are found in the CMV waveforms. This is due to the dead-time effect, and it can be eliminated by applying the proposed algorithm in [28].

Fig. 21 shows the experimental results for the output line voltage and current waveforms for IM load when operating at half-load condition. In all cases, the same current magnitude is obtained. The output currents are nearly sinusoidal with low distortions. To highlight this point, the experimental α-β and x-y components trajectory of the motor currents at M=0.9 and output frequency of 25 Hz are shown in Fig. 22. Clearly, the conventional SVPWM scheme corresponds to minimam xy current components than all CMV reduction schemes as expected in the analysis section, while the CMVR3 scheme introduces x-y current components with considerable magnitude. The induced xy current components consequently generate low-order current harmonics, especially the 3rd harmonic component as depicted by the motor current spectra shown in Fig. 23. The CMVR3 scheme gives rise to a slightly higher third harmonic current component. Under steady-state operation, the contribution of the xy current component to the torque production can be merely neglected [2].

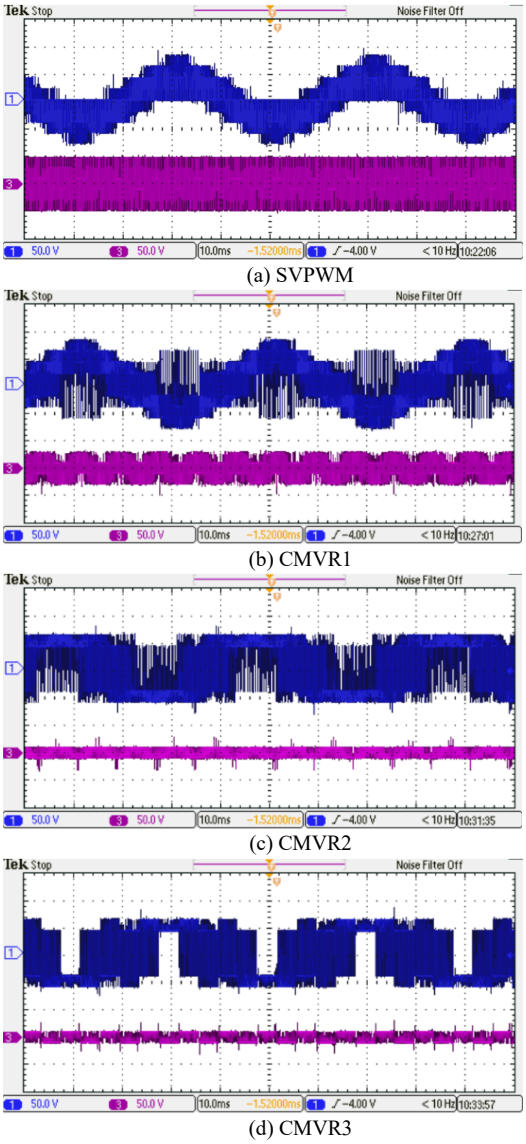

Fig. 20. Experimental phase-voltage (ch1) and CMV (ch3) waveforms at M=0.9 and 25Hz for static-load.

Table VI compares the experimental performance under different techniques based on true RMS values of the CMV as well as the phase voltage and current Total Harmonic Distortions (THD) under the same load condition. In terms of motor line current THD, all CMVR schemes seem close to the conventional SVPWM scheme. The THD experimental results are calculated by the *powergui* Fast Fourier Transformation (FFT) analysis tool in MATLAB with a maximum frequency of 25-kHz. Moreover, the CMVR2 and CMVR3 schemes correspond to an approximate performance.

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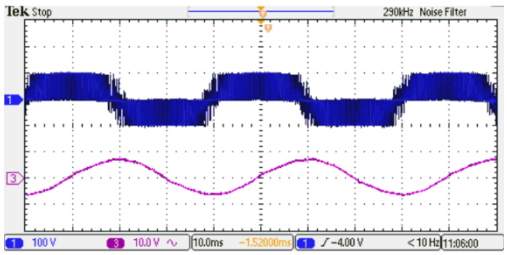
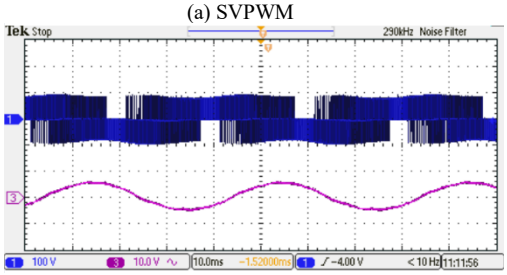
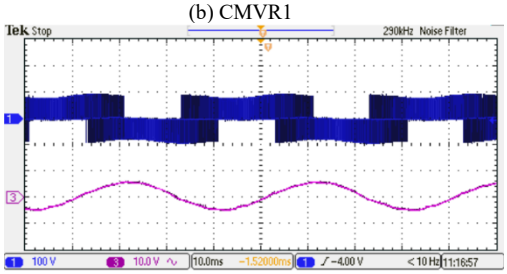


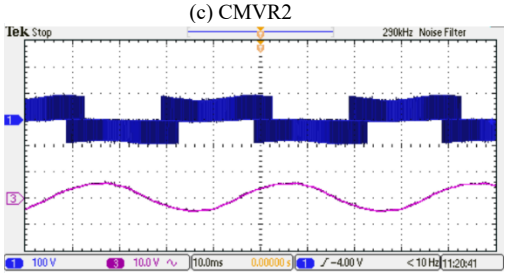
(a) SVPWM



(b) CMVR1

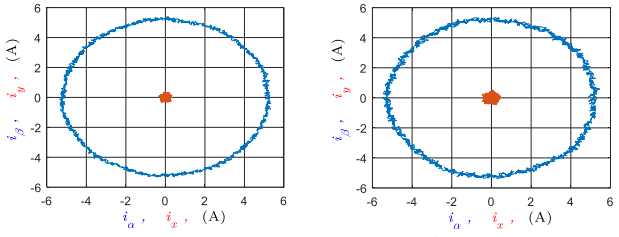


(c) CMVR2



(d) CMVR3

Fig. 21. Experimental line-voltage (ch1) and current (ch3) waveforms at M=0.9 and 25Hz for induction motor load (ch3 10A/div.).



(a) SVPWM (b) CMVR1

(c) CMVR2 (d) CMVR3

Fig. 22. Experimental $\alpha\beta$ current (blue line) and xy currents (red line) locus at M=0.9 and 25Hz for induction motor load.

B. *Results for Inverter Input-Side*

According to the analysis of the input current ripples given in section VI-D, the dc-link capacitor RMS current is influenced by the modulation index and load power factor for each PWM scheme. Simulation and experimental verifications have been carried out in this subsection to prove the theoretical developments.

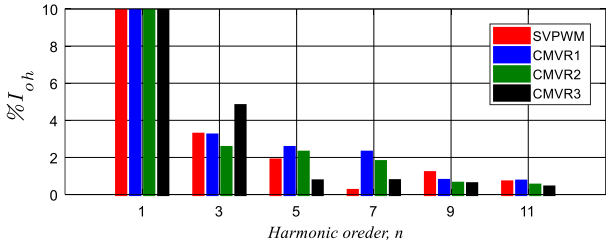


Fig. 23. Experimental output line current spectrum at M = 0.9.

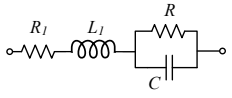
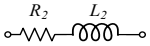
TABLE VI. EXPERIMENTAL EVALUATION OF CMV, THD OF THE OUTPUT PHASE VOLTAGE AND MOTOR CURRENT FOR THE CASE STUDY

Scheme	$V_{CM,rms}$	$\%THD_{v_{ph}}$	$\%THD_{i_{ph}}$
SVPWM	28.98	82.6	5.23
CMVR1	20.1	91.0	6.90
CMVR2	9.44	103.3	6.63
CMVR3	9.11	106.7	6.82

In the simulation results, two different kinds of load are considered in order to obtain near sinusoidal output currents with two different power factors with phase angles of $\phi = 0$ and $\phi = 36.87^o$, respectively, at an output frequency of 50Hz. Table VII shows the per-phase load parameters and configurations for each load. In order to obtain an accurate measurement, an inductance of 10 mH has been inserted between the dc-supply and the dc-link capacitors. Thus, the ac-component of the inverter input current flows through the capacitor. In both cases, a dc-link capacitor of 100µF is used.

For both loads (Load 1 and Load 2), the dc-link voltage and current were measured for a wide range of M with various PWM schemes. Fig. 24 shows the calculated capacitor-current stress factor, K_{dc}. It can be noted that large capacitance leads to minimal dc-link voltage ripples. In spite of the small error obtained, the calculated K_{dc} from the simulation results matches the analysed values shown in Figs. 12-14 for high modulation index region. However, significant errors between the simulation results and the theoretical analysis can be observed at low modulation index region. This is owed to the assumption made of a perfect sinusoidal load line current, while, practically, the output current will be usually contaminated with low order harmonics at low modulation index. In this region, the harmonics magnitude percentage is increased with respect to the fundamental component. The distortions in output currents is expected from the harmonic flux analysis shown in Fig. 16. Therefore, in order to achieve a fair comparison at the low modulation index region, the output current harmonics should be considered in the analysis of the dc-link ripples, which clearly complicate the mathematical derivation.

TABLE VII. PER-PHASE PARAMETERS AND CONFIGURATIONS FOR TWO DIFFERENT POWER FACTOR LOADS

Load type	Load Configuration	Parameters
Load 1 (RLC)		$R_1 = 10\Omega$ $L_1 = 5$mH $R = 1\Omega$ $C = 10\mu$F
Load 2 (RL)		$R_2 = 13\Omega$ $L_2 = 62$mH

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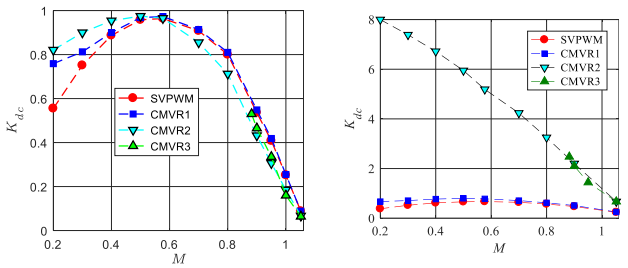
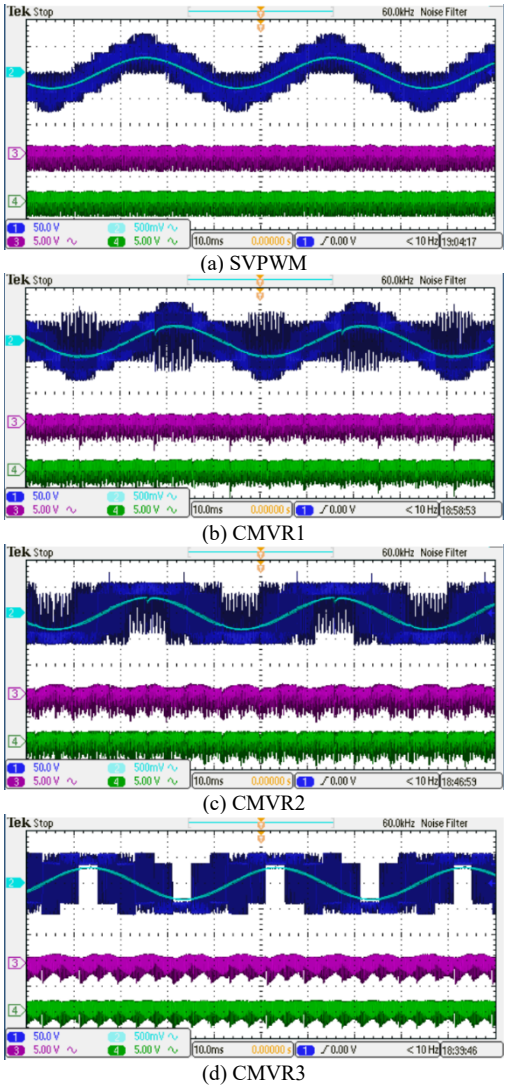


(a) $\phi = 0$ (b) $\phi = 36.87^o$

Fig. 24. Simulation Results of K_{dc} verses M at (a) $\phi = 0$ and (b) $\phi = 36.87^o$.

Moreover, the performance of the inverter input side is experimentally investigated for an RLC load (Load 2 in Table VII). The test is carried out at $M = 0.9$ and $f = 25$ Hz. Fig. 25 shows the experimental waveforms of the load phase-voltage, v_a, phase-current, i_a, capacitor-current, i_C, and input dc-current, i_{dc}, respectively for the considered PWM schemes at these assumed conditions. It can be observed from the phase voltage and current waveforms that unity power factor is achieved in all schemes with a near sinusoidal current waveform. The value of the capacitor-current stress factor, K_{dc} is evaluated using the measured values of the phase current, dc-link capacitor current and dc-current.



(a) SVPWM

(b) CMVR1

(c) CMVR2

(d) CMVR3

Fig. 25. Experimental waveforms of phase voltage (ch1, 50V/div.), phase current (ch2, 7A/div.), capacitor current (ch3, 7A/div.) and dc input current (ch4, 7A/div.) at M=0.9 and 25Hz for RLC load with unity power factor.

TABLE VIII. THE ANALYTICAL, SIMULATION AND EXPERIMENTAL EVALUATION OF K_{DC} AT $M = 0.9$ AND UNITY POWER FACTOR

Scheme \ K_{dc}	Analytical	Simulation	Experimental
SVPWM	0.387	0.548	0.572
CMVR1	0.395	0.536	0.581
CMVR2	0.223	0.432	0.414
CMVR3	0.236	0.464	0.493

Table VIII lists the obtained results of K_{dc} using the experiment and compares it with the results obtained based on both analytical and simulation results. The results are matched and the obtained error between the simulation and experimental results is owed to the output current ripple (which is neglected in the analytical solution) and the unmodeled phenomena. Clearly, the minimum K_{dc} is obtained from CMVR2 as predicted from the analysis section [Fig. 12].

It is worth mentioning that the CMV is a zero-sequence component. With the well-established fact in the literature [1] that the zero subspace can be assumed as a non-flux/non-torque producing subspace, there will be no notable difference in the CMV between a practical motor load and a passive star-connected load. So, the magnetic coupling effects can be neglected in this case. To depict the full image, the main difference appears in the possible higher distortion in the obtained current waveform when a motor load is employed because of the induced xy voltage components. The corresponding xy current component in a motor load will likely be higher – if for no other reason than because of the relatively low impedance of this subspace, especially when a stator with a double layer winding is employed.

In conclusion, although the CMV is reduced, the input and output current ripples are increased by the proposed methods. The choice is application-dependent. A significant reduction of the peak-to-peak and RMS of the CMV can be obtained with CMVR2 and CMVR3 schemes employed with an acceptable distortion in the machine line current. While in these schemes, the same voltage steps in the CMV are obtained, and hence they would both have the same dv/dt, and both of them would have the same influence on the machine's bearings.

VIII. CONCLUSIONS

This paper introduced a generalized scalar PWM strategy to reduce the common-mode voltage of a five-phase VSI. Three PWM schemes for common-mode voltage reduction were introduced. The CMV was reduced up to 80% compared with the conventional SVPWM scheme. A comprehensive analysis of these schemes in terms of voltage linearity region, common-mode voltage, switching losses, input current stresses and output current harmonics was presented. The given analysis proved that the CMVR2 and CMVR3 schemes give the minimum possible CMV for a five-phase VSI. Although the CMVR3 can effectively reduce the switching losses by about 15%, the CMVR2 has a wider linear operating region than CMVR3; the latter has a better performance in high modulation index region between $0.882 \leq M \leq 1.0515$. In terms of the dc-link current stresses, both schemes have a superior characteristic compared with the other presented PWM schemes especially at high load power factor. As a consequence, to all CMVR techniques, the load

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voltage and current will experience higher distortion since a higher harmonic flux will be obtained. Nevertheless, both CMVR2 and CMVR3 schemes give similar output current harmonics.

APPENDIX A
DUTY CYCLE CALCULATIONS FOR CMVR2

Applying the volt-second balance concept to sector A3 in the $\alpha\beta$ subspace of Fig. 2(a) gives

$$\vec{v}^*_{\alpha\beta} = \hat{\delta}_1\vec{v}_{1\alpha\beta} + \hat{\delta}_2\vec{v}_{2\alpha\beta} + \cdots + \hat{\delta}_5\vec{v}_{5\alpha\beta} + \hat{\delta}_6\vec{v}_{6\alpha\beta} \quad \text{(A1)}$$

Accordingly, in Fig. 2(b), the corresponding xy subspace reference voltage for $\vec{v}^*_{xy} = 0$ to generate sinusoidal outputs is given by

$$0 = \hat{\delta}_1\vec{v}_{1xy} + \hat{\delta}_2\vec{v}_{2xy} + \cdots + \hat{\delta}_5\vec{v}_{5xy} + \hat{\delta}_6\vec{v}_{6xy}. \quad \text{(A2)}$$

Equations (A1) and (A2) can be rewritten in a matrix form as

$$[V^*] = [\hat{C}][\hat{D}] \quad \text{(A3)}$$

where

$$[V^*] = [M\cos\theta \quad M\sin\theta \quad 0 \quad 0]^t \quad \text{(A4)}$$

$$[\hat{D}] = [\hat{\delta}_1 \quad \hat{\delta}_2 \quad \hat{\delta}_3 \quad \hat{\delta}_4 \quad \hat{\delta}_5 \quad \hat{\delta}_6]^t \quad \text{(A5)}$$

$$[C] = \frac{4}{5}\begin{bmatrix} L_1 & L_1^2 & L_1L_2 & -L_1L_2 & -L_1^2 & L_1 \\ 0 & L_1K_1 & L_1K_2 & L_1K_2 & L_1K_1 & 0 \\ -L_2 & L_2^2 & L_1L_2 & -L_1L_2 & -L_2^2 & L_2 \\ 0 & L_2K_2 & -L_2K_1 & -L_2K_1 & L_2K_2 & 0 \end{bmatrix} \quad \text{(A6)}$$

The duty cycles are governed by

$$\begin{cases} \hat{\delta}_1 + \hat{\delta}_2 + \hat{\delta}_3 + \hat{\delta}_4 + \hat{\delta}_5 + \hat{\delta}_6 = 1 \\ \hat{\delta}_1 = \hat{\delta}_6. \end{cases} \quad \text{(A7)}$$

By solving (A2) with the constraints given by (A7), the optimized duty cycles of CMVR2 scheme for generating sinusoidal outputs will be as given by (10).

APPENDIX B
DUTY CYCLE CALCULATIONS FOR CMVR3

Following the same procedure in Appendix-A for calculating the duty cycles of CMVR3 in sector B3, as an example. Based on the selected vectors in $\alpha\beta$ subspace of Fig. 2(a) and their mapping to the xy subspace in Fig. 2(b), (10) can be written as

$$[V^*] = [\tilde{C}][\tilde{D}] \quad \text{(B1)}$$

where

$$[\tilde{D}] = [\tilde{\delta}_1 \quad \tilde{\delta}_2 \quad \tilde{\delta}_3 \quad \tilde{\delta}_4 \quad \tilde{\delta}_5]^t \quad \text{(B2)}$$

$$[\tilde{C}] = \frac{4}{5}\begin{bmatrix} L_1 & L_1^2 & L_1L_2 & -L_1L_2 & -L_1^2 \\ 0 & L_1K_1 & L_1K_2 & L_1K_2 & L_1K_1 \\ -L_2 & L_2^2 & L_1L_2 & -L_1L_2 & -L_2^2 \\ 0 & L_2K_2 & -L_2K_1 & -L_2K_1 & L_2K_2 \end{bmatrix} \quad \text{(B3)}$$

By solving (B1), the duty cycles of this scheme will be as given by (12).

APPENDIX C
FIVE-PHASE INDUCTION MACHINE PARAMETERS

Parameter	Value	Parameter	Value	Parameter	Value
R_s (Ω)	1.913	R_{r1} (Ω)	0.614	R_{r3} (Ω)	0.245
L_{s1} (mH)	11.2	L_{s3} (mH)	11.2	L_{r1} (mH)	22.8
L_{r3} (mH)	9.1	L_{m1} (mH)	168.3	L_{m3} (mH)	14.7

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