# Hardware Emulation of Memristor Based Ternary Content Addressable Memory

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***Abstract*—MTCAM (Memristor Ternary Content Addressable Memory) is a special purpose storage medium in which data could be retrieved based on the stored content. Using Memristors as the main storage element provides the potential of achieving higher density and more efficient solutions than conventional methods. A key missing item in the validation of such approaches is the wide spread availability of hardware emulation platforms that can provide reliable and repeatable performance statistics. In this paper, we present a hardware MTCAM emulation based on 2-Transistors-2Memristors (2T2M) bit-cell. It builds on a bipolar memristor model with storing and fetching capabilities based on the actual current-voltage behaviour. The proposed design offers a flexible verification environment with quick design revisions, high execution speeds and powerful debugging techniques. The proposed design is modeled using VHDL and prototyped on Xilinx Virtex® FPGA.**

***Keywords*—Memristor, Memristor Ternary Content Addressable Memory (MTCAM), 2-transistors-Memristors bit-cell, VHDL, FPGA.**

## I. Introduction

Memristor-based Ternary Content addressable Memory (MTCAM) is considered as one of the most promising alternatives for current generation CMOS-ternary content addressable memories (TCAM) [1]. Different designs of MTCAM based on hybrid memristor-CMOS have been proposed over the last few years [2]. The designs varied in the numbers of both memristors and transistors used to build the bit-cell memory. Various cell configurations of possible MTCAM structures with SRAM 8T-2M (8-Transistors 2-memristors) [3], SRAM-6T-2M [4], SRAM-5T-2M [5], Re-CAM-5T-2M [1] and Re-CAM-2T-2M [6] were presented. The 2T2M bit-cell design is considered as the most concise and efficient structure. It uses 2 memristors to store data and 2 MOS transistors as access devices, allowing for a high density memory. Software simulators have been used to validate the performance of MTCAM architectures. However, to date, hardware emulators for realistic MTCAMs had never been proposed, even though software approaches are highly challenged when simulating large arrays that are typical in MTCAM applications. An FPGA based hardware emulation of a 2T2M bit-cell based MTCAM provides numerous advantages, 1) with hardware emulation, one can easily reconfigure memory to a variety of sizes, and collect performance statistics on the fly, 2) provides the ability to perform rapid design revisions at much faster execution rates, 3) provides deeper insight in the structures' operation, due to immediate feedback, 4) provides high capacity, flexibility and powerful debugging capabilities. In this paper, we propose for the first time an FPGA hardware design of MTCAM based on 2T2M bit-cell. The proposed MTCAM returns the corresponding addresses of the matching content after a comparison with stored data and an input search data for different sizes. Each entry in the memory contains dedicated search hardware that is activated in parallel, when a search pattern is supplied to the memory. Every entry is simultaneously compared to the input pattern, and if a match is found, the address is returned. The write operation was also simulated and functionally verified. The rest of the paper is organized as follows. Section II introduces preliminary concepts related to this work and describes the 2T2M based TCAM cell structure with conventional search approach. In Section III, The MTCAM implementation and design methodology are further discussed. Finally, Section IV presents the conclusion of results and future perspectives on potential applications.

## II. Background and Motivation

### A. Memristor

A memristor is a nonlinear resistor that changes its state according to the charge passing through it and retains this state after an electrical bias is removed [7] [8]. It is defined as a non-volatile two terminal memory device and considered as the key element to realize high scalability and low-power designs. Those properties can be implemented in the TCAM structure to reduce the power consumption significantly by removing the power supply of TCAM blocks. Binary states are stored on the memristor in the form of "high" and "low" resistances. The state '0' represent high resistance and state '1' the low resistance. The state can be encoded by applying appropriate voltage.

### B. Ternary Content Addressable Memory

Content Addressable Memory (CAM) is a type of memory that can be accessed using its contents rather than an explicit address[9]. In order to access a particular entry in such CAM, a search data word is compared against previously stored entries in parallel to find a match. Each stored entry is associated with a tag that is used in the comparison process. Once a search data word is applied to the input of a CAM, the matching data word is retrieved within a single clock cycle if it exists. The CAM can be classified as two forms, one is Binary CAM

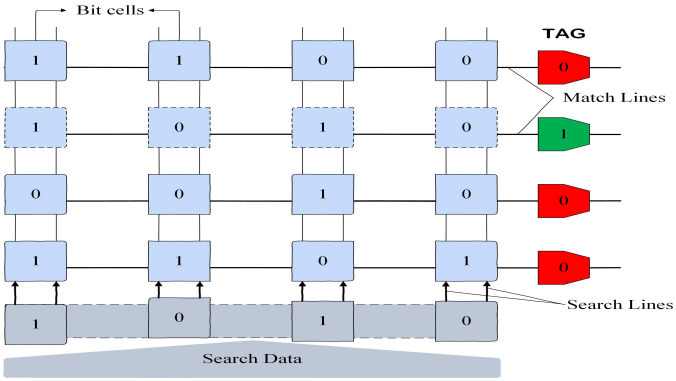


Fig. 1. Conceptual view of a Ternary Content Addressable Memory containing 4 words. In this example, the 'light gray' colour represents the Data input and the 'light blue 'represents the stored Data. The 'Red' Tag is the mismatched word location and the 'Green' Tag indicates the location of the matched word.

and other is ternary CAM (TCAM). As the name means, the binary CAM can store and search only binary bits i.e. '0' and '1'and the input search data will be either logic '0' or logic '1'. The ternary CAM (TCAM) allows storage and searching three different states which are '0', '1' and 'X'. The logic 'X' is a state which is regarded as a "Don't care" state. Both a logic '0' and a logic '1' from the searched data match the stored logic 'X'. At the present time, Ternary CAM is used for the reason that its ability to store and search 'Don't care' state, which an added feature to binary CAM. Nevertheless, designs have several major challenges. In particular design density of these devices is lean compared with SRAM, while they are power hungry devices. To address those issues, memristor based TCAM designs have been presented in [4] and [1]. In those paper, the authors used memristors to replace SRAM to store the information. Those designs can reduce power consumption up to 95 % [1]. Therefore, they are very power efficient and present high density. Different designs configurations of MTCAM based on hybrid memristor-CMOS have been proposed. The designs varied in the numbers of both memristors and transistors used to build the bit-cell memory. Recently, to further improve the performance of the memristor based TCAM, a design of MTCAM with only two transistors and two memristors is proposed in [6].

### *C. 2T2M bit-cell based TCAM*

In this work we adopt the 2T2M bit-cell based TCAM design as it is considered as the most concise and efficient structure. This memory bit-cell design consists only of two transistors and two memristors (2T2M) as shown in Figure 2. In this architecture the memristor device can work as a storage element and a switch at the same time. As highlighted previously, the essential requirement for a TCAM array is to sort out the location of matches with a search word: the input searched data will be provided into the memory, if they are matched with the stored data, a match signal will be activated to indicate the stored information has a matched data as shown in figure 1.

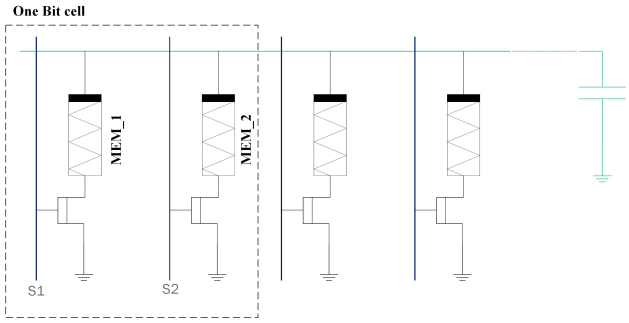


Fig. 2. Schematic for 2-Transistor 2-Memristor bit-cell based TCAM Row.

With the 2T2M based TCAM this is typically can be achieved by pre-charging all the rows of the array, and then a search word is applied to the columns. During the evaluation phase, the memory matching lines remain high if the search word fully matches the rows contents. Otherwise the capacitance is discharged to ground in case of a search bit mismatch [6]. The flowchart of 2T2M based TCAM search scheme is shown in Figure 3. In the last case, the memristor and the series transistor are of low resistances creating a path to ground. Therefore, data is stored in a "2T2M" cell in a complimentary mode. The high resistance device will not leak charges to the ground even in case of a mismatch, contrary to its complementary device. The search outcome is either a match, mismatch or a Don't care state in which both memristors in the cell are set to a high resistance value. The three states of one memristor TCAM bit cell are encoded in memristors (M1) and (M2) as shown in Table I. The memristor modeling and the MTCAM emulation in terms of the search and test bench generation are presented in the next section.

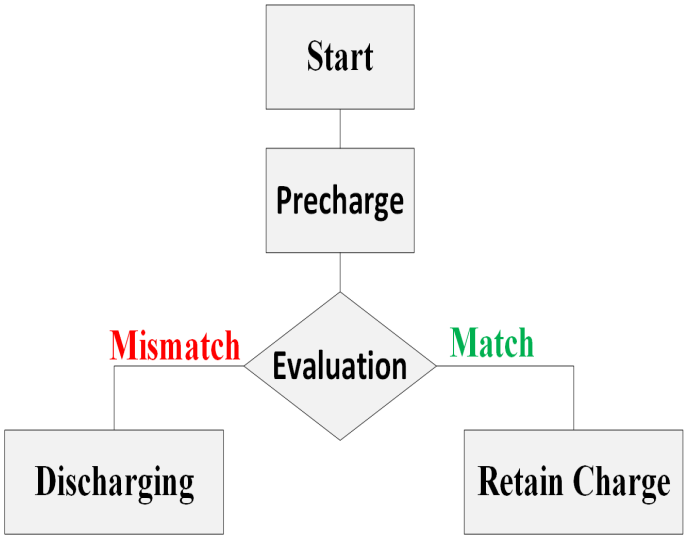


Fig. 3. Flow chart of conventional 2T2M search scheme.

TABLE I
MTCAM BIT-CELL TRUTH TABLE

| Search word | | Stored Data | | |
|---|---|---|---|---|
| $S1$ | $S2$ | $M1$ | $M2$ | $State$ |
| 0 | 1 | 1 | 0 | $Match$ |
| 1 | 0 | 1 | 0 | $Match$ |
| 1 | 0 | 1 | 0 | $Mismatch$ |
| 1 | 1 | 0 | 0 | $Mismatch$ |
| 0 | 1 | 0 | 0 | $Mismatch$ |
| 1 | 0 | 0 | 0 | $Mismatch$ |

## III. DESIGN METHODOLOGY

### A. Memristor Hardware Emulation

Foremost, as a basic circuit element, we start by implementing the memristor. Hence, in order to integrate the resistive device into the TCAM circuit design flow, a practical mathematical description of this device is required for the initial design phase. In this paper, we take on the threshold-type based bipolar device model of [10]. In this paper, a specific realization of a voltage-controlled memristive system with threshold has been suggested. In this model, the memristance R plays the role of the internal state variable x, namely,$x \equiv R$, defining the device state via the following equations.

$$I = x^{-1} V_M \tag{1}$$

$$\frac{dx}{dt} = f(V_M) W(x, V_M) \tag{2}$$

$$f(V_M) = \beta V_M + 0.5(\alpha_\beta)[|V_M + V_T| - |V_M - V_T|] \tag{3}$$

$$W(x, V_M) = \Theta(R_{off} - x) + (-V_M)\Theta(x - R_{on}) \tag{4}$$

Where $\Theta(.)$ is the step function, $\beta$ is a positive constant characterizing the rate of memristance change when $|VM| > V_T$, $V_T$ is the threshold voltage, and Ron and Roff are limiting values of the memristor resistance. In Eq. (4), the role of $\Theta$-functions is to confine the memristance change to the interval between Ron and Roff. In many real memristive devices, the resistance change is related to the atomic migration induced by the applied field and not by the electric current flow. Actually, those equations provide a compact realistic description of bipolar memristive devices. The model takes into account boundary values of memristance and threshold type switching behavior. Here we designed a simple memristor component. It was modeled using VHDL and implemented on a Xilinx VIRTEX® 7 XC4VSX35 FPGA with logic utilization less than 0.02%. The I-V characteristics for the bipolar memristor device with a sinusoidal input voltage is shown in Figure 4. The proposed bipolar device fits into an extremely small area with a maximum delay for the output buses of 1.86 ns. It allows to design large array MTCAM size.

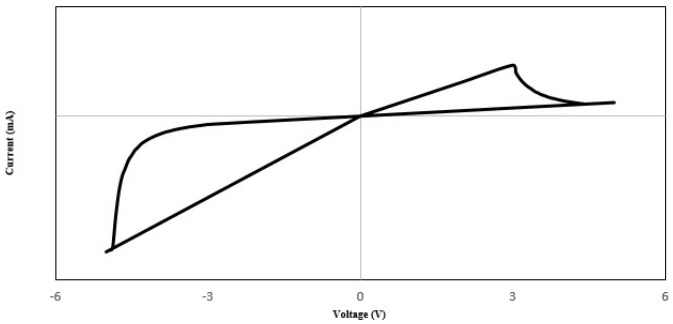


Fig. 4. : Memristor Current versus input voltage for sinusoidal input voltage.

### B. MTCAM Hardware Emulation

Using the memristor emulator, we next created an MTCAM row. The primary cell described earlier is instantiated numerous times. Both the read and write operations are performed by the proposed design. A match signal is used to indicate that the row contains the same data as the input. Functionality was simulated and verified using VHDL. The synthesizable code occupied less than 0.29 % of the Xilinx VIRTEX® 7 XC4VSX35 FPGA logic for 8 bit row width. Figure 5 shows the MTCAM row simulation result for a stored word "11111111".A short summary of basic information about the emulator HW is given in Table II for different memory width. It worth to note that the Logic Utilization increases linearly with the MTCAM row width. In addition to that, for 32 bit row the maximum delay is about 2.45 ns.

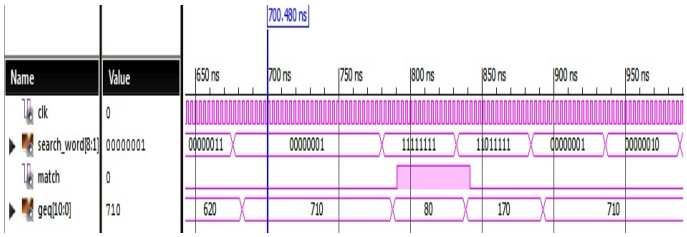


Fig. 5. MCAM Row simulation results.

To support large array sizes, larger FPGAs could be used or multiple FPGAs could be stacked where cross FPGA communication can be established using fast differential I/O capability and source-synchronous signalling. Since memories are mostly self-contained units, cross FPGA communication can be easily minimized.

TABLE II
AREA UTILIZATION AND MAX DELAY OF MTCAM ROW REALIZATION ON THE XILINX VIRTEX® 7 XC4VSX35 FPGA. THE CIRCUITS WERE SYNTHESIZED USING VIVADO 2016.1.

| $MTCAM\ WIDTH$ | $LOGIC\ UTILIZATION$ | $MAX\ DELAY(ns)$ |
|---|---|---|
| 8 | 889 / 0.29% | 1.96 |
| 16 | 1761 / 0.58% | 1.993 |
| 32 | 3514 / 1.16% | 2.445 |

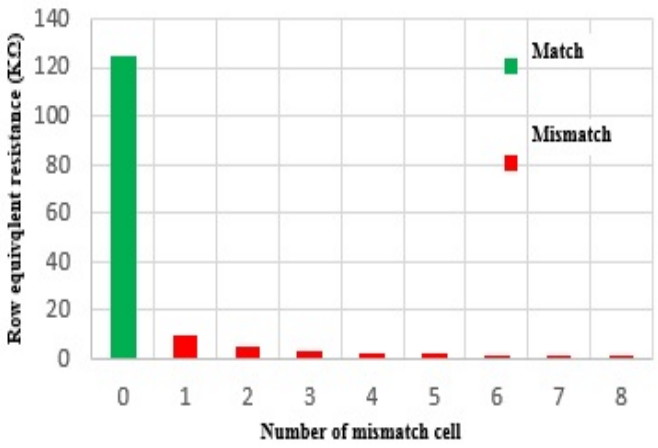


Fig. 6. Match line equivalent resistance versus Number of mismatching bit-cell.

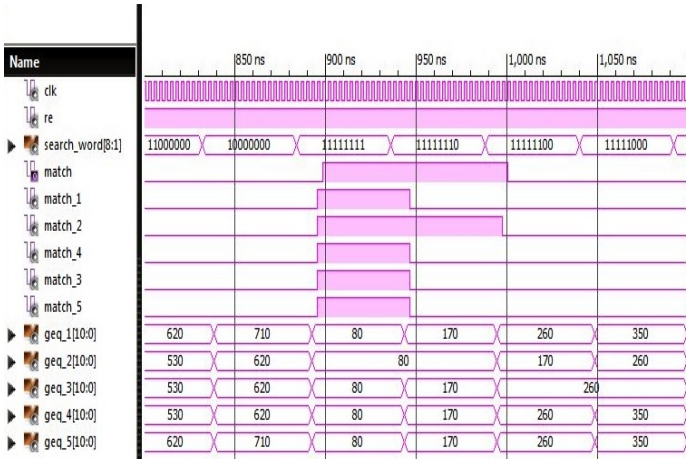


Fig. 7. 2 D MTCAM array simulation

The matching scheme is based on the equivalent resistance within a row. Note that the mismatch model for the M-TCAM bit-cell is the equivalent pull down resistance consisting of transistor resistance and state 1 memristor resistance “Ron”. On the contrary, in case of match, it is equivalent to the state 0 memristor resistance “Roff” which disconnects the match line to the ground.

The proposed emulator provides as an output, the equivalent resistance of each row which depends on the number of mismatching cells. Hence depending on the equivalent resistance we have defined a threshold between the match and mismatch state. Figure 6 shows the variation of the equivalent virtual row resistance with the number of mismatching bit-cell per 8 bit MTCAM row.

Accurate emulation for realistic 2D memory array sizes is essential to mimic realistic MTCAM. In order to achieve this goal and verify the functionality of the proposed MTCAM, we wrote a Python script that creates VHDL netlists for practical memory size and sweep different parameters and data patterns. Thus, the emulation memory can be filled with any required data pattern content. Figure 7 shows a sample hardware simulation results of a 2 D array. In this simulation, fives 8 bits words have been stored in the proposed M-TCAM. Initially the match signal is ’0’ and the input signal research_word changes from the binary bit pattern "00000000" to "11111111". Match is the output signal. It becomes ’1’ when the search word matches with one of the stored word. Furthermore, for each MTCAM row we provide as an output the equivalent admittance (inverse of the equivalent resistance).

## IV. Conclusion

In this work, we have presented a hardware implementation of a memristor ternary content addressable memory (MCAM). First we modeled the threshold based bipolar memristor device. The primary 2T2M bit-cell was then developed with the realistic memristor as the main building block. With the instantiation of this component we have shown the emulation for one row along with the technique to expand it into a 2D MCAM array. Its low FPGA HW resources witch are very promising to support much larger memristor based TCAM. As a CAM is the fundamental unit of associative processing (AP), we plan to integrate this emulator in a simple AP architecture. It serves as the first step for hardware verification where simple arithmetic operations are tested providing preliminary performance metrics.

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