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# Wavy Architecture Thin Film Transistor for Ultra-High Resolution Flexible Display

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A novel wavy shaped thin-film-transistor (TFT) architecture, capable of achieving 70% higher drive current per unit chip area when compared to planar conventional TFT architectures, is reported for flexible display application. The transistor due to its atypical architecture does not alter the turn-on voltage or the OFF current values, leading to higher performance without compromising static power consumption. The concept behind this architecture is expanding the transistor's width vertically through grooved trenches in a structural layer deposited on a flexible substrate. We show operation of Zinc Oxide (ZnO) based TFTs down to a bending radius of 5 mm with no degradation in the electrical performance or cracks in the gate stack. We finally demonstrate flexible low power LEDs driven by the respective currents of the novel wavy, as well as, conventional coplanar architectures, where the novel architecture is able to drive the LED at 2× the output power, 3 mW *vs.* 1.5 mW, which demonstrates the potential use for ultra-high resolution displays in an area efficient manner.

Display technology is one of the most prominent technologies in the consumer electronics genre. Two important device components for display technology are light emitting devices and backplane transistors to control them. A number of different Flat Panel Display (FPD) technologies have been introduced in the market. The most successful FPD technologies are both active matrix liquid crystal display (AM-LCD), and active matrix organic light emitting display (AM-OLED). Forecasts for OLED displays expect market growth from $16bn in 2016 to about $57bn in 2026[1]. For AMOLED, the active-matrix backplane consists of an array of the thin film transistor (TFT) pixel circuits, each of them directly controls the charges on RGB subpixels[2]. Unlike passive matrix LEDs, only the selected pixel receives a charge, through a driving TFT, and thus no interference comes from neighboring pixels[3]. As a result, the resolution of active matrix based displays can be dramatically increased in comparison to passive matrix displays. The current market dominant product of Full High Definition (FHD) AM-LCDs has pixel numbers around three millions (1920×1080×3(RGB))[4]. Future 8K displays are expected to have more than 33.2 megapixels (4320×7680×3(RGB)), more than 300 Pixels Per Inch (PPI), and a fast frame rate (> 240 Hz) in order to suppress the motion blur effect at such high resolution[5]. The essential requisite for achieving these features is a high field-effect mobility, μ, in thin-film transistors (TFTs). For example, 8K displays switching at 240 Hz frame rate demand field effect mobility around 10–20 $cm^2/V.s$, and even higher values are desired for future displays[6]. This is because a higher μ induces a higher drain current, thus enabling the TFTs to switch faster and/or occupy a smaller pixel area. A typical current controlled active matrix circuit, which controls individual OLED or LCD pixels, has 4 TFTs and 2 capacitors[3, 7, 8]. Thus, a smaller TFT area is required for achieving both higher resolutions, as well as, higher pixel fill factor, which is defined as the ratio of the light emitting area over the total area of the pixel. Another important motivation for scaling TFT sizes is that the allowed pixel size decreases as the number of Pixel Per Inch (PPI) increases which is critical for future high resolution mobile applications such as the use of flexible displays for point-of-care medical

diagnostic testing[9]. For example, the pixel size for 500 PPI is only 50.8× 16:9 μm$^2$[4]. Hence, it is imperative that the TFT size be scaled down along with the pixel size to be fitted inside such a small pixel area.

Amorphous Oxide Semiconductors (AOS) have been excellent TFT channel material candidates for future large area FPD since their typical field effect mobility values for n-type oxides have been in the range of 10 cm$^2$/V.s for Indium Gallium Zinc Oxide (InGaZnO – or popularly IGZO) based devices, and 20 cm$^2$/V.s for Indium (In) rich films, which are within the required range for future 8K displays[10]. However, in order to reduce the area occupied by TFT circuitry, gate length scaling has been the traditional route of downsizing TFT area[11-13]. Various studies have been conducted to study gate length scaling effects on n-type oxides such as ZnO[14], InGaZnO[4, 15], and InZnO[16]. For the case IGZO, scaling $L_g$ below 5 μm has been shown to induce short-channel effects (SCE) such as negative $V_T$ values, higher OFF current, higher subthreshold slope, lower output resistance, and lower saturation field effect mobility[4, 15]. SCE lead to both higher static power consumption, and lower frame rates for scaled down pixels due to lower switching speeds as a result of mobility degradation. While there are attempts to mitigate SCE at small $L_g$ such as the use of double-gate TFT architecture[17, 18], which have shown higher transconductance and lower subthreshold values when compared to single gate architecture, they have disadvantages such at a higher integration complexity due to the added requirement of aligning both gates, and an overall higher cost per transistor which might be problematic for large-area displays. Besides, negative $V_T$ values are still noticed for $L_g$ below 5 μm such as in the case of IGZO[17]. On the other hand, scaling down transistor width has not been shown to induce SCE[4], which means there is an open window for improvement in terms of packing more device width within the same chip area. Therefore, a novel TFT architecture is proposed which allows for increasing the device width vertically without extra chip area penalty on flexible substrates through etching deeps trenches in a structural layer. The novel architecture thus allows boosting performance of the smallest reliable $L_g$ without

changing $V_T$ or $I_{OFF}$. We have previously shown the same architecture on rigid substrates, where it has demonstrated the ability to leverage 2× drive current per unit chip area when compared to planar TFT[19-22], as well as, improve performance of digital circuits significantly[23-25]. In this work, we demonstrate the novel architecture ability to drive LEDs at 70% higher currents compared to conventional coplanar TFTs integrated on the same substrate.

**Figure 1(a)** illustrating the device schematics for both coplanar thin film transistor architecture (top) and the proposed wavy architecture (bottom) which shows the added device width due to sidewalls of the etched structural layer (α-Si in this case). It also shows the different materials in the device gate stack of the ZnO TFT. The wavy shape of the TFT channel is why it is denoted as the wavy channel (WC) TFT, as opposed to co-planar TFTs. **Figure 1(b)** show the fabricated WC and planar TFTs in the same die, where it shows both devices occupying identical chip area. **Figures 1(c and d)** show images of peeled-off TFT and LED substrates. Substrate thicknesses allows for achieving bending radii down to 5 mm. **Figure 1(e)** shows a digital image of a planar device, which has channel length of 50 µm and channel width of 240 µm. **Figure 1(f)** shows a digital image of the flexible red (640 nm) LED under forward bias. The LED color was arbitrarily chosen to illustrate the potential of the WC TFT to improve the drive current per unit chip area through power output measurement. Since we designed the experiment to allow for comparison of both WC and planar devices, mask design laid out both devices within the same die to eliminate variation of electrical characteristics such as film resistivity across the wafer, as illustrated in **Figure 1(b)**.

**Figure 2(a)** shows a side view SEM image of TFT that has 3 µm wide 'fins' and 6 µm fin pitch, which is why we denote as 3 µm 1-1 device. This device possesses 70% larger width when compared to coplanar devices due to it's 2 µm high sidewalls and 6 µm fin pitch. Figure **2(b)** shows a schematic of the ZnO/$Al_2O_3$/Al layers in the gate-stack of the fabricated TFT, which is fabricated on top of an etched strctural layer, α-Si, that is covered by $Al_2O_3$ for electrical isolation from the fabricated devices. **Figure 2(c)** shows a false colored cross-

sectional SEM image showing the various layers in the gate stack. This achitecture allows for conformal deposition on the both the sidewalls and bottom of the trenches due to the 75° sidewal profile angle. $SF_6$ etch gas flow rate was optimized to allow for smooth side walls, thus avoiding roughness induced gate stack electrical shorting problems. The conformal deposition and smooth sidewalls mitigate problems that arise in TFT nonplanar architectures such as the vertical TFT architecture, which suffer from both higher gate leakage and gate-to-source/drain overlap paristic capacitance when compared to nonplanar vertical architectures[12, 13]. Also, the proposed architecture allows for self-alinged source/drain deposition, thus elminating parastic capaciatnace problem due to gate to source/drain overlap.

**Figure 3(a)** shows an XRD image of the deposited polycrystalline ZnO film on a Si substrate showing two dominant (100) and (002) Wurtzite peaks. The crystallite size was calculated to be ~22 nm from Scherrer formula, which was also confirmed by SEM image of the deposited film in **Figure 3(b)**. ZnO was chosen as a channel material since it could be deposited with Atomic Layer Deposition (ALD) which allows for highly uniform/confromal despositions leading to uniformity of electrical properties across the wafer. However, the novel wavy architecture is compatible with other channel deposition methods such as DC and RF magnetron sputtering since the trench sidewall slanted profile allows for ample coverage of sputtered species such as DC sputtered Al in the case of **Figure 2(c)**. This means the novel architecture is material agnostic, and thus could be applied to channel material deposited by other deposition methods such as IGZO[4], and IZO[16].

**Figure 4(a)** shows electrical transfer characteristics, dual sweep, of planar and WC TFTs. The first thing to notice is that both devices possess similar 'OFF' current values, at $V_{GS}$ = 0V, which means that both devices would enable similar OFF state static power consumption. Both architecture have $V_{ON} \cong -2.2V$, which is defined as the voltage at which the drain current increases exponentially from the noise floor, i.e. gate leakage[26]. The threshold voltage, $V_T$, of both devices was extracted in the saturation regime from the point of the highest first derivative

of $\sqrt{I_{ds}}$ *vs.* $V_{gs}$ curve[27]. The planar and WC TFTs $V_T$ values were 6.6V and 4.2V, respectively. Output characteristics are shown in **Figure 4(b)**, which demonstrates 70% higher drain current values for WC devices, which are proportional to the extra device width. Minimum subthreshold slope, SS, values for planar and WC devices were 0.4 and 0.2 V/decade. The lower SS and $V_T$ values for WC TFT could be attributed to higher electric field at trench corner, i.e. corner effects, as was demonstrated from our previous work[19, 21].

To test the flexibility of the WC TFT, we tested it at a smaller bending radius, R, of 5 mm, as shown in **Figures 4(c and d)**. **Figure 4(c)** shows the transfer characteristics in linear and saturation regimes, the device 'ON' current does not degrade with bending down to R = 5 mm. Also, gate leakage values remain below 10 nA for R = 5 mm, and does not show signs of increasing with further electric cycling. The hysteresis in transfer characteristics remained less than 0.2V. Saturation field effect mobility, $\mu_{sat}$ was calculated according to the MOSFET expression[28]:

$$\mu_{sat} = \left(\frac{2L_g}{W}\right)\left(\frac{1}{C_{ox}}\right)\left(\frac{d\sqrt{I_{DS}}}{dV_{GS}}\right) \quad (1)$$

$C_{ox}$ is the oxide gate capacitance per unit area, $L_g$ is the gate length, and W is the device width. We took into account the 70% higher width in the saturation mobility calculation. This demonstrates the potential of this device architecture to radically increase output current per unit chip area without compromising static power consumption. **Figure 4(d)** demonstrates that the output characteristics did not degrade with mechanical bending as $I_{ds} = 1 \times 10^{-3}$ A down to R = 5 mm.

To test the potential of the novel architecture for flexible display application, low power red light (640 nm) LEDs were mounted on a flexible substrate, and optical power outputs of the LED when driven by the respective drive currents of both the planar and WC TFTs were measured. **Figure 5(a)** shows typical diode I-V characteristics of the off-the-shelf LED with a

turn-on voltage of ~1.6V. **Figure 5(b)** shows the output power *vs.* injection current, which shows that for the injection currents of planar TFT (600 μA) and WC TFT (1100 μA), the device is operating in the linear region, as shown in the inset of **Figure 5(b)**. This demonstrates that the optical output of the LED operated by WC TFT is ~ 2× the optical power emitted by the LED operated by coplanar TFT, i.e. 3 mW *vs.* 1.5 mW, under similar gate and drain bias conditions for both devices. **Figure 5(c)** shows the Electro-luminescence (EL) measurements of the LED when driven by the respective currents of the planar and 3 μm 1-1 WC TFTs. The LED driven by the WC TFT exhibits more than 2× intensity at the peak wavelength of 640 nm when compared to the LED driven by coplanar TFT, when both are biased under similar gate and drain bias conditions. This shows that the WC TFT enables pixel area down-scaling and higher pixel fill factors when compared to planar TFT providing identical drive currents.

In conclusion, we have demonstrated a novel flexible nonplanar TFT architecture which is capable of achieving 70% higher device width within the same chip area when compared to TFT coplanar architecture. The novel nonplanar TFT achieves 70% higher drive current, lower subthreshold slope, and lower $V_T$ values when compared to coplanar TFTs even when bent down to 5 mm bending radius. We have demonstrated flexible LED driven by the respective currents of the novel and coplanar TFTs, where flexible LED driven by the WC TFT shows 2× the output power when compared to the planar TFT occupying identical chip area. This means the novel wavy channel architecture can occupy 70% lower area when compared to planar TFT at an identical drive current, and thus enable higher pixel fill factor, as well as, higher number of pixels per inch (PPI). This provides a potential solution for future ultra-high-definition flexible displays of beyond 8K resolution. Future designs of WC TFT could lead to more than 2× higher drive current per unit chip area if given tighter fin pitches and higher aspect ratio trenches.

**Experimental Section**

*Fabrication*:

We start by spinning polyimide PI-6211 low stress polymer from Dupont on a Si substrate at 2000 RPM and curing it at 360$^{o}$C which yields 9 µm thick film. We then deposit a 200 nm $SiO_2$ film using plasma enhanced chemical vapor deposition (PECVD), which acts as an adhesion layer and etch stop layer for the following layer. A 2 µm thick α-Si film is then deposited at 250$^{o}$C which acts as the structural layer for trench formation. We then etch the 2 µm α-Si layer using $SF_6$ based Reactive Ion Etching leading to a 75$^{o}$ sidewall angle. We then deposit 50 nm $Al_2O_3$ layer using atomic layer deposition (ALD) in order to electrically insulate the devices from the α-Si structural layer. This is followed by deposition of 200 nm of Al using DC magnetron sputtering and patterning it by lift-off technique. The wafers are then loaded one more time in ALD chamber, where two subsequent deposition of 50 nm $Al_2O_3$, which acts as a gate dielectric, and 40 nm of ZnO layer, which acts as the channel material, are done without breaking vacuum. The ZnO layer is then patterned using Buffered Oxide Etchant (BOE) for 10 seconds. This is followed by deposition of Ti(50 nm)/Au(200nm) source/drain layers, which are also patterned using lift-off technique. The devices are annealed in air at 200 $^{o}$C for 1 hour to improve the electrical characteristics. Finally, a photoresist passivation layer is applied to protect the channel from environmental degradation and etch the gate oxide to allow access to the Al gate pads. The devices are finally peeled-off from the Si substrate and transferred on a PDMS substrate. ZnO film is also independently deposited on $SiO_2$/Si substrate for XRD characterization. Also, a 2 µm α-Si film is deposited on $SiO_2$(300nm)/Si substrate, which is etched using the exact process, followed by deposition of Al/$Al_2O_3$/ZnO gate stack layer for cross-sectional scanning electron microscope (SEM) imaging.

For LEDs, interconnections are first patterned on a polyethylene terephthalate(PET) aluminum metallized film (Good Fellow 0.006mm, resistivity of 1.4 Ohms/Square) using 1.06 µm ytterbium-doped fiber laser (PLS6MW Multi Wavelength Laser Platform, Universal Laser

Systems). Near Infrared surface mounted devices (SMD) LEDs (Vishay Semiconductors, turn-on voltage of 1.6 V and dimensions of 1.6 mm x 0.8 mm x 0.6 mm) were bonded on the patterned PET film via Flip Chip technology (Fine Placer Femto Die Bonder) and conductive silver epoxy (Electron microscopy Sciences).

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**Figures**

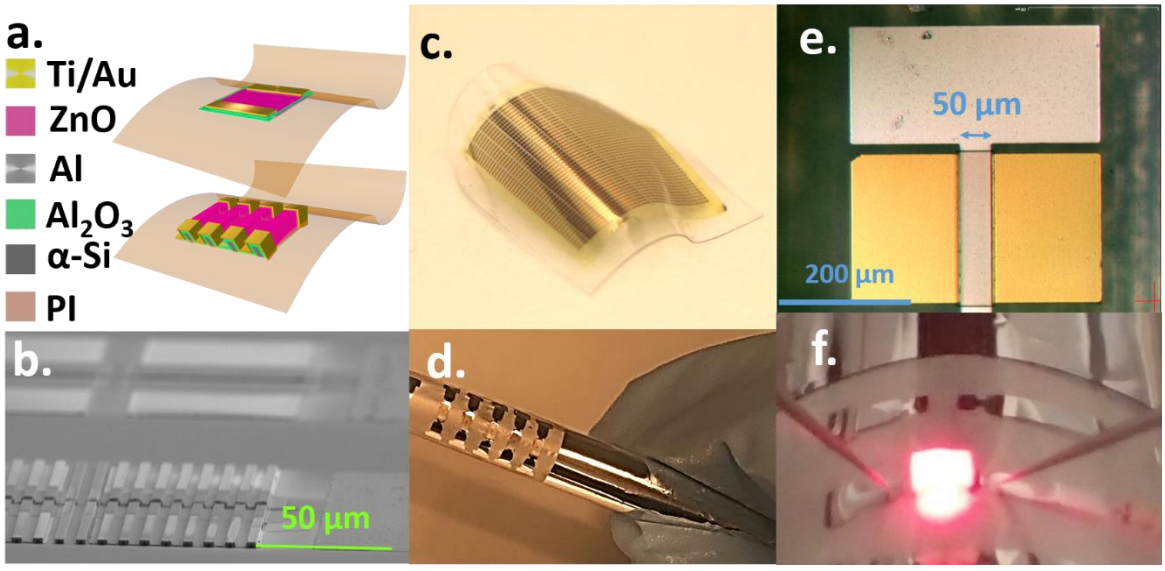


**Figure 1. a)** 3D schematic of coplanar and wavy channel thin film transistors (TFTs) on a flexible substrate. **b)** Side view SEM of planar(top)and wavy channel (bottom) TFTs. **c)** Digital image of peeled-off TFTs which is transferred on a PDMS substrate, and **d)** flexible LEDs substrates showing flexibility down to 5 mm bending radius. Digital images of a **e)** planar TFT having $L_g$ = 50 µm and W = 240 µm and a **f)** flexible red LED under forward.

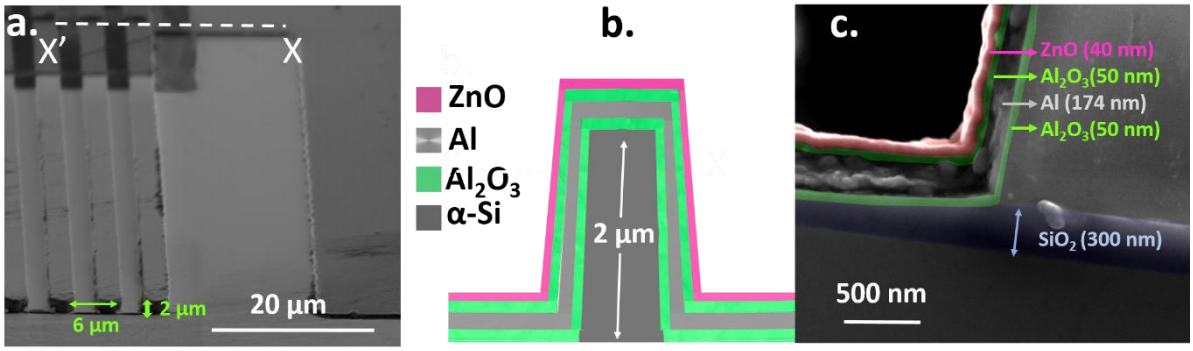


**Figure 2. a)** SEM image of wavy channel TFT showing a side view of the 3 µm wide fins and 6 µm fin pitch. **b)** Cross-sectional schematic showing the various layer in the gate stack. **c)** A false-colored cross-sectional SEM image of the TFT gate-stack showing a stack of ZnO (40 nm)/$Al_2O_3$ (50 nm)/Al (170 nm)/ $Al_2O_3$ (50 nm).

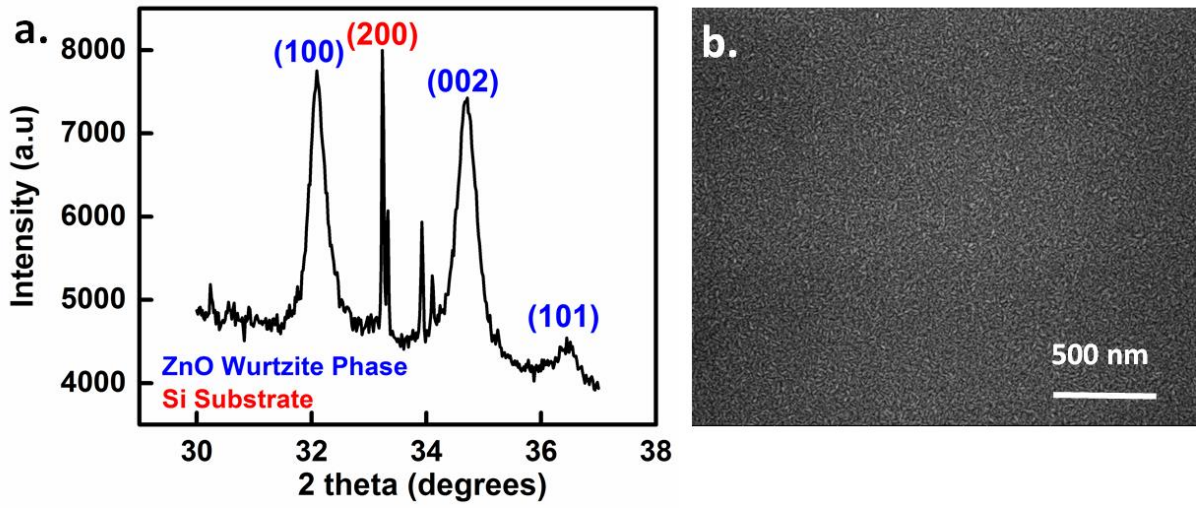


**Figure 3. a)** X-ray Diffraction pattern of the ZnO/$SiO_2$/Si thin film showing the presence of dominant (100) and (002) Wurtzite peaks, and weak (101) peak. Scherrer formula have yielded grain size of ~22 nm for both peaks, which was confirmed by top-down SEM image of the ZnO film in **b)**.

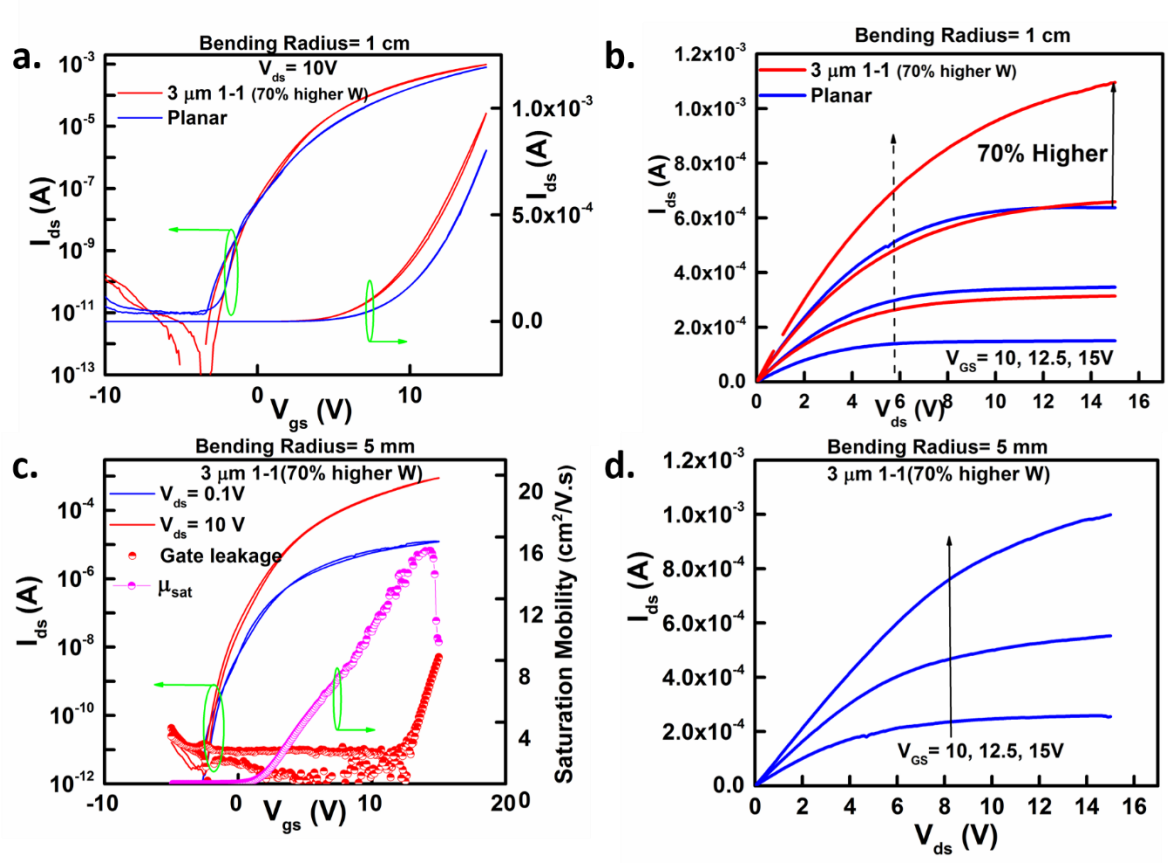


**Figure 4. a)** High $V_{ds}$ (saturation region) transfer and **b)** output characteristics of both planar and 3 µm 1-1 wavy channel TFTs devices showing 70% higher output current for wavy channel TFT when compared to planar TFT at a bending radius, R, equal to 10 mm. **c)** linear and saturation regions transfer characteristics, and saturation mobility calculation of 3 µm 1-1 wavy channel TFT at R = 5 mm. **d)** Output characteristics of 3 µm 1-1 wavy channel TFT at R = 5 mm.

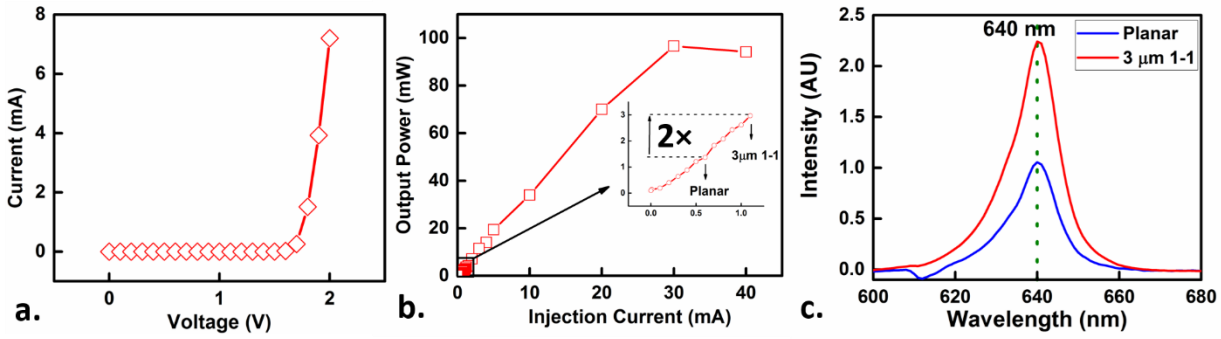


**Figure 5. a)** LED under forward bias showing a turn-on voltage of ~1.6 V. **b)** Output power vs. injection current characteristics showing a linear relationship for the injection currents of interest, 0.6 mA and 1.1 mA, corresponding to the planar and wavy channel TFTs, respectively. **c)** Electro-luminescence of the LED driven by 3 µm 1-1 WC TFT and coplanar TFT respective current under similar gate and drain bias conditions.