A Highly Sensitive RF-to-DC Power Converter with an Extended Dynamic Range

Abdullah Almansouri, Mahmoud Ouda and Khaled N. Salama
Computer, Electrical and Mathematical Science and Engineering Division
King Abdullah University of Science and Technology (KAUST), Thuwal, 23955-6900, Saudi Arabia
Email: {abdullah.almansouri, mahmoud.ouda, khaled.salama}@kaust.edu.sa

***Abstract*—This paper proposes a highly sensitive RF-to-DC power converter with an extended dynamic range that is designed to operate at the medical band 433 MHz and simulated using 0.18 µm CMOS technology. Compared to the conventional fully cross-coupled rectifier, the proposed design offers 3.2× the dynamic range. It is also highly sensitive and requires -18 dBm of input power to produce a 1 V-output voltage when operating with a 100 kΩ load. Furthermore, the proposed design offers an open circuit sensitivity of -23.4 dBm and a peak power conversion efficiency of 67%.**

***Keywords*—RF-DC converter, energy harvesting, wireless powering, self-bias, rectifier.**

I. Introduction

Wireless powering is a fundamental requirement for energizing myriad battery-less devices, such as RFIDs [1], implanted biomedical devices [2-4] and wireless sensors [5]. Depending on the application, frequencies ranging from low MHz [2, 4] up to UHF [1] are used. Due to the vast operating conditions, it is favourable to have a wireless power receiver that is capable of operating at the maximum level of efficiency and undertaking a broad range of both input and output power levels.

An RF-to-DC converter is a key component within a wireless power receiver and is responsible for converting the received RF signal into a DC voltage, as shown in Fig. 1. In general, the performance of an RF-to-DC converter is evaluated by its sensitivity, power conversion efficiency (PCE) and dynamic range (DR). Sensitivity is the minimum input power required to generate an output DC voltage of 1 V. The DR is the range of input power levels in which the converter works efficiently. It is ultimately ideal to have a high and as constant as possible PCE over the whole possible range of input power, as a wider DR means that the rectifier is capable of operating efficiently at a broader range of RF power. However, in practice the harvested energy leaks back to the RF input throughout the rectifying circuit, causing a significant drop in the PCE at higher input power levels [6].

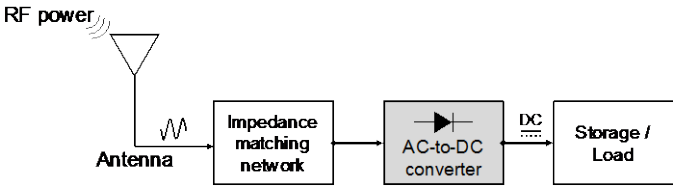

Fig. 1. Block diagram of wireless power receiver

Fig. 2 shows a range of RF-to-DC rectifiers that have traditionally been implemented. Diode-based rectifiers [7], such as Dickson (Fig. 2a)[8], have good performance at high RF power. However, they suffer from bad sensitivity and perform poorly at low RF power given that diodes require a firm dropout voltage (v_{th}) to turn on. Fully cross-coupled rectifiers (FX) solved the sensitivity problem by applying the RF signal differentially across four rectifying transistors, as shown in Fig. 2b [1]. As a consequence, the FX architecture has a smaller dropout voltage (less than the threshold voltage)

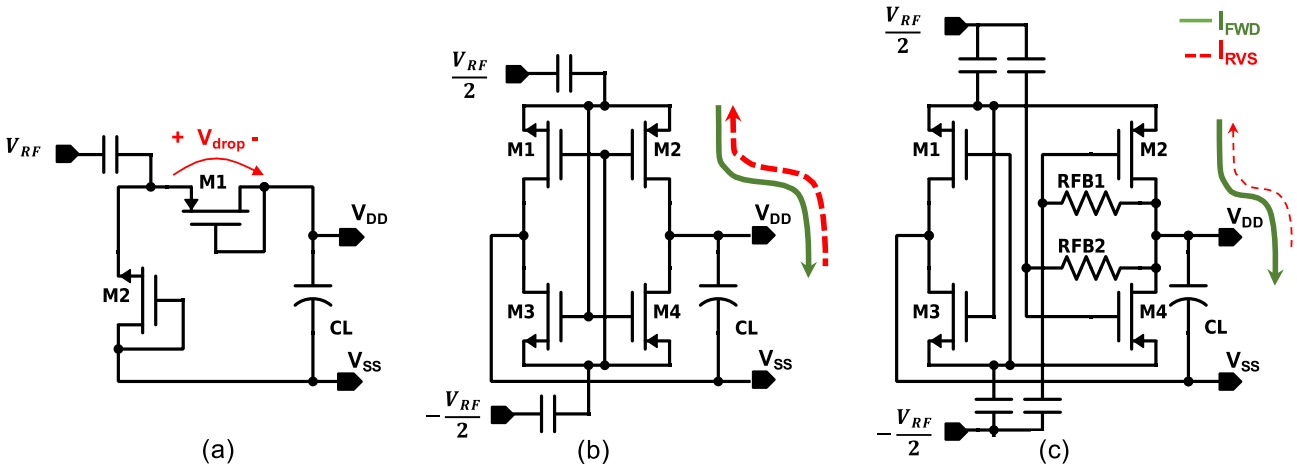

Fig. 2. Schematics of (a) Dickson [8], (b) fully cross-coupled (FX) [1] and (c) self-biased [6] rectifier architectures

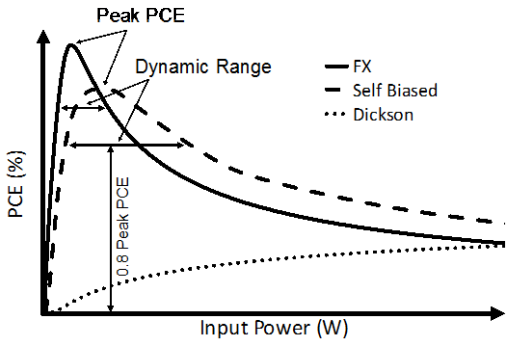

Fig. 3. Power conversion efficiency (PCE) comparison for the different architectures

and is capable of operating efficiently at a relatively low RF power; in other words, the FX architecture has a high PCE and good sensitivity. Nonetheless, this design suffers from a poor DR due to the presence of a reverse current (I_{REV}) that leaks part of the harvested energy back to the RF input. Since MOSFETs are bi-directional devices, when the accumulated output DC voltage becomes larger than the instantaneous RF input voltage, the current flows back towards the input [6]. This reverse current becomes dominant as the RF power increases, which then restricts the efficient operation of the FX architecture to a tight range of RF power. Self-biased design introduced by [6] reduced I_{REV} by utilizing feedback resistors to limit the conduction of the rectifying devices, shown in Fig. 2c. However, limiting the rectifying transistors' conduction also reduced the forward current (I_{FWD}), which resulted in a drop of the peak PCE and poor performance at low RF power. Moreover, the added resistors consume a large area and introduce lots of parasitics, which is not favourable in the RF application. Fig. 3 presents a comparison of the power conversion efficiency at varying input power levels for these different architectures. In short, the FX architecture has the highest PCE for a very narrow region; the self-biased design sacrifices the peak PCE and efficiency at low input power to offer a wider dynamic range; and the Dickson architecture's performance becomes acceptable only at a relatively high RF power.

In this work, we present an RF-to-DC power converter that has a high sensitivity and wide dynamic range that is capable

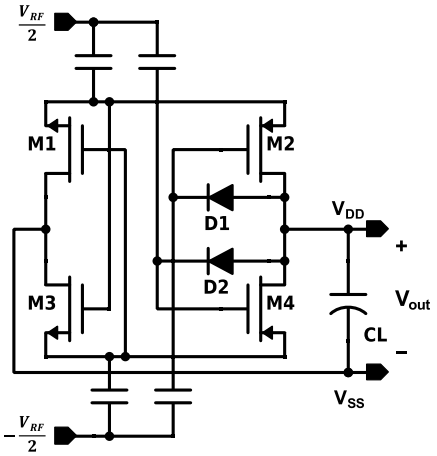

Fig. 4. Proposed rectifier

of operating efficiently at the medical band 433MHz. The paper is organized as follows: Section II describes the proposed design and its basic working methodology, Section III compares the performances of the different architectures and Section IV presents conclusions.

II. Proposed Design

A schematic of the proposed design for the enhanced performance is shown in Fig. 4. The design is based on the cross-coupled configuration for maintaining the high sensitivity feature. Moreover, it realizes the self-biased concept by utilizing two feedback diodes, namely D1 and D2, that are reverse biased for the RF signal and forward biased for the DC voltage. The distinguishing advantage of using diodes is that they provide variable feedback resistors depending on the RF power level while isolating the RF signal from the output node. In general, the threshold voltage of the diodes determines the voltage level at which a diode's behaviour for the forward signal changes from open-circuit ($R_{diode} \approx \infty\ \Omega$) to short-circuit ($R_{diode} \approx 0\ \Omega$). For low RF power, the voltage drop across the diodes is smaller than the threshold voltage; as such, the diodes act as an open circuit. For high RF power, the voltage drop across the diodes is larger than the threshold voltage, which results in the diodes acting as a short circuit for the DC voltage.

The operating points for the different architectures has a critical impact on determining I_{FWD} and I_{REV}, hence, the overall performance. For the FX architecture (Fig. 2b), the gate voltage is biased by a relatively high voltage ($|V_{G,FX}| = V_{RF}/2$); this allows a large current to flow through the transistor and hence enables the rectifier to operate effectively at low RF power. However, at high RF power, the drain voltage (V_D) becomes significant and can be much larger than the instantaneous source voltage (V_S). As a consequence, the strong bias at the gate allows a large current (I_{REV}) to leak from the drain back to the source. For the self-biased architecture (Fig. 2c), the gate bias voltage is reduced due to the presence of the feedback resistor ($|V_{G,\text{Self-biased}}| = V_{RF}/2 - V_{DD}$). The transistor's conduction is consequently reduced, limiting the flow of I_{REV}. However, this approach is harmful at low RF power where I_{REV} is less significant and the need to enhance I_{FWD} by improving the conductivity of the rectifying transistors is critical. When the proposed design (Fig. 4) is driven by low RF power, V_{DD} is relatively small, which means that the diode remains off. As a consequence, the rectifying device acts as the FX design and inherits its efficient performance at low power. At high input power, V_{DD} increases and the voltage drop across the diode becomes large enough to turn the diode on. The output DC voltage consequently passes to the gate of the rectifying transistor, which results in the rectifying device acting as the self-biased architecture (and hence inheriting its efficient performance at high power). Table I summarizes the current's flow in the various architectures and their impact on the PCE performance at different power levels.

TABLE I. CURRENT FLOW AND PCE PERFORMANCE

Architecture	Forward current (I_{FWD})	Reverse current (I_{REV})	PCE at low RF power	PCE at high RF power
Dickson	Low	Low	Low	Medium
FX	High	High	High	Low
Self-biased	Low	Low	Medium	High
Proposed	**Medium**	**Low**	**High**	**High**

III. RESULTS AND DISCUSSION

The proposed rectifier is simulated using 0.18 µm CMOS technology. For the sake of a fair comparison, the Dickson, self-biased and FX architectures are also simulated in this work. The test is conducted by sweeping the input voltage for each design and extracting the steady state equivalent input power, output voltage and conversion efficiency.

Fig. 5a shows the PCE versus the input power for the different architectures, with a 100 kΩ load resistance (R_{Load}) and 433MHz RF frequency. The peak PCE for the proposed design is 67%, compared to 76% and 53% for the FX and self-biased designs, respectively. The Dickson architecture's performance is poor for this range of input power, with a maximum PCE of 29% at 40 µW RF power. The DR is defined as the range of the input power at which the rectifier PCE is greater than 80% of its peak PCE. By setting the DR of the FX as a reference, the proposed design offers 3.2× wider DR (compared to 2× for the self-biased design). The DR is not applicable for the Dickson architecture within this range of RF power.

Fig. 5b shows the current flowing in the rectifier when the RF power is fixed at 10 µW. The FX architecture offers the highest I_{FWD}; however, approximately 33% of the harvested energy leaks back to the RF input. The self-biased architecture has a negligible I_{REV}; but the significantly reduced I_{FWD} results in the architecture having a net performance that is about the same as the FX design. The proposed design also offers a negligible I_{REV}; however, as it has a higher I_{FWD}, it offers the best net performance.

Fig. 6 shows the output voltage at different power levels. Compared to the Dickson, FX and self-biased architectures, the proposed design is capable of producing a higher output voltage for a wide range of RF power. For instance, when an input power of 20 µW is utilized, the proposed design is able to generate 91%, 27% and 10% higher DC voltage than the Dickson, FX and self-biased architectures, respectively. The proposed design also offers the best sensitivity among the designs considered: it requires only 16 µW (-18 dBm) to produce 1 V at the output, compared to 47.62 µW (-13.2 dBm) for the Dickson design, 41.8 µW (-13.8 dBm) for the FX design and 20.5 µW (-16.9 dBm) for the self-biased design. Moreover, when setting R_{Load} to open circuit (R_{Load} = 1 MΩ, to implicate the self-leakage in the storage element CL), the obtained open-circuit sensitivity for the proposed design is -23.4 dBm, compared to -15.1 dBm and -20.5 dBm for the FX and self-biased architectures, respectively.

Fig. 7a shows a layout of the proposed architecture designed in 0.18 µm CMOS technology. The layout also includes the RF and DC pads that are required for testing. Fig. 7b is an enlarged image of the active area, which has a geometry of 70 × 120 µm.

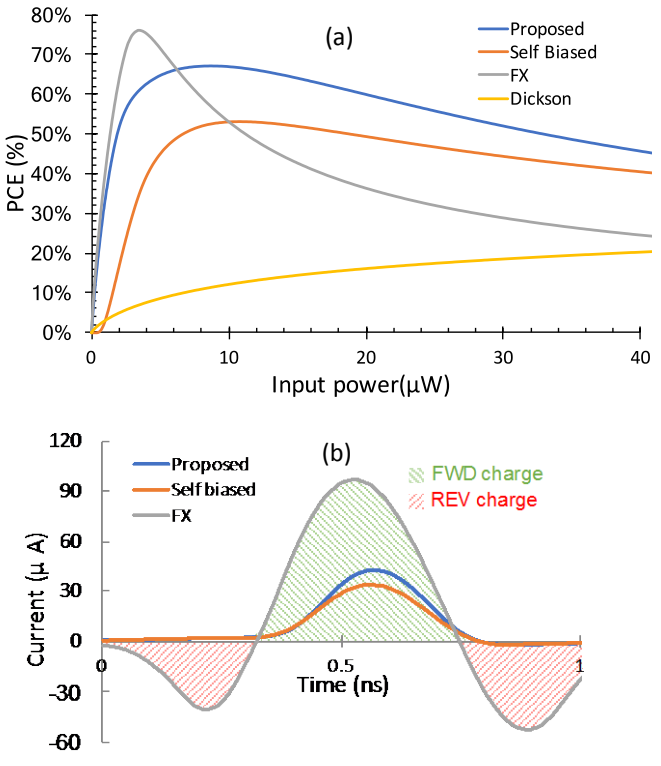

Fig. 5. (a) Simulated power conversion efficiency (PCE), and (b) transient current behaviour for the different architectures at 10 µW input RF power. R_{Load} is 100 kΩ.

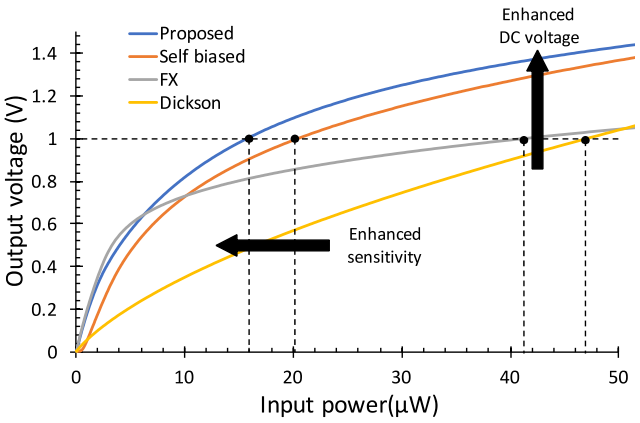

Fig. 6. Simulated DC output voltage versus RF input power

TABLE II. PERFORMANCE COMPARISON

Architecture [a]	Technology	Area	Number of stages	Peak Power Conversion Efficiency (PCE)	Normalized [b] dynamic range [c] ($P_{in\_max.}$ / $P_{in\_min.}$)	Sensitivity [d]	Open circuit sensitivity [d, e]
	µm	$\times 10^3$ µm^2	stage	%	%	dBm	dBm
Proposed	**0.18**	**8.4**	**1**	**67**	**324**	**-18**	**-23.4**
Fully cross-coupled (FX)[f] [1]	0.18	5	1	76	100	-13.8	-15.1
Self-biased [f] [6]	0.18	17	1	53	197	-16.9	-20.5
Adaptive [f] [9]	0.18	8.4	1	77	158	-17.7	-21.7
Auto-calibrating V_{th} compensation [10]	0.18	150	1	34	N.A	-14	-18.4
Fully cross-coupled with inter-stage RF injection [11]	0.18	88	3	10	80	-4.1	-11.2

[a] All architectures are operating at 433 MHz with a 100 kΩ load, [b] Normalized to the fully cross-coupled architecture, [c] 80% of the peak PCE, [d] Pin at Vout = 1V, [e] RLoad = 1 MΩ, [f] simulation results are reproduced in this work

Fig. 8 utilizes a post-layout simulation to compare the performance of the rectifiers, including the parasitics. The PCE of both the proposed and self-biased architectures are normalized to the FX design. Depending on the RF power, the proposed design is capable of producing up to an 84% enhancement of the PCE for RF power levels greater than 6 µW. On the other hand, the self-biased design provides up to 53% improvement for RF power levels greater than 14 µW.

Table II compares the performances of different architectures operating at 433 MHz with a load resistance of 100 kΩ and designed using 0.18 µm CMOS technology. The proposed design offers a considerably wider DR and the highest sensitivity while maintaining a high PCE and a relatively small area.

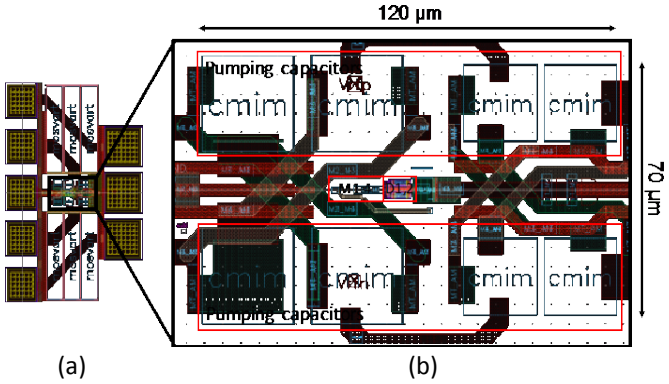

Fig. 7. (a) Layout of the proposed rectifier and (b) an enlarged view of the active area

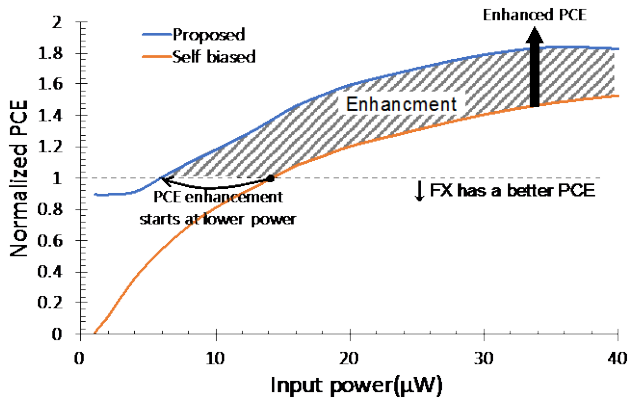

Fig. 8. Post-layout simulation of the PCE normalized to the FX architecture

IV. CONCLUSION

This work demonstrated an enhanced performance for a self-biased RF-to-DC converter that selectively controls the converter's conduction to minimize the leakage current without degrading the performance of the rectifier. The sensitivity of proposed design is -18 dBm and the peak power conversion efficiency is 67% when operating at 433MHz with a 100 kΩ load. Compared to the conventional FX architecture, the proposed design offers a 324% wider dynamic range and 261% better sensitivity.

REFERENCES

[1] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 3011-3018, 2009.

[2] X. Li, C.-Y. Tsui, and W.-H. Ki, "Power management analysis of inductively-powered implants with 1X/2X reconfigurable rectifier," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, pp. 617-624, 2015.

[3] M. Arsalan, M. H. Ouda, L. Marnat, A. Shamim, and K. N. Salama, "Implantable Intraocular Pressure Monitoring systems: Design considerations," in *2013 IEEE MTT-S International Microwave Workshop Series on RF and Wireless Technologies for Biomedical and Healthcare Applications (IMWS-BIO)*, 2013, pp. 1-3.

[4] T. C. Chang, M. L. Wang, J. Charthad, M. J. Weber, and A. Arbabian, "27.7 A 30.5 mm 3 fully packaged implantable device with duplex ultrasonic data and power links achieving 95kb/s with< 10− 4 BER at 8.5 cm depth," in *Solid-State Circuits Conference (ISSCC), 2017 IEEE International*, 2017, pp. 460-461.

[5] M. H. Ouda, M. Arsalan, L. Marnat, A. Shamim, and K. N. Salama, "5.2-GHz RF Power Harvester in 0.18-/spl mu/m CMOS for Implantable Intraocular Pressure Monitoring," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, pp. 2177-2184, 2013.

[6] M. Ouda, W. Khalil, and K. Salama, "Self-Biased Differential Rectifier with Enhanced Dynamic Range for Wireless Powering," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2016.

[7] S. Dwari, R. Dayal, L. Parsa, and K. N. Salama, "Efficient direct ac-to-dc converters for vibration-based low voltage energy harvesting," in *2008 34th Annual Conference of IEEE Industrial Electronics*, 2008, pp. 2320-2325.

[8] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of solid-state circuits*, vol. 11, pp. 374-378, 1976.

[9] M. H. Ouda, W. Khalil, and K. N. Salama, "Wide-Range Adaptive RF-to-DC Power Converter for UHF RFIDs," *IEEE Microwave and Wireless Components Letters*, vol. 26, pp. 634-636, 2016.

[10] K. Gharehbaghi, Ö. Zorlu, F. Koçer, and H. Külah, "Auto-calibrating threshold compensation technique for RF energy harvesters," in *Radio*

Frequency Integrated Circuits Symposium (RFIC), 2015 IEEE, 2015, pp. 179-182.
[11] S. S. Chouhan and K. Halonen, "A novel cascading scheme to improve the performance of voltage multiplier circuits," *Analog Integrated Circuits and Signal Processing*, vol. 84, pp. 373-381, 2015.