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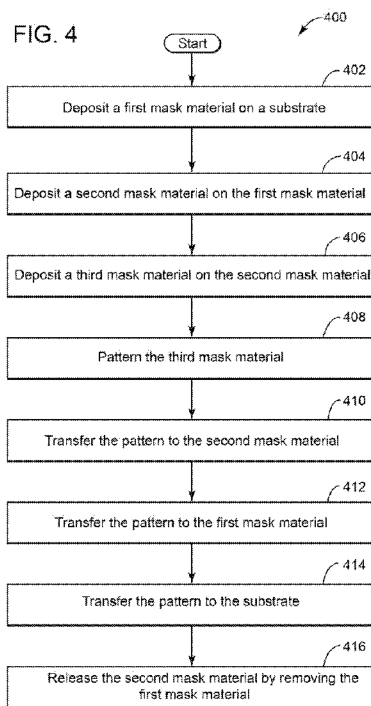
[Continued on next page]

(54) Title: HYBRID MASK FOR DEEP ETCHING



(57) Abstract: Deep reactive ion etching is essential for creating high aspect ratio micro-structures for microelectromechanical systems, sensors and actuators, and emerging flexible electronics. A novel hybrid dual soft/hard mask bilayer may be deposited during semiconductor manufacturing for deep reactive etches. Such a manufacturing process may include depositing a first mask material on a substrate; depositing a second mask material on the first mask material; depositing a third mask material on the second mask material; patterning the third mask material with a pattern corresponding to one or more trenches for transfer to the substrate; transferring the pattern from the third mask material to the second mask material; transferring the pattern from the second mask material to the first mask material; and/or transferring the pattern from the first mask material to the substrate.

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HYBRID MASK FOR DEEP ETCHING

CROSS-REFERENCE TO RELATED PATENT APPLICATIONS

[0001] None.

FIELD OF THE DISCLOSURE

[0002] The instant disclosure relates to semiconductor manufacturing. More specifically, portions of this disclosure relate to use a hybrid mask layer to allow deep etching through layers during a semiconductor manufacturing process.

BACKGROUND

[0003] Micromachining fabrication techniques are used in, for example, manufacturing microelectromechanical systems (MEMS), dynamic random access memory (DRAM) capacitors, through silicon vias (TSVs) for 3D packaging, and novel structures for the emerging Internet of Everything (IoE) free-form electronics. Conventional micromachining techniques include surface micromachining for structures that are a few microns deep and bulk micromachining for deeper structures. Bulk micromachining techniques have been used for making deep structures with high aspect ratio, fine features, and smooth sidewalls.

[0004] One bulk micromachining technique uses a hard mask material to withstand sustained deep reactive ion etching (DRIE) of patterns in a substrate. The hard mask material could be a metal, due to their inertness, or thin oxide layers. FIGURE 1 is a cross-section showing conventional deep etching with a metal hard mask. A hard mask layer 104 is deposited on a substrate 102 and patterned. The pattern in the hard mask layer 104 is then

transferred into the substrate 102. The obtainable depth of the pattern into the substrate is, in part, dependent upon the characteristics of the hard mask layer 104.

[0005] Another bulk micromachining technique involves the use of a soft mask layer. FIGURE 2 is a cross-section showing conventional deep etching with a soft hard mask. A soft mask layer 204, such as a photoresist layer or one or more other organic materials or non-metallic materials, is deposited on the substrate 102 and patterned. The pattern of the soft mask layer 204 is then transferred into the substrate 102. Photoresist (PR) and other soft materials are generally not suitable masks for DRIE processes. One such soft mask layer 204 may include a bilayer of oxide and photoresist and used for 300 μm deep etches. For tens of microns deep etches, photoresist masks may be sufficient. However, deeper trenches, such as for stretchable electronics where etching goes through the entire thickness of a silicon wafer, requires a hard mask of, for example, a Titanium/Gold bilayer.

[0006] The use of hard masks in deep etches (e.g., 100's of microns) imposes some limitations, especially for the semiconductor industry. The first challenge is the choice of the hard mask material. The DRIE time is affected, in part, by the depth of the trenches and the lateral dimensions due to the micro loading effect. The micro loading effect causes etching rate dependence such that narrower trenches would need more time to reach desired depth than wider features. This is explained by the effect of feature dimensions on trench conductance. The feature conductance is a measure of how easily reaction by-products can be vented and reactant gases can be supplied for more etching. As the trench depth (and aspect ratio) increases, the collisions between the leaving and entering gases increase, resulting in a dropping of the etch rate. Micro-loading results due to drop in feature conductance and narrower features suffer more because of the relative difficulty inherent in a smaller outlet/inlet trench.

[0007] The hard mask needs to be selective to the extremely long DRIE process, such that the mask is not etched during the process and at the same time the hard mask needs to be easily removed after the deep etch is performed. For instance, nickel is one conventional hard

mask that supports deep etching, but nickel is difficult to remove using dry etching techniques. Further, nickel, and other metals, can bond with other materials used during the semiconductor manufacturing process and alter their chemistry. For example, nickel forms NiSi with silicon substrates when exposed to high temperatures. Alternatively, gold can be used as a hard mask, but gold does not adhere well to silicon and requires an underlying titanium layer for adhesion. Titanium readily oxidizes in air and is also hard to remove using dry etching. Alternatively, aluminum can be easily etched using metal RIE in halide gases, but aluminum forms alloys with silicon at the interface. One alternative to dry etching is wet etching. But, wet etching involves immersing the whole wafer causing contamination and selectivity issues that would not be suitable for complementary metal-oxide-semiconductor (CMOS) process flows, especially at an advanced stage after the devices are fabricated.

[0008] Another issue with the use of hard masks is the deposition method, which is sputtering in most cases. The metal/silicon interface is degraded due to ion bombardment during the deposition or diffusion (if alternative deposition methods, such as atomic layer deposition, are used at elevated temperature). Finally, even dry etching of a hard mask involves plasma and DC power that can detrimentally affect the surface roughness of the silicon or underlying material interface, which is also undesirable for MEMS manufacturing. Thus, conventional manufacturing techniques for deep etching present many challenges when using either hard masks or soft masks.

SUMMARY

[0009] A hybrid dual soft/hard mask layer may be used to obtain some of the benefits of soft mask layers and some of the benefits of hard mask layers, while overcoming some of the challenges for deep etching of structures, including those of tens or hundreds of microns thick. The hybrid mask layer may include a hard mask layer above a soft mask layer. The hard mask layer may provide a desirable etch selectivity, such that deep structures may be manufactured using a relatively thin hard mask layer to create high aspect ratio structure. The soft mask layer under the hard mask layer may be used as a buffer to prevent undesirable chemical reactions between the hard mask layer and the underlying semiconductor structure. The soft mask layer may also be used as a sacrificial layer to allow easy removal of the hard mask layer by dissolving the soft mask layer to release the hard mask layer.

[0010] The processes involving the hybrid mask layer is generic and various sacrificial layers (such as amorphous Si, poly Si, dielectrics, polymers, etc.) and hard masks (Ni, dielectrics, Cu, Au, Pt, etc.) can be used. The disclosed processes have little or no effect on the surface of the material under the hybrid mask, prevents diffusion and alloy formation between hard mask and underlying layers, and/or avoids the abrasive etching of the hard mask after DRIE.

[0011] According to one embodiment, a manufacturing process may include depositing a first mask material on a substrate; depositing a second mask material on the first mask material; depositing a third mask material on the second mask material; patterning the third mask material with a pattern corresponding to one or more trenches for transfer to the substrate; transferring the pattern from the third mask material to the second mask material; transferring the pattern from the second mask material to the first mask material; and/or transferring the pattern from the first mask material to the substrate.

[0012] The foregoing has outlined rather broadly certain features and technical advantages of embodiments of the present invention in order that the detailed description that

follows may be better understood. Additional features and advantages will be described hereinafter that form the subject of the claims of the invention. It should be appreciated by those having ordinary skill in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same or similar purposes. It should also be realized by those having ordinary skill in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims. Additional features will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended to limit the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] For a more complete understanding of the disclosed system and methods, reference is now made to the following descriptions taken in conjunction with the accompanying drawings.

[0014] FIGURE 1 is a cross-section showing conventional deep etching with a metal hard mask.

[0015] FIGURE 2 is a cross-section showing conventional deep etching with a soft hard mask.

[0016] FIGURES 3A-3F are cross-sections showing a method of deep etching using a hybrid hard/soft mask according to one embodiment of the disclosure.

[0017] FIGURE 4 is a flow chart showing a method of deep etching features in one or more layers of a semiconductor structure using a hybrid hard/soft mask according to one embodiment of the disclosure.

[0018] FIGURES 5A-5H are illustrations showing a method of deep etching using a hybrid hard/soft mask with a metal and a negative-tone photoresist according to one embodiment of the disclosure.

[0019] FIGURE 6 is a flow chart showing a method of deep etching using a hybrid hard/soft mask with a metal and a negative-tone photoresist according to one embodiment of the disclosure.

[0020] FIGURE 7 is a flow chart showing a method of deep etching using a hybrid hard/soft mask according to another embodiment of the disclosure in which the metal is deposited as a pattern.

[0021] FIGURE 8 is a cross-section showing a through silicon via (TSV) that may be manufacturing using deep etching provided by a hybrid hard/soft mask according to one embodiment of the disclosure.

[0022] FIGURES 9A-9D are illustrations showing a method of encapsulating electronics using deep etching provided by a hybrid hard/soft mask according to one embodiment of the disclosure.

[0023] FIGURE 10 is a flow chart showing a method of preparing electronic device dies using deep etching provided by a hybrid hard/soft mask according to one embodiment of the disclosure.

DETAILED DESCRIPTION

[0024] FIGURES 3A-3F are cross-sections showing a method of deep etching using a hybrid hard/soft mask according to one embodiment of the disclosure. FIGURE 3A shows a hybrid mask after deposition of layers on a semiconductor structure, such as a semiconductor substrate. A first soft mask layer 304 may be deposited on substrate 302. A hard mask layer 306 may be deposited on the first soft mask layer 304, and a second soft mask layer 306 may be deposited on the hard mask layer 306. The soft mask layer 304 and the hard mask layer 306 may form a hybrid hard/soft bilayer mask.

[0025] FIGURE 3B shows the structure of FIGURE 3A after patterning of the second soft mask layer 308. The second soft mask layer 308 may be used to pattern a desired structure into the hard mask layer 306. Openings 310 may be patterned in the second soft mask layer 308, in which the openings 310 correspond to trenches or other structures to replicate in lower layers such as the substrate 302. The pattern 310 may include one or more trenches, such as those used to form through silicon vias (TSVs) or encapsulation of electronics formed on the substrate 302.

[0026] The pattern 310 may be transferred to lower layer hard mask layer 306 as shown in FIGURE 3C and again transferred to lower layer soft mask layer 304 as shown in FIGURE 3D. The pattern 310 may then be transferred to the substrate 302 as shown in FIGURE 3E. The transfer may etch through some or all of the semiconductor structure below the first soft mask layer 304. Then, the hybrid mask may be stripped from the substrate 302 as shown in FIGURE 3F. The hybrid mask may be removed by dissolving the soft mask layer 304, such that the hard mask layer 306 and any remaining second soft mask layer 308, is released from the substrate 302. The soft mask layer 304 is generally easier to remove than the hard mask layer 306 and leaves the surface of substrate 302 with less change. However, the hard mask layer 306 provides better functionality as a mask layer for deep etching through semiconductor structures, such as substrate 302. Thus, by combining the soft mask layer 304 and hard mask layer 306, a

hybrid mask provides many of the benefits of both the soft mask layer 304 and the hard mask layer 306, while reducing the disadvantages of each.

[0027] One semiconductor manufacturing process using a hybrid mask for deep etching is described with reference to FIGURE 4. FIGURE 4 is a flow chart showing a method of deep etching features in one or more layers of a semiconductor structure using a hybrid hard/soft mask according to one embodiment of the disclosure. A method 400 begins at block 402 with depositing a first mask material on a substrate. Then, at block 404, a second mask material is deposited on the first mask material. Next, at block 406, a third mask material is deposited on the second mask material. The mask materials of 402, 404, and 406 may be the soft mask layer 304, the hard mask layer 306, and the soft mask layer 308 shown in FIGURES 3A-3F.

[0028] With the hybrid mask layers deposited, the layers may then be patterned and the pattern transferred to semiconductor structures below the hybrid mask. At block 408, the third mask material is patterned, and that pattern transferred to the second mask material at block 410 and then to the first mask material at block 412. The patterning at block 408 may include exposing the third mask material through a photomask and developing the third mask material to form a physical pattern corresponding to the pattern on the photomask. The transfer of blocks 410 and 412 may include etching through the first and second mask material, such as by sputter etching or reactive ion etching (RIE). The pattern may be transferred to the hybrid mask layers, including the first mask material and the second mask material, by using the third mask material as a mask for the etching process.

[0029] After the pattern is transferred to the hybrid mask, semiconductor structures below the hybrid mask may be etched. For example, at block 414, the pattern of the hybrid mask may be transferred to the substrate by deep etching through the substrate using the hybrid mask as an etch mask. The deep etch may create openings the substrate that extend the entire length of the substrate and emerge on the other side to allow interconnecting of electronics

on both sides of the substrate. The hard mask material of the hybrid mask allows the deep etching to form high aspect ratio structures in the semiconductor layers. The soft mask material of the hybrid mask reduces or prevents contamination of the surface of the semiconductor layers by the hard mask material. After transferring the pattern to the semiconductor layers, the second mask material may be released by removing the first mask material. For example, the soft mask material may be dissolved in a solvent or developer and any remaining structures above the soft mask material are then released from the semiconductor structure.

[0030] One application of the semiconductor manufacturing process described with reference to FIGURES 3-4 is described with reference to FIGURES 5-6. The process of FIGURES 5-6 will be described involving specific materials selections and etching chemistries. However, embodiments of the manufacturing process described with reference to FIGURES 3-4 may involve many other materials and processes. FIGURES 5A-5H are illustrations showing a method of deep etching using a hybrid hard/soft mask with a metal and a negative-tone photoresist according to one embodiment of the disclosure. FIGURE 6 is a flow chart showing a method of deep etching using a hybrid hard/soft mask with a metal and a negative-tone photoresist according to one embodiment of the disclosure.

[0031] Referring to FIGURE 6, a method 600 begins with forming the hybrid mask on a semiconductor structure. Initially, at block 602, a negative-tone photoresist is deposited as a first mask material on a semiconductor substrate, such as a silicon substrate. FIGURE 5A shows a silicon wafer 302, and FIGURE 5B shows the silicon wafer 302 after spinning on an AZ-5214 negative-tone photoresist first mask layer 304. At block 604, the negative-tone photoresist is flood exposed under an appropriate light source with no photomask, resulting in exposure of the entire layer 304. Next, at block 606, an aluminum metal layer is deposited on the negative-tone photoresist. FIGURE 5C shows the aluminum layer second mask layer 306 deposited on the first mask layer 302. Then at block 608, a positive-tone photoresist is deposited as the third mask layer on the second mask layer. FIGURE 5D shows the ECI-3027 positive-tone photoresist third mask layer 308 on the second mask layer 306. The third mask

layer may serve as a mask for patterning the hybrid mask including the negative-tone photoresist layer and the aluminum layer.

[0032] After the hybrid mask is formed, a pattern may be formed in the hybrid mask and the hybrid mask used to transfer the pattern to the semiconductor structure. At block 610, the positive-tone photoresist may be patterned by exposing the photoresist to an appropriate light source through a photomask and developing the photoresist. FIGURE 5D shows a pattern feature 310 formed in the photoresist third mask layer 308. Then, at block 612, the pattern may be transferred to the aluminum layer using the positive-tone photoresist as a mask. FIGURE 5E shows the pattern 310 transferred into the aluminum second mask layer 306. Next, at block 614, the pattern is transferred to the negative-tone photoresist using the aluminum mask material as a mask. FIGURE 5F shows the pattern 310 transferred to the negative-tone photoresist first mask material 304. Optionally, the positive-tone photoresist third mask material 308 may be removed after the pattern is transferred from the third mask material to the hybrid mask. The positive-tone photoresist may be removed, for example, by exposing the semiconductor structure to an oxygen plasma.

[0033] Finally, the etching of the substrate 302 or other semiconductor structures may be performed using the hybrid mask as a mask for deep etching. At block 614, the pattern is transferred from the hybrid mask to the substrate. FIGURE 5G shows the pattern 310 transferred to the substrate 302. Next, at block 616, the negative-tone photoresist may be dissolved in solvent to remove the aluminum layer and the negative-tone photoresist. For example, the semiconductor structure may be placed in an ultrasonic acetone batch. FIGURE 5H shows the pattern 310 in the substrate 302 after the hybrid mask is removed.

[0034] As a proof of concept, the hybrid dual-layer mask was used to etch through the whole thickness of a Si (100) 4” wafer having a thickness of approximately 500 μm. First, negative-tone PR AZ 5214E with image reversal capability is spun at 3000 rpm for an approximately 1.6 μm thick layer. Pyrolysis bake is then carried out at 100°C for 60 seconds

followed by flood exposure and an image reversal bake at 120°C for 2 minutes. This makes the complete PR layer insoluble in AZ 726 MIF developer. Next, a thin 200 nm Aluminum layer is sputtered at room temperature followed by positive-tone PR AZ 3027 spun at 3000 rpm to deposit an approximately 4 μm thick layer that is patterned using a 200 mJ/cm^2 constant dose and developed in AZ 726 MIF developer for 60 seconds. Then, the Aluminum layer is patterned using the PR mask and metal RIE using a 1500 Watt inductively coupled plasma (ICP), 50 W RF, 20 mTorr, 40 sccm Cl_2 and 10 sccm BCl_3 at 80°C. Then, the negative tone PR is etched in O_2 plasma RIE followed by DRIE of Silicon using SF_6 and C_4F_8. Finally, the hybrid dual PR/Al mask is removed by immersing in Acetone bath.

[0035] A similar approach for patterning a semiconductor substrate has been performed using photoresist (PR)-only mask. The maximum depth achieved before the PR was totally etched during DRIE was 100 μm. On the other hand, the hybrid PR/Al mask persisted during etching of the whole silicon substrate (~525 μm).

[0036] To assess the effect of the new process on the etched features and the underlying silicon substrate surface, profiler measurements for surface roughness and scanning electron microscopy (SEM) imaging for feature size measurements, were performed. The results show that the surface of the substrate using only PR and etched during the DRIE process has the highest variations in height and highest surface roughness. This is a challenge when using PR, especially because the process does not have real time feedback to know when the PR is about to be etched through and what is the maximum safe depth using specific PR types. On the other hand, using an Al-only hard mask and wet etching in Gravure or a PR/Al hybrid mask and removal in acetone showed similar results to pristine silicon surface. Gravure is strongly acidic and not recommended for wafers containing fabricated devices and structures. Thus, although the Al-only hard mask may produce results similar to the hybrid mask on a test wafer, the Al-only hard mask process is inappropriate for use on substrates containing electronic circuitry or precursor layers or structures for electronic circuitry.

[0037] The demonstrated deep etching using a hybrid mask enables sub-millimeter etching structures, variations of regular etching enabled by choice of any hard mask without the requirement for later removal using strong chemicals or abrasive etching, highly-customized dicing patterns (parallel process and can have customized curves and twists), supporting high-performance bulk mono-crystalline silicon modules on polymers for flexible systems, and is a step forward towards novel flexible packaging of high performance electronics.

[0038] The semiconductor manufacturing process with a hybrid mask described with reference to FIGURES 3-6 may be varied while retaining the benefits of the hybrid mask. Another manufacturing processing using the hybrid mask is shown in FIGURE 7. FIGURE 7 is a flow chart showing a method of deep etching using a hybrid hard/soft mask according to another embodiment of the disclosure in which the metal is deposited as a pattern. The process of FIGURE 7 involves the deposition of a patterned hard mask layer of the hybrid mask. Thus, a third mask layer used for patterning the second, hard mask material may be omitted. A method 700 begins at block 402 with depositing a first material on a substrate. Then, at block 704, a second mask material may be deposited as a patterned layer on the first mask material. The second mask material may be a hard mask layer of a hybrid mask, and the first mask material may be a soft mask layer of the hybrid mask. The patterned deposition may be performed, for example, by evaporating a metal, such as aluminum, through a stencil mask to form a patterned metal layer on the first mask material. The remaining steps of the processing method 700 may continue similar to those described with reference to FIGURE 4. For example, the pattern of the second mask material may be transferred to the first mask material at block 412, transferred to the substrate at block 414, and then the second mask material released by removing the first mask material at block 416.

[0039] The hybrid mask and semiconductor manufacturing processes using the hybrid mask, such as those described above with reference to FIGURES 3-7 may be used to form through silicon vias (TSVs). TSVs may extend the entire thickness of a silicon substrate. The TSV may be filled with one or more conductors to allow transfer or power or data from one side

of a substrate to another side of the substrate. FIGURE 8 is a cross-section showing a through silicon via (TSV) that may be manufacturing using deep etching provided by a hybrid hard/soft mask according to one embodiment of the disclosure. A pattern 310 created in the substrate 302 using the hybrid mask may extend from one side of the substrate 302 to another side of the substrate 302 to form a TSV. A conductor 802 may be deposited in the TSV to provide conduction from one side of the substrate 302 to another side of the substrate 302. Electronics (not shown) on one side of the substrate 302 may then be coupled to the conductor 802 and electronics on the other side of the substrate 302 coupled to the conductor 802, and power or data signals passed through the conductor 802. The TSV may also include multiple conductors 802, such as in a concentric ring configuration, to allow multiple power lines or multiple-bit data signals to be passed from one side of the substrate 302 to the other side of the substrate 302.

[0040] Another application of the hybrid mask in semiconductor manufacturing processes uses the hybrid mask for the manufacturing and encapsulation of electronic circuits. One such method will be described with reference to FIGURES 9-10. FIGURES 9A-9D are illustrations showing a method of encapsulating electronics using deep etching provided by a hybrid hard/soft mask according to one embodiment of the disclosure. FIGURE 10 is a flow chart showing a method of preparing electronic device dies using deep etching provided by a hybrid hard/soft mask according to one embodiment of the disclosure. A method 1000 of FIGURE 10 begins at block 1002 with forming electronic circuitry on a substrate. FIGURE 9A shows electronic circuitry formed on a substrate having a silicon layer 902 and a polymer layer 904. Then, at block 1004, a hybrid mask may be formed on the substrate and electronic circuitry. The hybrid mask may be patterned such that the hybrid mask remains over the electronic circuitry. Thus, during later processing, the substrate materials around the electronics materials may be etched back around the electronic circuitry. Block 1004 may include, for example, blocks 402-410 of FIGURE 4. FIGURE 9B shows the hybrid mask 905 patterned on the electronic circuitry. Next, at block 1006, the pattern in the hybrid mask is transferred to form a recessed area around the electronic circuitry formed at block 1002. FIGURE 9C shows a portion of the substrate 902 recessed around the electronic circuitry. Then, at block 1007, the

hybrid mask may be removed, and, at block 1008, bonding pads may be deposited in the recessed area and the bonding pads coupled to the electronic circuitry. FIGURE 9C shows bonding pads 906 coupled through wiring 908 to electronic circuitry. Next, at block 1010, the electronic circuity may be encapsulated. FIGURE 9D shows encapsulation 910 deposited around the electronic circuitry and parts or all of the wiring 908 and the bonding pads 906.

[0041] Embodiments described above illustrate a deep etching technique using a hybrid dual soft/hard mask layer for harnessing the benefits of easy removal, preserving the interface of underlying substrate, and persisting through long duration etches. Negative-PR/Al metal layer hybrid masks have been used to demonstrate the capabilities of the technique, and properties of the etched features are at least as good as those obtained using only a hard and present none of the issues involved with using only a hard mask. These processing techniques can be adapted towards realization of future flexible and stretchable electronics and flexible packaging techniques. Further, the deep etching ability described above may be employed in bulk micromachining to fabricate micro-motors, electrostatic resonators, optical filters, micro-lenses, thermal actuators, MEMS switches, capacitive sensors and actuators, and flexible and stretchable electronic devices.

[0042] The schematic flow chart diagrams of FIGURE 3, FIGURE 4, FIGURE 5, FIGURE 6, FIGURE 7, and FIGURE 10 are generally set forth as a logical flow chart diagrams. As such, the depicted order and labeled steps are indicative of aspects of the disclosed methods. Other steps and methods may be conceived that are equivalent in function, logic, or effect to one or more steps, or portions thereof, of the illustrated methods. Additionally, the format and symbols employed are provided to explain the logical steps of the methods and are understood not to limit the scope of the methods. Although various arrow types and line types may be employed in the flow chart diagram, they are understood not to limit the scope of the corresponding methods. Indeed, some arrows or other connectors may be used to indicate only the logical flow of the methods. For instance, an arrow may indicate a waiting or monitoring period of unspecified duration between enumerated steps of the depicted methods. Additionally,

the order in which a particular method occurs may or may not strictly adhere to the order of the corresponding steps shown.

[0043] Although the present disclosure and certain representative advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS

What is claimed is:

1. A method, comprising:

   depositing a first mask material on a substrate;

   depositing a second mask material on the first mask material;

   depositing a third mask material on the second mask material;

   patterning the third mask material with a pattern corresponding to one or more trenches for transfer to the substrate;

   transferring the pattern from the third mask material to the second mask material;

   transferring the pattern from the second mask material to the first mask material; and

   transferring the pattern from the first mask material to the substrate.

2. The method of claim 1, further comprising removing the first mask material, the second mask material, and the third mask material by releasing the second mask material and the third mask material by dissolving the first mask material.

3. The method of claim 1, wherein the first mask material comprises a non-metallic material, the second mask material comprises a metallic material, and the third mask material comprises a non-metallic material.

4. The method of claim 3, wherein the first mask material comprises a negative tone photoresist and the third mask material comprises a positive tone photoresist.

5. The method of claim 1, wherein the step of transferring the pattern from the first mask material to the substrate comprises forming one or more through silicon vias (TSVs).

6. The method of claim 1, wherein the step of transferring the pattern from the first mask material to the substrate comprises etching an entire thickness of the substrate.

7. The method of claim 1, wherein the step of transferring the pattern from the first mask material to the substrate comprises etching one or more trenches around electronic components.

8. The method of claim 7, further comprising forming bonding pads in the one or more trenches around electronic components.

9. The method of claim 8, further comprising coupling the bonding pads to the electronic components; and encapsulating the electronic components.

10. The method of claim 9, wherein the steps of forming the bonding pads, coupling the bonding pads, and encapsulating the electronic components comprises forming a flexible electronics package.

FIG. 1
Prior Art

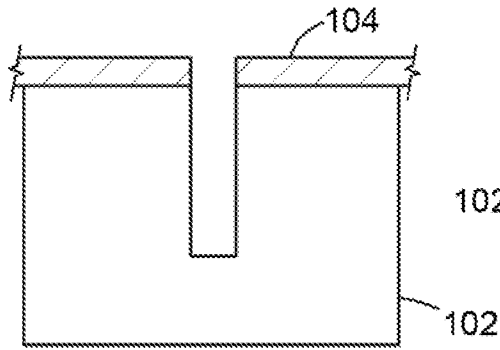


FIG. 2
Prior Art

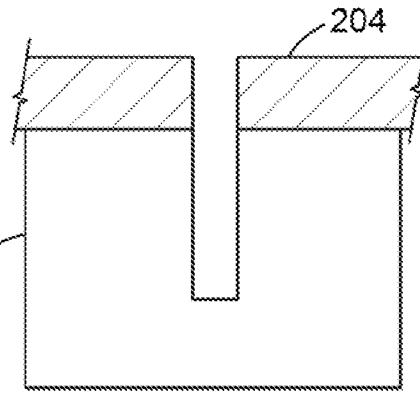


FIG.3A

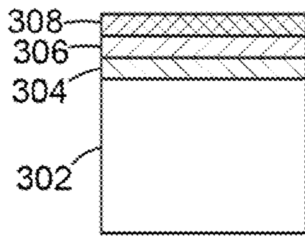


FIG.3B

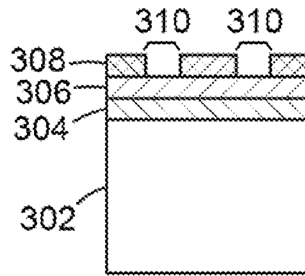


FIG.3C

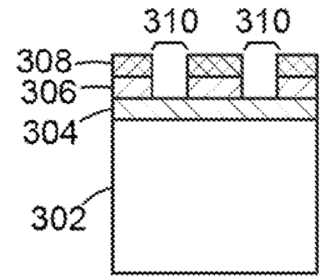


FIG.3D

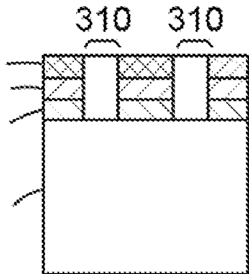


FIG.3E

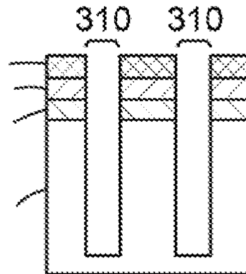
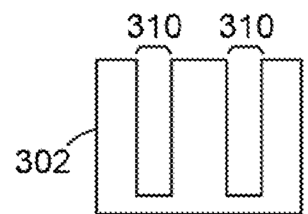


FIG.3F



308 (Top sacrificial)

306 (Hard Mask)

304 (Bottom sacrificial)

302 (Material to be Etched)

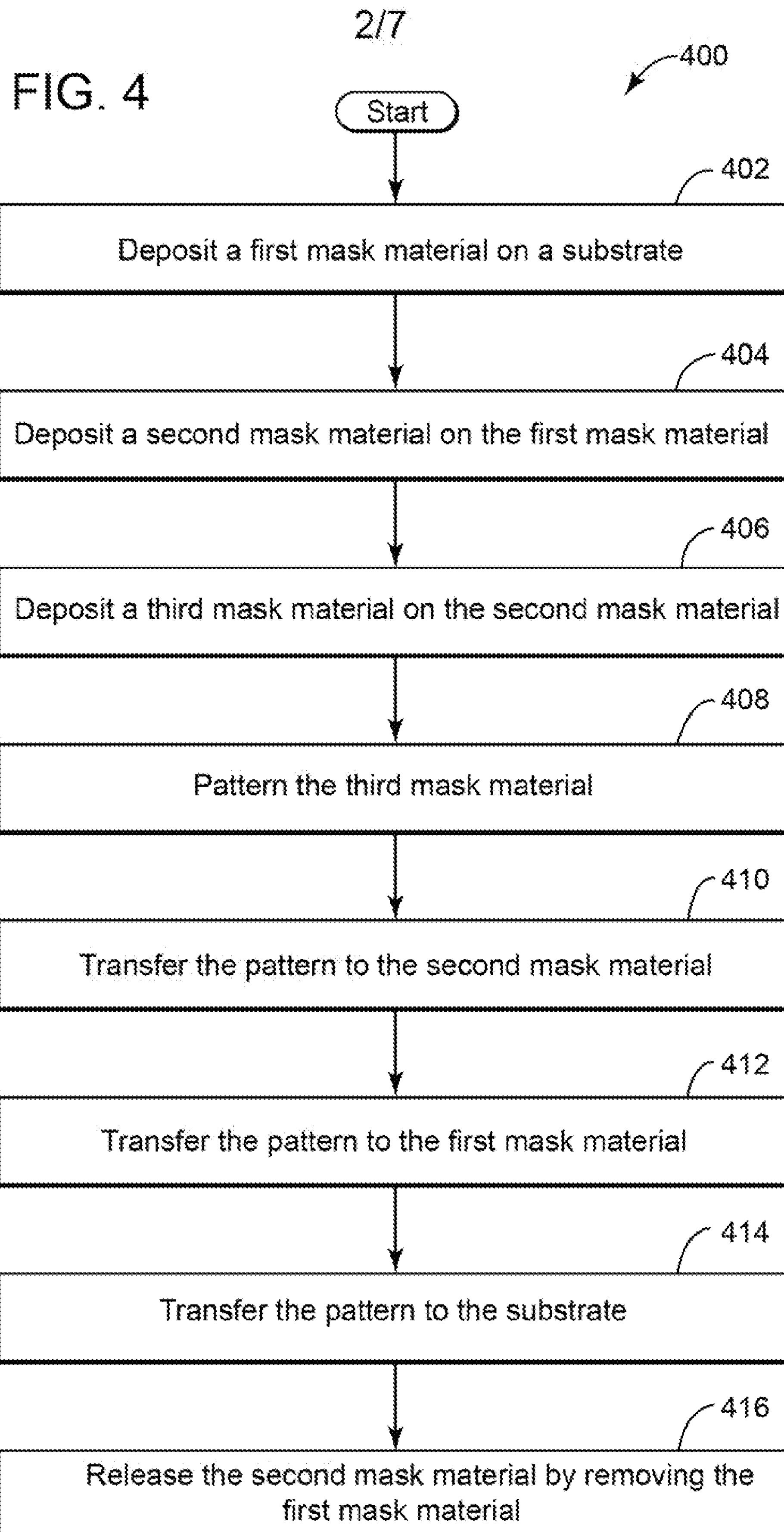


FIG. 4
400
Start
402
Deposit a first mask material on a substrate
404
Deposit a second mask material on the first mask material
406
Deposit a third mask material on the second mask material
408
Pattern the third mask material
410
Transfer the pattern to the second mask material
412
Transfer the pattern to the first mask material
414
Transfer the pattern to the substrate
416
Release the second mask material by removing the first mask material

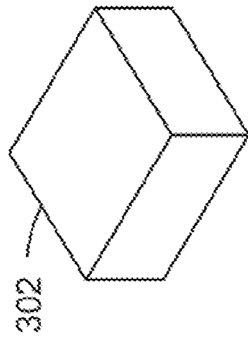


FIG. 5A

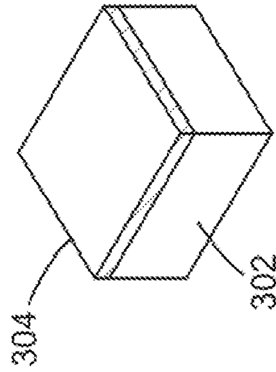


FIG. 5B

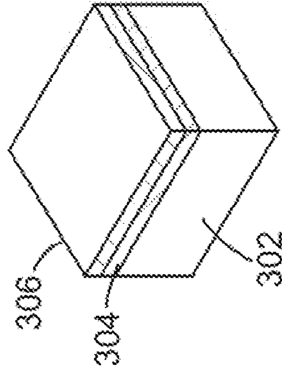


FIG. 5C

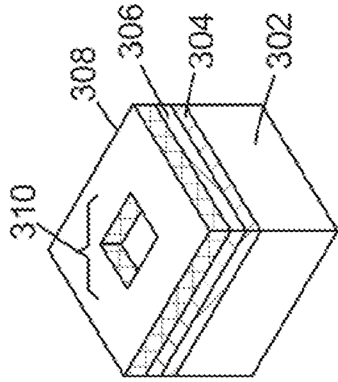


FIG. 5D

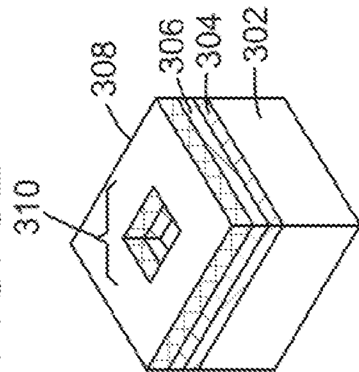


FIG. 5E

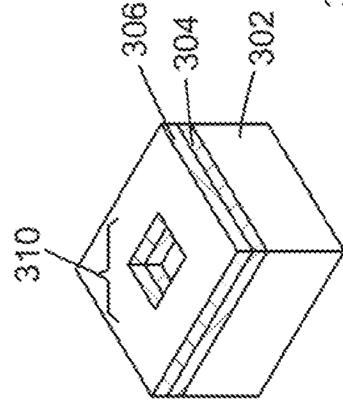


FIG. 5F

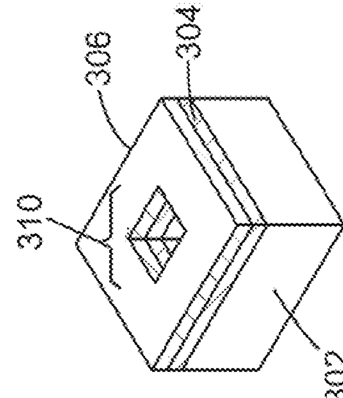


FIG. 5G

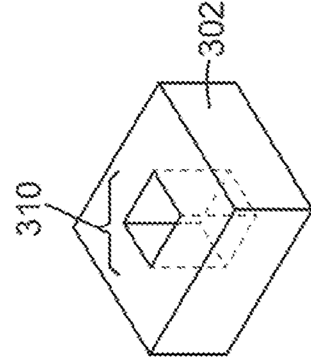


FIG. 5H

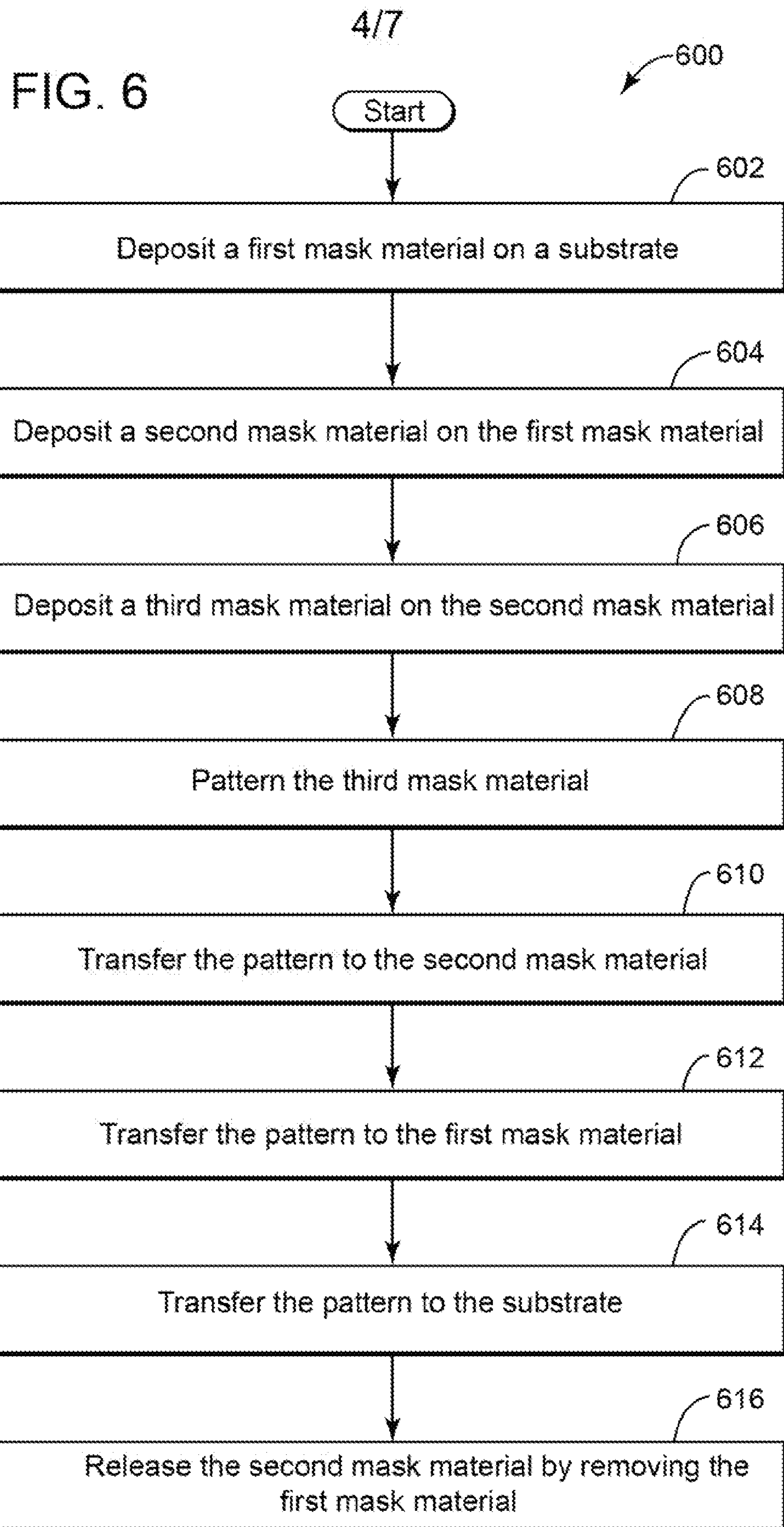


FIG. 6
600
Start
602
Deposit a first mask material on a substrate
604
Deposit a second mask material on the first mask material
606
Deposit a third mask material on the second mask material
608
Pattern the third mask material
610
Transfer the pattern to the second mask material
612
Transfer the pattern to the first mask material
614
Transfer the pattern to the substrate
616
Release the second mask material by removing the first mask material

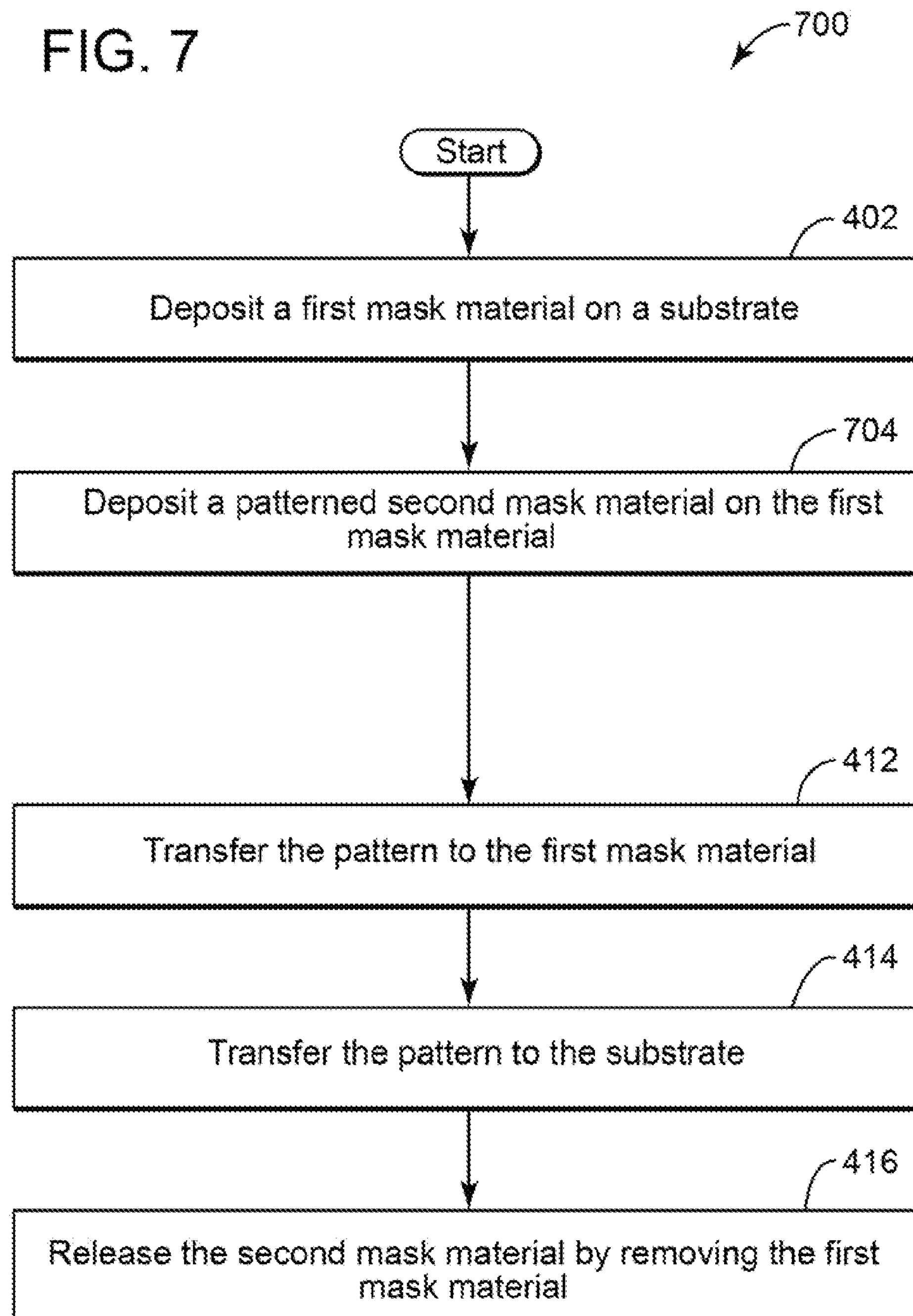


FIG. 7
700
Start
402
Deposit a first mask material on a substrate
704
Deposit a patterned second mask material on the first mask material
412
Transfer the pattern to the first mask material
414
Transfer the pattern to the substrate
416
Release the second mask material by removing the first mask material

FIG. 8

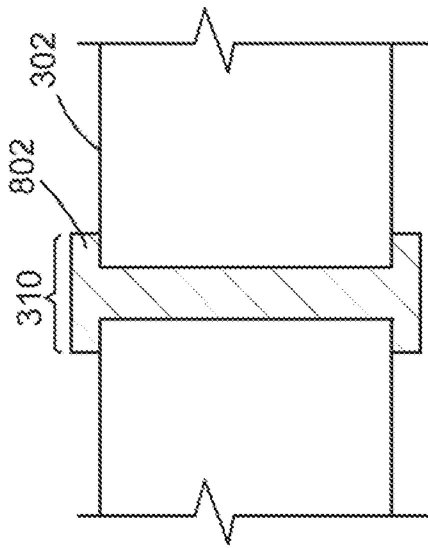


FIG. 9A

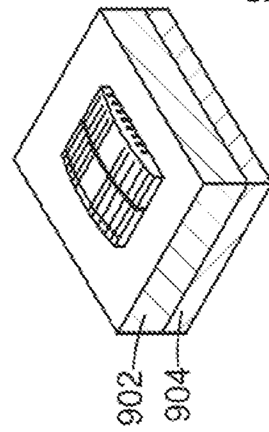


FIG. 9B

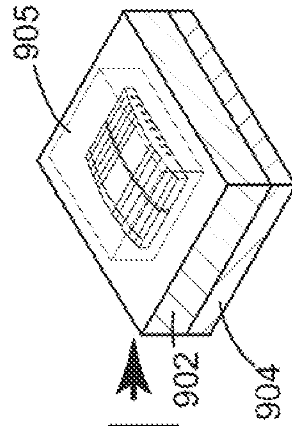


FIG. 9C

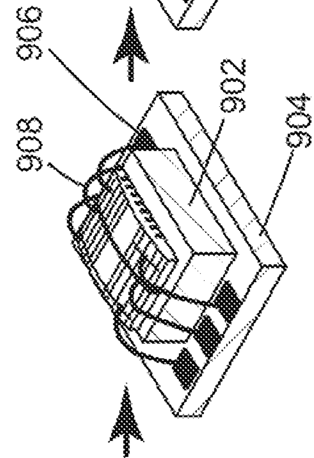
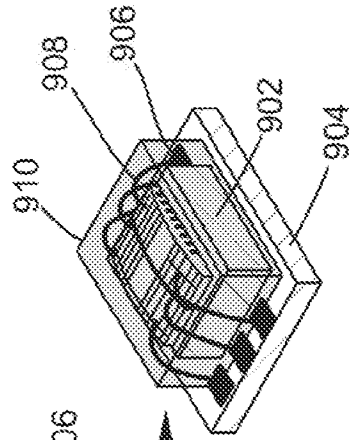


FIG. 9D



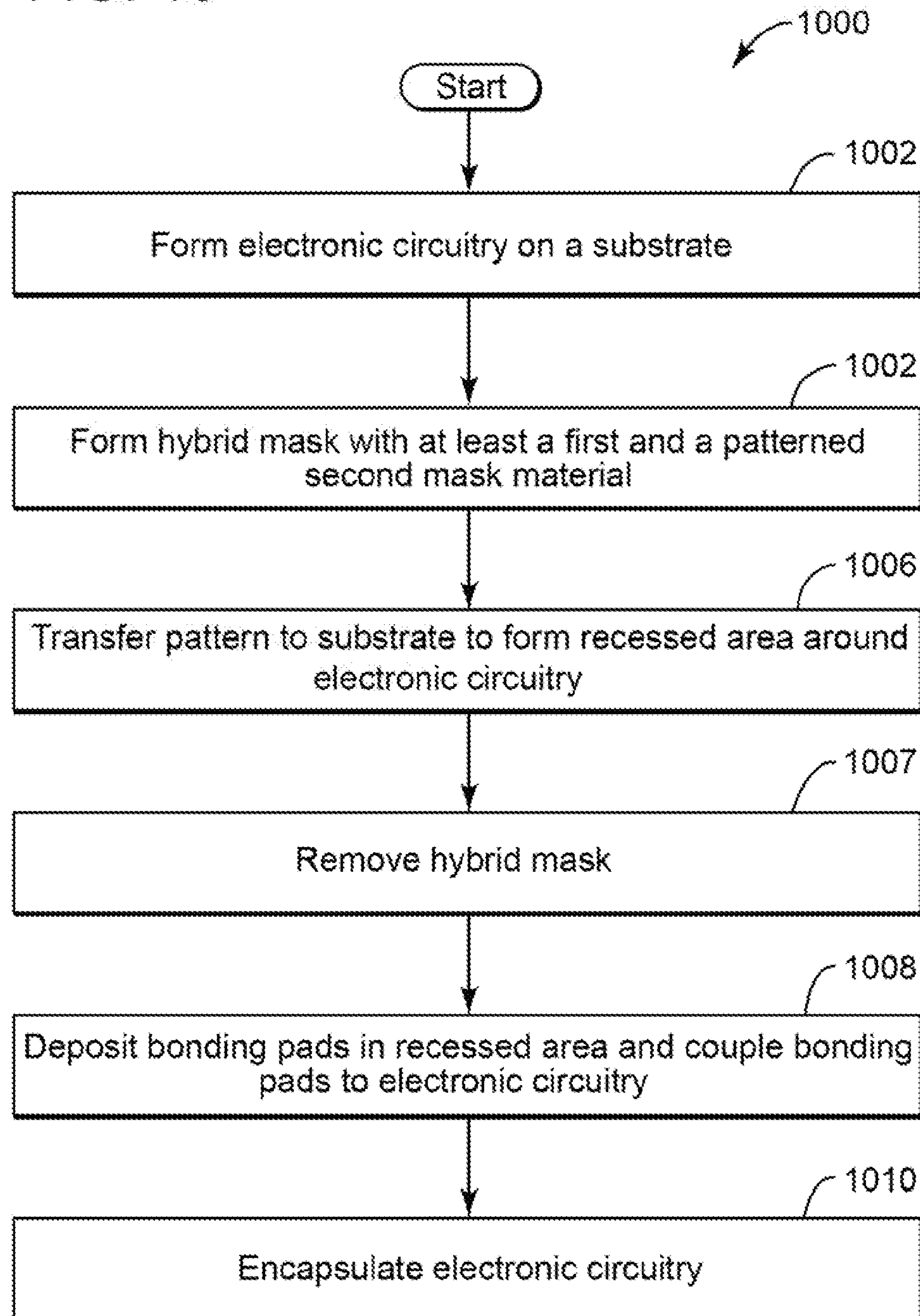


FIG. 10
1000
Start
1002
Form electronic circuitry on a substrate
1002
Form hybrid mask with at least a first and a patterned second mask material
1006
Transfer pattern to substrate to form recessed area around electronic circuitry
1007
Remove hybrid mask
1008
Deposit bonding pads in recessed area and couple bonding pads to electronic circuitry
1010
Encapsulate electronic circuitry

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2017/050417

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/308
ADD. H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2015/380251 A1 (GLODDE MARTIN [US] ET AL) 31 December 2015 (2015-12-31) paragraphs [0015] - [0021], [0047]; figures 4-6	1,3 4,7-10
X	EP 0 232 894 A2 (SELENIA IND ELETTRONICHE [IT]) 19 August 1987 (1987-08-19) page 3, last paragraph - page 5, paragraph 3; figure 2	1-3
X	US 2014/225233 A1 (HIRSCHLER JOACHIM [AT] ET AL) 14 August 2014 (2014-08-14) paragraph [0003]; figure 3	1,5,6
Y	WO 01/79933 A1 (OBDUCAT AB [SE]; HEIDARI BABAK [SE]) 25 October 2001 (2001-10-25) page 10, line 30 - page 11, line 23; figure 4	4

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
14 July 2017	21/07/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Gori, Patrice

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2017/050417

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012/115331 A1 (KOH CHA-WON [KR] ET AL) 10 May 2012 (2012-05-10) figure 3	7-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2017/050417

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