(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(10) International Publication Number
WO 2017/109734 A1

(43) International Publication Date
29 June 2017 (29.06.2017)

(51) International Patent Classification:
H01L 51/05 (2006.01) *H01L 51/10* (2006.01)

(21) International Application Number:
PCT/IB2016/057897

(22) International Filing Date:
21 December 2016 (21.12.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/270,682 22 December 2015 (22.12.2015) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

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(54) Title: ORGANIC TUNNEL FIELD EFFECT TRANSISTORS

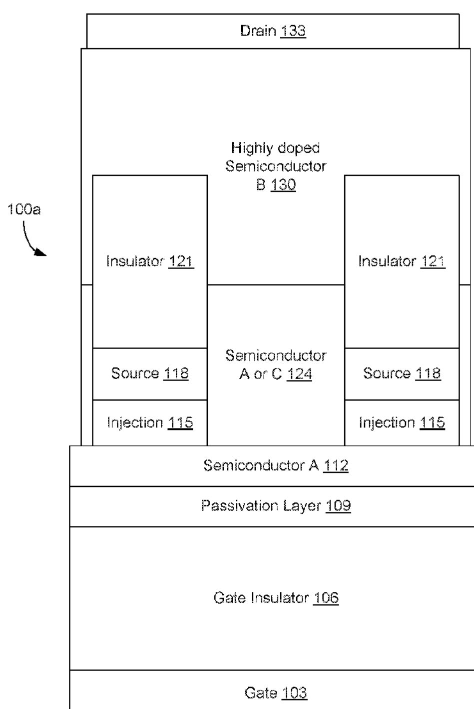

FIG. 2A

(57) Abstract: Various examples are provided for organic tunnel field effect transistors (OTFET), and methods thereof. In one example, an OTFET includes a first intrinsic layer (i-layer) of organic semiconductor material disposed over a gate insulating layer; source (or drain) contact stacks disposed on portions of the first i-layer; a second i-layer of organic semiconductor material disposed on the first i-layer surrounding the source (or drain) contact stacks; an n-doped organic semiconductor layer disposed on the second i-layer; and a drain (or source) contact layer disposed on the n-doped organic semiconductor layer. The source (or drain) contact stacks can include a p-doped injection layer, a source (or drain) contact layer, and a contact insulating layer. In another example, a method includes disposing a first i-layer over a gate insulating layer; forming source or drain contact stacks; and disposing a second i-layer, an n-doped organic semiconductor layer, and a drain or source contact.

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SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

— *with international search report (Art. 21(3))*

ORGANIC TUNNEL FIELD EFFECT TRANSISTORS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to, and the benefit of, co-pending U.S. provisional application entitled "Organic Tunnel Field Effect Transistors" having serial no. 62/270,682, filed December 22, 2015, which is hereby incorporated by reference in its entirety.

BACKGROUND

[0002] Field effect transistors are one of the most important devices of the modern microelectronics industry. Reliable doping of the semiconductor materials allows for precise tuning of the device properties (p-type vs. n-type), which can yield complementary metal-oxide-semiconductor (CMOS) technology – the basis of many digital circuits. Organic electronics offers an alternative class of low-cost and flexible electronics.

SUMMARY

[0003] Embodiments of the present disclosure are related to organic tunnel field effect transistors.

[0004] In one embodiment, among others, an organic tunnel field effect transistor comprises a first intrinsic layer (i-layer) of organic semiconductor material disposed over a gate insulating layer, where the first i-layer of organic semiconductor material is undoped; a plurality of source (or drain) contact stacks disposed on portions of the first i-layer of organic semiconductor material; a second i-layer of organic semiconductor material disposed on the first i-layer of organic semiconductor material surrounding the plurality of source (or drain) contact stacks, where a thickness of the second i-layer of organic semiconductor material is of the same thickness or greater than a combined thickness of the p-doped injection layer and the source (or drain) contact layer, and the second i-layer of P5 is undoped; an n-doped organic semiconductor layer disposed on the second i-layer of organic semiconductor

material surrounding and disposed on the plurality of source (or drain) contact stacks; and a drain (or source) contact layer disposed on the n-doped organic semiconductor layer. Each of the plurality of source (or drain) contact stacks can comprise a p-doped injection layer disposed on a corresponding portion of the first i-layer of organic semiconductor material; a source (or drain) contact layer disposed on the p-doped injection layer; and a source (or drain) contact insulating layer disposed on the source (or drain) contact layer.

[0005] In one or more aspects of these embodiments, each of the plurality of source (or drain) contact stacks can include a stack i-layer of organic semiconductor material disposed on the source (or drain) contact insulating layer. The stack i-layer of organic semiconductor material can be undoped and a thickness of the stack i-layer of organic semiconductor material can correspond to the thickness of the second i-layer of organic semiconductor material. The thickness of the second i-layer of organic semiconductor material and the stack i-layer of organic semiconductor material can be about 100 nm or more, or about 30 nm or more. In one or more aspects of these embodiments, the first i-layer of organic semiconductor material and the second i-layer of organic semiconductor material can comprise undoped pentacene (P5). The n-doped organic semiconductor layer can comprise n-doped pentacene (n-P5). The thickness of the n-doped organic semiconductor layer can be about 100 nm or more, or about 30 nm or more. In one or more aspects of these embodiments, the organic semiconductor material of the first i-layer can be different than the organic semiconductor material of the second i-layer.

[0006] In one or more aspects of these embodiments, the p-doped injection layer can comprise a p-doped P5 (p-P5) layer disposed on the corresponding portion of the first i-layer of organic semiconductor material. The p-P5 layer can comprise a blend of P5 and a p-dopant. The p-dopant is 2,2'-(perfluoronaphthalene-2,6-diylidene) dimalononitrile (F6-TCNNQ). The p-doped injection layer can comprise a pristine p-dopant layer disposed on the p-P5 layer. The pristine p-dopant layer can consist of the p-dopant. The p-P5 layer can have a thickness of about 10 nm and the pristine p-dopant layer can have a thickness of about 2 nm. In one or more aspects of these embodiments, the p-doped injection layer can

consist of pristine p-dopant disposed on the corresponding portion of the first i-layer of organic semiconductor material. The p-dopant can be 2,2'-(perfluoronaphthalene-2,6-diylidene) dimalononitrile (F6-TCNNQ). In one or more aspects of these embodiments, an n-doped organic semiconductor layer can extend beyond the source (or drain) contact insulating layer.

[0007] In another embodiment, a method comprises disposing a first intrinsic layer (i-layer) of organic semiconductor material over a gate insulating layer; forming a plurality of p-doped injection layer sections on corresponding portions of the first i-layer of organic semiconductor material; forming a plurality of source (or drain) contacts on corresponding ones of the plurality of p-doped injection layer sections; forming a plurality of source (or drain) contact insulation layer sections on corresponding ones of the plurality of source (or drain) contacts; disposing a second i-layer of organic semiconductor material on the first i-layer of organic semiconductor material surrounding the plurality of p-doped injection layer sections and the plurality of source (or drain) contacts; disposing an n-doped organic semiconductor layer on the second i-layer of organic semiconductor material, the n-doped organic semiconductor layer encapsulating portions of the plurality of source (or drain) contact insulation layer sections; and disposing a drain (or source) contact on the n-doped organic semiconductor layer.

[0008] In one or more aspects of these embodiments, the first i-layer of organic semiconductor material and the second i-layer of organic semiconductor material can comprise undoped pentacene (P5). The thickness of the second i-layer of organic semiconductor material can be about 100 nm or more, or 30 nm or more. The n-doped organic semiconductor layer can comprise n-doped pentacene (n-P5). The thickness of the n-doped organic semiconductor layer can be about 100 nm or more, or 30 nm or more. In one or more aspects of these embodiments, the organic semiconductor material of the first i-layer is different than the organic semiconductor material of the second i-layer.

[0009] In one or more aspects of these embodiments, forming the plurality of p-doped injection layer sections can comprise forming a plurality of p-doped P5 (p-P5) layer sections

on the corresponding portions of the first i-layer of organic semiconductor material, the p-P5 layer sections comprising a blend of P5 and a p-dopant; and forming a plurality of pristine p-dopant layer sections on corresponding ones of the p-P5 layer sections, the pristine p-dopant layer sections consisting of the p-dopant. The p-dopant can be 2,2'-(perfluoronaphthalene-2,6-diylidene) dimalononitrile (F6-TCNNQ). The plurality of p-doped injection layer sections can consist of a layer of pristine p-dopant. The pristine p-dopant can be 2,2'-(perfluoronaphthalene-2,6-diylidene) dimalononitrile (F6-TCNNQ).

[0010] Other systems, methods, features, and advantages of the present disclosure will be or become apparent to one with skill in the art upon examination of the following drawings and detailed description. It is intended that all such additional systems, methods, features, and advantages be included within this description, be within the scope of the present disclosure, and be protected by the accompanying claims. In addition, all optional and preferred features and modifications of the described embodiments are usable in all aspects of the disclosure taught herein. Furthermore, the individual features of the dependent claims, as well as all optional and preferred features and modifications of the described embodiments are combinable and interchangeable with one another.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Many aspects of the present disclosure can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present disclosure. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

[0012] FIG. 1 is a graphical representation illustrating an example of a tunneling mode of organic tunnel field effect transistors in accordance with various embodiments of the present disclosure.

[0013] FIGS. 2A, 2B, 3A, 3B, 4A and 4B are graphical representations of examples of organic tunnel field effect transistors in accordance with various embodiments of the present disclosure.

[0014] FIGS. 5A and 5B are plots illustrating examples of transistor output and transfer characteristics of the transistor of FIGS. 4A and 4B in the reverse (tunnel) direction in accordance with various embodiments of the present disclosure.

[0015] FIGS. 6A and 6B are graphical representations of examples of organic tunnel field effect transistors in accordance with various embodiments of the present disclosure.

[0016] FIGS. 7A and 7B are plots illustrating examples of characteristics of the transistor of FIGS. 6A and 6B in the reverse (tunnel) direction in accordance with various embodiments of the present disclosure.

[0017] FIGS. 8A-8F and 9A-9C are plots illustrating examples of transistor output and transfer characteristics of various embodiments of the transistor of FIGS. 6A and 6B in accordance with various embodiments of the present disclosure.

DETAILED DESCRIPTION

[0018] Disclosed herein are various embodiments related to organic tunnel field effect transistors. Organic electronics offers an emerging class of electronics in which the transistor acts as switching element. Generally, horizontal geometries can be used; however vertical structures can be utilized to overcome disadvantages such as long channel lengths. Reference will now be made in detail to the description of the embodiments as illustrated in the drawings, wherein like reference numbers indicate like parts throughout the several views.

[0019] In general, both of CMOS and organic devices can be operated in a forward direction, where the transistors are switched on by field effect control via the gate potential. The field effect control leads to a unipolar current from the source to the drain contact (forward direction) of the device. Using the technology of molecular doping, either for reducing the contact resistance at the source and/or drain contacts (contact doping) or for

controlling and stabilizing the threshold voltage (channel doping), the overall performance of the transistors can be improved. Tuning of the switching voltage of the transistors is further realized by changing the physical properties of the semiconductor-insulator interface, in particular filling trap states at this interface. Therefore, the doping density should be at least higher than the interface trap density. However, if the doping levels become too high, usually the off-currents of the transistor are increased from which the on/off ratio suffers.

[0020] The present disclosure presents an organic tunnel field effect transistor (OTFET) 100 which differs from known structures by its basic working principle, which is in reverse rather than the forward direction. FIG. 1 illustrates the OFET turned OFF (V_{GS}=0), and in the tunneling mode with the OFET turned ON (V_{GS}<0). The tunnel transistor 100 can be switched on by biasing the device in the break down regime, which is characterized by a tunnel current between the conduction and valence bands of two (or three) adjacent semiconductors. Such tunnel transistors 100 have been realized by employing an "artificial" p-i-n semiconductor hetero structure in a vertical geometry. This is "artificial" in the sense that the OTFET devices actually comprise only of a vertical stacking of intrinsic and n-doped layers, while the p-layer is induced in the on-state of the transistor 100 by the field effect produced when applying a negative potential to the gate.

[0021] The tunnel transistors 100 offer two main advantages that make them interesting for use in commercial applications in the field of organic electronics:

- Although employing highly doped layers, the transistors 100 can be completely switched off (i.e., the off-state currents remain low and are only limited by leakage effects). Therefore, the on/off ratio does not suffer and much higher doping levels than previously used are feasible, which can further improve the conductivity of the organic layers.
- The threshold (switching) voltage of the transistor 100 is not exclusively determined by the semiconductor-insulator interface properties or doping levels, respectively. It can be further controlled by the thickness of the organic layers, in particular for

vertical geometries since the tunnel break down strongly depends on the distance between the n-type and p-type layers.

- If employing a vertical stacking of different semiconductor materials (e.g., A, B and/or C), using a real semiconductor hetero-structure, operation of the tunnel transistor can be furthermore optimized by the choice of suitable materials in terms of high mobilities (vertical for semiconductor B and C, horizontal for A) as well as their relative energy levels, i.e., aiming a tuning of the effective tunnel gap, which is, e.g., HOMO(semiconductor A) to LUMO(semiconductor B).

[0022] Referring to FIGS. 2A and 2B, shown are examples of organic tunnel field effect transistors (OTFETs) 100 with a vertical structure. The OTFETs 100 include a substrate having a gate insulator layer 106 disposed on a gate 103. Disposed on the gate insulator layer 106, opposite the gate 103, is a passivation layer 109. After the pretreatment with the passivation layer 109, an intrinsic layer (i-layer) of semiconductor A 112 is formed on the passivation layer 109. After the layer of semiconductor A 112 is formed, injection sections 115 can be structured on the semiconductor A layer 112 using, e.g., evaporation through shadow masks or other appropriate patterning methods (e.g., photolithography).

[0023] As illustrated in the OTFET embodiment 100a of FIG. 2A, individual injection structures 115 can be formed on the layer of semiconductor A 112. The injection sections 115 improve the injection of holes at the source contacts 118 disposed on those sections 115. The source contacts 118 can then be formed on the injection sections 115 using, e.g., evaporation through shadow masks or other appropriate patterning methods. Insulator sections 121 can then be disposed on the source sections 118 using, e.g., evaporation through shadow masks or other appropriate patterning methods. The stacks of injection sections 115, source contacts 118 and insulator sections 121 can be referred to as source contact stacks.

[0024] As illustrated in the OTFET embodiment 100b of FIG. 2B, the individual injection structures 115 can be formed on the layer of semiconductor A 112. The drain contacts 133 can then be formed on the injection sections 115 using, e.g., evaporation through shadow

masks or other appropriate patterning methods. Insulator sections 121 can then be disposed on the drain sections 133 using, e.g., evaporation through shadow masks or other appropriate patterning methods. The stacks of injection sections 115, drain contacts 133 and insulator sections 121 can be referred to as drain contact stacks.

[0025] Following the formation of the insulator sections 121, additional layers can be formed on the OTFET 100 as illustrated in FIGS. 2A and 2B. A second intrinsic layer (i-layer) of semiconductor A or C can be disposed on the device to form a second semiconductor layer 124 on the exposed portions of the initial semiconductor layer 112. In some implementations, semiconductor A or C may also be disposed on the insulator sections 121. As can be seen in FIGS. 2A and 2B, the second layer of semiconductor A or C 124 covers the exposed portions of the source electrodes 118 or drain electrodes 133. The insulator sections 121 can also extend through the second semiconductor layer 124, providing separation between the second layer of semiconductor A or C 124 and the semiconductor sections on the insulator sections 121.

[0026] Following deposition of the second semiconductor layer 124, a doped layer of semiconductor B 130 can be disposed on the device, covering the second layer of semiconductor A or C 124, and covering and filling between the insulator sections 121 as shown in FIGS. 2A and 2B. A drain contact 133 (FIG. 2A) or a source contact 118 (FIG. 2B) can then be formed on the doped semiconductor B layer 130. The tunnel transistor 100 is a bipolar type device with electrons extracted in reverse direction at the top drain 133 in FIG. 2A or the drain contacts 133 in FIG. 2B. If two similar types of doping are used in layers 115 and 130 at both the source 118 and drain 133, then a monopolar transistor results and the tunnel effect is not possible, even with reverse operation.

[0027] Referring next to FIGS. 3A and 3B, shown are other examples of OTFETs 100. The OTFET 100 includes a substrate having a gate insulator layer 106 disposed on a gate 103. Disposed on the gate insulator layer 106, opposite the gate 103, is a passivation layer 109. After the pretreatment with the passivation layer 109, injection sections 115 can be structured on the passivation layer 109 using, e.g., evaporation through shadow masks or

other appropriate patterning methods (e.g., photolithography). The source contacts 118 in FIG. 3A or the drain contacts 133 in FIG. 3B can then be formed on the injection sections 115 using, e.g., evaporation through shadow masks or other appropriate patterning methods, and insulator sections 121 can then be disposed on the source sections 118 (FIG. 3A) or the drain sections 133 (FIG. 3B) using, e.g., evaporation through shadow masks or other appropriate patterning methods. The stacks of injection sections 115, source contacts 118 and insulator sections 121 can be referred to as source contact stacks. The stacks of injection sections 115, drain contacts 133 and insulator sections 121 can be referred to as drain contact stacks.

[0028] Following the formation of the insulator sections 121, additional layers can be formed on the OTFET 100 as illustrated in FIGS. 3A and 3B. An intrinsic layer (i-layer) of semiconductor A can be disposed on the device to form a semiconductor layer 124 on the exposed portions of the passivation layer 109. In some implementations, semiconductor A may also be disposed on the insulator sections 121. As can be seen in FIGS. 3A and 3B, the layer of semiconductor A 124 covers the exposed portions of the source electrodes 118 (FIG. 3A) or the drain electrodes 133 (FIG. 3B). The insulator sections 121 can also extend through the semiconductor layer 124, providing separation between the layer of semiconductor A 124 and the semiconductor sections on the insulator sections 121. Following deposition of the semiconductor A layer 124, a doped layer of semiconductor B 130 can be disposed on the device, covering the layer of semiconductor A 124, and covering and filling between the insulator sections 121 as shown in FIGS. 3A and 3B. A drain contact 133 (FIG. 3A) or a source contact 118 (FIG. 3B) can then be formed on the doped semiconductor B layer 130. While the examples have been illustrated with vertical structures, the OTFET are equally applicable to (horizontal) hetero-structure devices.

[0029] Referring now to FIGS. 4A and 4B, shown is an example of an organic tunnel field effect transistor (OTFET) 100a that was implemented with a vertical structure. The OTFET 100a includes a substrate having a thermal silicon oxide (SiOx) layer (gate insulator) 106 disposed on a silicon (Si) wafer 103, which may be utilized as the gate electrode. For

example, the SiOx layer 106 can formed on the Si wafer 103 with a thickness of about 300 nm or in a range from about 50 nm to about 500 nm. Other oxides may also be used for the gate insulator layer 106. For example, Al_2O_3 can be formed on the Si wafer 103 with a thickness in a range from about 2 nm to about 200 nm. Disposed on the SiOx layer 106, opposite the Si wafer 103, is a layer of hexamethyldisilazane (HMDS) as the passivation layer 109. The HDMS 109 can be applied to the SiOx layer 106 at room temperature for about 30 min. A thickness in the range of about 1-2 nm may be achieved. Other layers 106 can include, but are not limited to, self-aligned monolayers (SAMs) of n-octadecyltrichlorosilane (OTS) or phosphonic acids. After the pretreatment with HDMS 109, an intrinsic layer (i-layer) of undoped pentacene (i-P5) 112 (semiconductor A) is formed on the HDMS layer 109. The layer of pentacene 112 can be deposited at a rate of about 1 Å/s while at room temperature. For example, the i-P5 layer 112 can be formed with a thickness of about 20 nm or in a range of about 10 nm to about 100 nm.

[0030] After the i-P5 layer 112 is formed, p-doped injection sections 115 comprising, e.g., pristine 2,2'-(perfluoronaphthalene-2,6-diylidene) dimalononitrile (F6-TCNNQ) disposed on a blend of F6-TCNNQ and pentacene (P5) can be structured on the i-P5 layer 112 to form a p-doped section of P5 (p-P5) using, e.g., evaporation through shadow masks or other appropriate patterning methods (e.g., photolithography). The F6-TCNNQ doping of the blend can be about 8 wt% or in a range from about 1wt% to about 8 wt%. As illustrated in FIG. 2A, individual p-doped structures 115 can be formed on the i-P5 layer 112. For example, the p-doped structures 115 can be formed by evaporation (or deposition) of a P5:F6-TCNNQ blend on the i-P5 layer 112 at a rate of about 1 Å/s while at room temperature, followed by evaporation (or deposition) of the pristine F6-TCNNQ at a rate of about 0.05 Å/s while at room temperature. In one embodiment, among others, the structured p-doped sections 115 comprise a layer of pristine F6-TCNNQ with a thickness of about 2 nm disposed on a layer of the P5:F6-TCNNQ blend with a thickness of about 10 nm or in a range from about 10 nm to about 100 nm. Other p-dopants that can be utilized to

form the blend and pristine layers include, e.g., tetrafluoro-tetracyanoquinonedimethane (F4TCNQ) or C60F36.

[0031] The p-doped sections 115 improve the injection of holes at the source contacts 118 disposed on those sections 115. The source contacts 118 can then be formed on the p-doped sections 115 using, e.g., evaporation through shadow masks or other appropriate patterning methods (e.g., lithography). While aluminum (Al) is used to form the electrodes in the example of FIG. 4A, other appropriate metals (e.g., silver, gold or platinum) can also be used. For example, Al can be disposed on the p-doped sections 115 at a rate of about 0.3 Å/s while at room temperature to form structured sections of the Al layer 118. In one embodiment, the source contacts 118 have a thickness of about 30 nm or in a range from about 20 nm to about 40 nm. Isolating SiOx 121 (source insulator) can then be disposed on the Al sections 118 using, e.g., evaporation through shadow masks or other appropriate patterning methods. The SiOx sections 121 can be structured at a rate of about 0.2 Å/s while at room temperature. For example, the SiOx sections 121 can be formed with a thickness of about 100 nm or in a range from about 50 nm to about 200 nm. The stacks of p-doped injection sections 115, source contacts 118 and SiOx insulator sections 121 can be referred to as source contact stacks.

[0032] After the SiOx sections 121 have been formed as shown in FIG. 4A, they are allowed to sit in air at room temperature for about 15 minutes, followed by 1 hour at 80°C in a glovebox. Following this time, additional layers can be formed on the OTFET 100a as illustrated in FIG. 4B. A second intrinsic layer (i-layer) of undoped pentacene (i-P5) is disposed on the device to form a second i-P5 layer 124 (semiconductor A) on the exposed portions of the initial i-P5 layer 112 (semiconductor A) and i-P5 sections 127 (semiconductor A) on the SiOx sections 121. The i-P5 can be applied at a rate of about 1 Å/s while at room temperature. For example, the second i-P5 layer 124 and i-P5 sections 127 can be formed with a thickness of about 100 nm or in a range from about 50 nm to about 200 nm. As illustrated in FIG. 2A, this layer may be formed of a different intrinsic semiconductor material (semiconductor C), which may have a similar thickness range or may have a smaller range

(e.g., about 5 nm to about 20 nm) depending on the type of semiconductor material being used. As can be seen in FIG. 4B, the second i-P5 layer 124 covers the exposed portions of the source electrodes 118. The SiOx sections 121 can also extend through the second i-P5 layer 124, providing separation between the second i-P5 layer 124 and the i-P5 sections 127 on the SiOx sections 121. The i-P5 sections 127 can be considered part of the source contact stacks, while the second i-P5 layer 124 surrounds the source contact stacks and extends over the height of the source contacts 118 and at least partially up the SiOx sections 121.

[0033] Following deposition of the second i-P5 layer 124 and sections 127, a layer of n-doped pentacene (n-P5) 130 (semiconductor B) is disposed on the device, covering the second i-P5 layer 124 and the i-P5 sections 127, and may fill in between the SiOx sections 121 as shown in FIG. 4B. In one embodiment, among others, the n-P5 comprises pentacene blended with tetrakis (1,3,4,6,7,8-hexahydro-2H-pyrimido [1 ,2-a] pyrimidinato) ditungsten (II) (W2(hpp)4). The W2(hpp)4 doping of the n-P5 can be about 8 wt% or a range from about 2 wt% to about 16 wt%. The n-P5 can be applied at a rate of about 1 Å/s while at room temperature. For example, the n-P5 layer 130 can be formed with a thickness in a range from about 100 nm to about 150 nm or a range from about 50 nm to about 200 nm. Other n-dopants that can be utilized to form the n-P5 layer include, e.g., 3,6-bis-(dimethyl amino)-cridine, bis(ethylene-dithio) tetrathiafulvalene (BEDT-TTF), oxocarbon, or pseudooxocarbonderivatives.

[0034] A drain contact 133 can then be formed on the n-P5 layer 130. While aluminum (Al) is used to form the electrode in the example of FIG. 4B, other appropriate metals (e.g., silver, gold or platinum) can also be used. For example, Al can be disposed on the n-P5 layer 130 at a rate of about 0.3 Å/s while at room temperature. In one embodiment, the drain contact 133 has a thickness of about 30 nm or a range from about 20 nm to about 40 nm. The tunnel transistor 100a is a bipolar type device with electrons injected at the top drain 133. If two similar types of doping are used in layers 115 and 130 at both the source

118 and drain 133, then a monopolar transistor results and the tunnel effect is not possible, even with reverse operation.

[0035] In some embodiments, the p-doped sections 115 may not include a layer of p-doped pentacene (p-P5) such as the blend of F6-TCNNQ and P5. The p-doped sections 115 can be formed of a single layer of pristine F6-TCNNQ structured on the i-P5 layer 112. For example, the single layer can be formed by evaporation (or deposition) of the pristine F6-TCNNQ at a rate of about 0.05 Å/s while at room temperature, resulting in a layer of pristine F6-TCNNQ with a thickness of about 2 nm (or a range of about 1-2 nm) disposed on the i-P5 layer 112. Operation of the transistor 100a is provided by the combination of p-doped layer 115 at the source 118 and the n-P5 layer 130 at the drain 133. In alternative embodiments, sections 115 can comprise n-doped P5 with layer 130 comprising p-doped P5.

[0036] The thickness of the second i-P5 layer 124 determines the tunnel break down voltage (the minimum voltage needed to be applied to the top drain 133) to get the tunnel transistor 100 to operate once the gate 103 has been switched on. Roughness is an issue in pentacene based devices, so a comparably thick second i-P5 layer 124 is used under the n-P5 layer 130.

[0037] Referring to FIGS. 5A and 5B, shown are plots illustrating examples of the transistor output and transfer characteristics of the transistor of FIGS. 4A and 4B in the reverse (tunnel) direction. The disclosed output and transfer characteristics illustrate the principles of the tunnel field effect transistors.

[0038] Referring next to FIGS. 6A and 6B, shown is another example of an OTFET 100c that was implemented with a vertical structure. The OTFET 100c includes an anodic aluminum oxide (Al_2O_3) layer (gate insulator) 106 disposed on an aluminum (Al) layer 103, which may be utilized as the gate electrode. For example, the aluminum layer 103 can be formed on a glass substrate with a thickness of about 150 nm or in a range from about 50 nm to about 200 nm. The Al_2O_3 layer 106 can formed on the Al layer 103 with a thickness of about 100 nm or in a range from about 2 nm to about 200 nm. Other oxides may also be

used for the gate insulator layer 106. For example, SiOx can be formed on the Al layer 103 with a thickness in a range from about 50 nm to about 500 nm. Disposed on the Al_2O_3 layer 106, opposite the Al layer 103, is a layer of tetratetracontane (TTC) as the passivation layer 109. The TTC 109 can be applied to the Al_2O_3 layer 106 with a thickness of about 30 nm or in a range from about 10 nm to about 60 nm. After the pretreatment with TTC 109, an intrinsic layer (i-layer) of undoped pentacene (i-P5) 112 (semiconductor A) is formed on the TTC layer 109. The layer of pentacene 112 can be deposited at a rate of about 1 Å/s while at room temperature. For example, the i-P5 layer 112 can be formed with a thickness of about 45 nm or in a range of about 10 nm to about 100 nm.

[0039] After the i-P5 layer 112 is formed, p-doped injection sections 115 comprising, e.g., a blend of $C_{60}F_{36}$ and pentacene (P5) can be structured on the i-P5 layer 112 to form a p-doped section of P5 (p-P5) using, e.g., evaporation through shadow masks or other appropriate patterning methods (e.g., photolithography). The $C_{60}F_{36}$ doping of the blend can be about 1.92 mol% or in a range from about 0.5 mol% to about 10 mol%. As illustrated in FIG. 6A, individual p-doped structures 115 can be formed on the i-P5 layer 112. For example, the p-doped structures 115 can be formed by evaporation (or deposition) of a P5: $C_{60}F_{36}$ blend on the i-P5 layer 112. This may be followed by evaporation (or deposition) of pristine $C_{60}F_{36}$. In one embodiment, among others, the structured p-doped sections 115 have a thickness of about 40 nm or in a range from about 10 nm to about 100 nm. Other p-dopants that can be utilized to form the blend and pristine layers include, e.g., tetrafluoro-tetracyanoquinonedimethane (F4TCNQ) or 2,2'-(perfluoronaphthalene-2,6-diylidene) dimalononitrile (F6-TCNNQ). In some embodiments, the p-doped sections 115 may not include a layer of p-doped pentacene (p-P5), but instead may be formed of a single layer of pristine $C_{60}F_{36}$ or F6-TCNNQ structured on the i-P5 layer 112.

[0040] The p-doped sections 115 improve the injection of holes at the drain contacts 133 disposed on those sections 115. The drain contacts 133 can then be formed on the p-doped sections 115 using, e.g., evaporation through shadow masks or other appropriate patterning methods (e.g., lithography). While aluminum (Al) can be used to form the

electrodes 133, other appropriate metals (e.g., silver, gold or platinum) can also be used. For example, Al can be disposed on the p-doped sections 115 at a rate of about 0.3 Å/s while at room temperature to form structured sections of the Al layer 133. In one embodiment, the drain contacts 133 have a thickness of about 30 nm or in a range from about 20 nm to about 40 nm. Isolating SiOx 121 (drain insulator) can then be disposed on the Al sections 133 using, e.g., evaporation through shadow masks or other appropriate patterning methods. For example, the SiOx sections 121 can be formed with a thickness of about 200 nm or in a range from about 50 nm to about 200 nm. The stacks of p-doped injection sections 115, drain contacts 133 and SiOx insulator sections 121 can be referred to as drain contact stacks.

[0041] After the SiOx sections 121 have been formed as shown in FIG. 6A, additional layers can be formed on the OTFET 100c similar to the layers illustrated in FIG. 2B. A second intrinsic layer (i-layer) of undoped pentacene (i-P5) can be disposed on the device to form a second i-P5 layer 124 (semiconductor A) on the exposed portions of the initial i-P5 layer 112 (semiconductor A) and the drain contact stacks. For example, the second i-P5 layer 124 and i-P5 sections 127 can be formed with a thickness of about 30 nm, about 50 nm, about 70 nm, about 90 nm, in a range from about 30 nm to about 150 nm, or in a range from about 10 nm to about 200 nm. As illustrated in FIG. 2B, this layer may be formed of a different intrinsic semiconductor material (semiconductor C), which may have a similar thickness range or may have a smaller range (e.g., about 5 nm to about 20 nm) depending on the type of semiconductor material being used. As can be seen in FIG. 6B, the second i-P5 layer 124 covers the exposed sides of the drain electrodes 133 and the SiOx insulator sections 121.

[0042] Following deposition of the second i-P5 layer 124, a layer of n-doped pentacene (n-P5) 130 (semiconductor B) is disposed on the device, covering the second i-P5 layer 124, as shown in FIG. 6B. In one embodiment, among others, the n-P5 comprises pentacene blended with tetrakis (1,3,4,6,7,8-hexahydro-2H-pyrimido [1 ,2-a] pyrimidinato) ditungsten (II) ($W_2(hpp)_4$). The $W_2(hpp)_4$ doping of the n-P5 can be about 2.9 mol% or a range from about

0.5 mol% to about 10 mol%. For example, the n-P5 layer 130 can be formed with a thickness of about 40 nm or in a range from about 40 nm to about 150 nm or a range from about 20 nm to about 200 nm. Other n-dopants that can be utilized to form the n-P5 layer include, e.g., 3,6-bis-(dimethyl amino)-cridine, bis(ethylene-dithio) tetrathiafulvalene (BEDT-TTF), oxocarbon, or pseudooxocarbonderivatives.

[0043] A source contact 118 can then be formed on the n-P5 layer 130. While aluminum (Al) is used to form the electrode in the example of FIG. 6B, other appropriate metals (e.g., silver, gold or platinum) can also be used. In one embodiment, the source contact 118 has a thickness of about 130 nm or a range from about 50 nm to about 150 nm or a range from about 20 nm to about 200 nm. The tunnel transistor 100c is a bipolar type device with electrons injected at the top source 118. Operation of the transistor 100c is provided by the combination of p-doped layer 115 at the drain 133 and the n-P5 layer 130 at the source 118. The thickness of the second i-P5 layer 124 determines the tunnel break down voltage (the minimum voltage needed to be applied to the drain contacts 133) to get the tunnel transistor 100c to operate once the gate 103 has been switched on. In alternative embodiments, sections 115 can comprise n-doped P5 with layer 130 comprising p-doped P5. In this case, the devices are switched on by positive gate voltages, thus, having an n-type channel.

[0044] Referring to FIGS. 7A and 7B, shown are plots illustrating examples of the currents of the transistor of FIGS. 6A and 6B in the reverse (tunnel) direction ($V_D<0$ and $V_{GS}<0$). A tunneling OFET is achieved with an ON/OFF ratio of 10^5, which is applicable for commercial devices. Ultra-low off current in the range of 10^{-11} A provides low-energy consumption. The gate current (I_G) is limited to a range of 10^{-8} A.

[0045] FIGS. 8A-8D and 8E-8F show plots illustrating examples of the transfer characteristics and transistor output of the transistor of FIGS. 6A and 6B with a 30 nm intrinsic pentacene (i-P5) layer 124. The disclosed output and transfer characteristics illustrate the principles of the tunnel field effect transistors. The off current ($I_{D,off}$) depends strongly on the drain voltage (V_{DS}) with $I_{D,off}$ being about 10^{-9} A at V_{DS} = -8V and $I_{D,off}$ being

about 10^{-10} A at V_{DS} = -4V. An ON/OFF ratio of 10^4 was seen at V_{DS} = -8V and 10^5 was seen at V_{DS} = -4V. The output current behaves as standard OFETs (with linear and saturation regions) when V_{GS} is less than -8V. When V_{GS} is greater than -8V, the drain current I_D increases with increasing V_D as with a PIN diode. FIGS. 9A-9C show plots illustrating examples of the transfer characteristics of the transistor of FIGS. 6A and 6B with a thicker 50 nm i-P5 layer 124.

[0046] It should be emphasized that the above-described embodiments of the present disclosure are merely possible examples of implementations set forth for a clear understanding of the principles of the disclosure. Many variations and modifications may be made to the above-described embodiment(s) without departing substantially from the spirit and principles of the disclosure. All such modifications and variations are intended to be included herein within the scope of this disclosure and protected by the following claims.

[0047] It should be noted that ratios, concentrations, amounts, and other numerical data may be expressed herein in a range format. It is to be understood that such a range format is used for convenience and brevity, and thus, should be interpreted in a flexible manner to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. To illustrate, a concentration range of “about 0.1% to about 5%” should be interpreted to include not only the explicitly recited concentration of about 0.1 wt% to about 5 wt%, but also include individual concentrations (*e.g.*, 1%, 2%, 3%, and 4%) and the sub-ranges (*e.g.*, 0.5%, 1.1%, 2.2%, 3.3%, and 4.4%) within the indicated range. The term “about” can include traditional rounding according to significant figures of numerical values. In addition, the phrase “about ‘x’ to ‘y’” includes “about ‘x’ to about ‘y’”.

CLAIMS

Therefore, at least the following is claimed:

1. An organic tunnel field effect transistor, comprising:

a first intrinsic layer (i-layer) of organic semiconductor material disposed over a gate insulating layer, where the first i-layer of organic semiconductor material is undoped;

a plurality of source contact stacks disposed on portions of the first i-layer of organic semiconductor material, each of the plurality of source contact stacks comprising:

a p-doped injection layer disposed on a corresponding portion of the first i-layer of organic semiconductor material;

a source contact layer disposed on the p-doped injection layer; and

a source contact insulating layer disposed on the source contact layer;

a second i-layer of organic semiconductor material disposed on the first i-layer of organic semiconductor material surrounding the plurality of source contact stacks, where a thickness of the second i-layer of organic semiconductor material is greater than a combined thickness of the p-doped injection layer and the source contact layer, and the second i-layer of P5 is undoped;

an n-doped organic semiconductor layer disposed on the second i-layer of organic semiconductor material surrounding and disposed on the plurality of source contact stacks; and

a drain contact layer disposed on the n-doped organic semiconductor layer.

2. The organic tunnel field effect transistor of claim 1, wherein each of the plurality of source contact stacks includes a stack i-layer of organic semiconductor material disposed on the source contact insulating layer, where the stack i-layer of organic semiconductor material is undoped and a thickness of the stack i-layer of organic

semiconductor material corresponds to the thickness of the second i-layer of organic semiconductor material.

3. The organic tunnel field effect transistor of claim 2, wherein the thickness of the second i-layer of organic semiconductor material and the stack i-layer of organic semiconductor material is about 30 nm or more.

4. The organic tunnel field effect transistor of any of claims 1-3, wherein the first i-layer of organic semiconductor material and the second i-layer of organic semiconductor material comprise undoped pentacene (P5).

5. The organic tunnel field effect transistor of claim 4, wherein the n-doped organic semiconductor layer comprises n-doped pentacene (n-P5).

6. The organic tunnel field effect transistor of claim 5, wherein the thickness of the n-doped organic semiconductor layer is about 30 nm or more.

7. The organic tunnel field effect transistor of any of claims 1-3, wherein the organic semiconductor material of the first i-layer is different than the organic semiconductor material of the second i-layer.

8. The organic tunnel field effect transistor of any of claims 1-7, wherein the p-doped injection layer comprises a p-doped P5 (p-P5) layer disposed on the corresponding portion of the first i-layer of organic semiconductor material, the p-P5 layer comprising a blend of P5 and a p-dopant.

9. The organic tunnel field effect transistor of claim 8, wherein the p-dopant is 2,2'-(perfluoronaphthalene-2,6-diylidene) dimalononitrile (F6-TCNNQ).

10. The organic tunnel field effect transistor of claim 8, wherein the p-doped injection layer comprises a pristine p-dopant layer disposed on the p-P5 layer, the pristine p-dopant layer consisting of the p-dopant.

11. The organic tunnel field effect transistor of claim 10, wherein the p-P5 layer has a thickness of about 10 nm and the pristine p-dopant layer has a thickness of about 2 nm.

12. The organic tunnel field effect transistor of any of claims 1-7, wherein the p-doped injection layer consists of pristine p-dopant disposed on the corresponding portion of the first i-layer of organic semiconductor material.

13. The organic tunnel field effect transistor of claim 12, wherein the p-dopant is 2,2'-(perfluoronaphthalene-2,6-diylidene) dimalononitrile (F6-TCNNQ).

14. The organic tunnel field effect transistor of any of claims 1-13, wherein an n-doped organic semiconductor layer extends beyond the source contact insulating layer.

15. An organic tunnel field effect transistor, comprising:

a first intrinsic layer (i-layer) of organic semiconductor material disposed over a gate insulating layer, where the first i-layer of organic semiconductor material is undoped;

a plurality of drain contact stacks disposed on portions of the first i-layer of organic semiconductor material, each of the plurality of drain contact stacks comprising:

a p-doped injection layer disposed on a corresponding portion of the first i-layer of organic semiconductor material;

a drain contact layer disposed on the p-doped injection layer; and

a drain contact insulating layer disposed on the drain contact layer;

a second i-layer of organic semiconductor material disposed on the first i-layer of organic semiconductor material surrounding the plurality of drain contact stacks, where a thickness of the second i-layer of organic semiconductor material is greater than a combined thickness of the p-doped injection layer and the drain contact layer, and the second i-layer of P5 is undoped;

an n-doped organic semiconductor layer disposed on the second i-layer of organic semiconductor material surrounding and disposed on the plurality of drain contact stacks; and

a source contact layer disposed on the n-doped organic semiconductor layer.

16. A method, comprising:

disposing a first intrinsic layer (i-layer) of organic semiconductor material over a gate insulating layer;

forming a plurality of p-doped injection layer sections on corresponding portions of the first i-layer of organic semiconductor material;

forming a plurality of source contacts on corresponding ones of the plurality of p-doped injection layer sections;

forming a plurality of source contact insulation layer sections on corresponding ones of the plurality of source contacts;

disposing a second i-layer of organic semiconductor material on the first i-layer of organic semiconductor material surrounding the plurality of p-doped injection layer sections and the plurality of source contacts;

disposing an n-doped organic semiconductor layer on the second i-layer of organic semiconductor material, the n-doped organic semiconductor layer encapsulating portions of the plurality of source contact insulation layer sections; and

disposing a drain contact on the n-doped organic semiconductor layer.

17. The method of claim 16, wherein the first i-layer of organic semiconductor material and the second i-layer of organic semiconductor material comprise undoped pentacene (P5).

18. The method of claim 17, wherein the thickness of the second i-layer of organic semiconductor material is about 30 nm or more.

19. The method of any of claims 17 or 18, wherein the n-doped organic semiconductor layer comprises n-doped pentacene (n-P5).

20. The method of claim 19, wherein the thickness of the n-doped organic semiconductor layer is about 30 nm or more.

21. The method of claim 16, wherein the organic semiconductor material of the first i-layer is different than the organic semiconductor material of the second i-layer.

22. The method of any of claims 16-21, wherein forming the plurality of p-doped injection layer sections comprises:

forming a plurality of p-doped P5 (p-P5) layer sections on the corresponding portions of the first i-layer of organic semiconductor material, the p-P5 layer sections comprising a blend of P5 and a p-dopant; and

forming a plurality of pristine p-dopant layer sections on corresponding ones of the p-P5 layer sections, the pristine p-dopant layer sections consisting of the p-dopant.

23. The method of claim 22, wherein the p-dopant is 2,2'-(perfluoronaphthalene-2,6-diylidene) dimalononitrile (F6-TCNNQ).

24. The method of any of claims 16-21, wherein the plurality of p-doped injection layer sections consists of a layer of pristine p-dopant.

25. The method of claim 24, wherein the pristine p-dopant is 2,2'-(perfluoronaphthalene-2,6-diylidene) dimalononitrile (F6-TCNNQ).

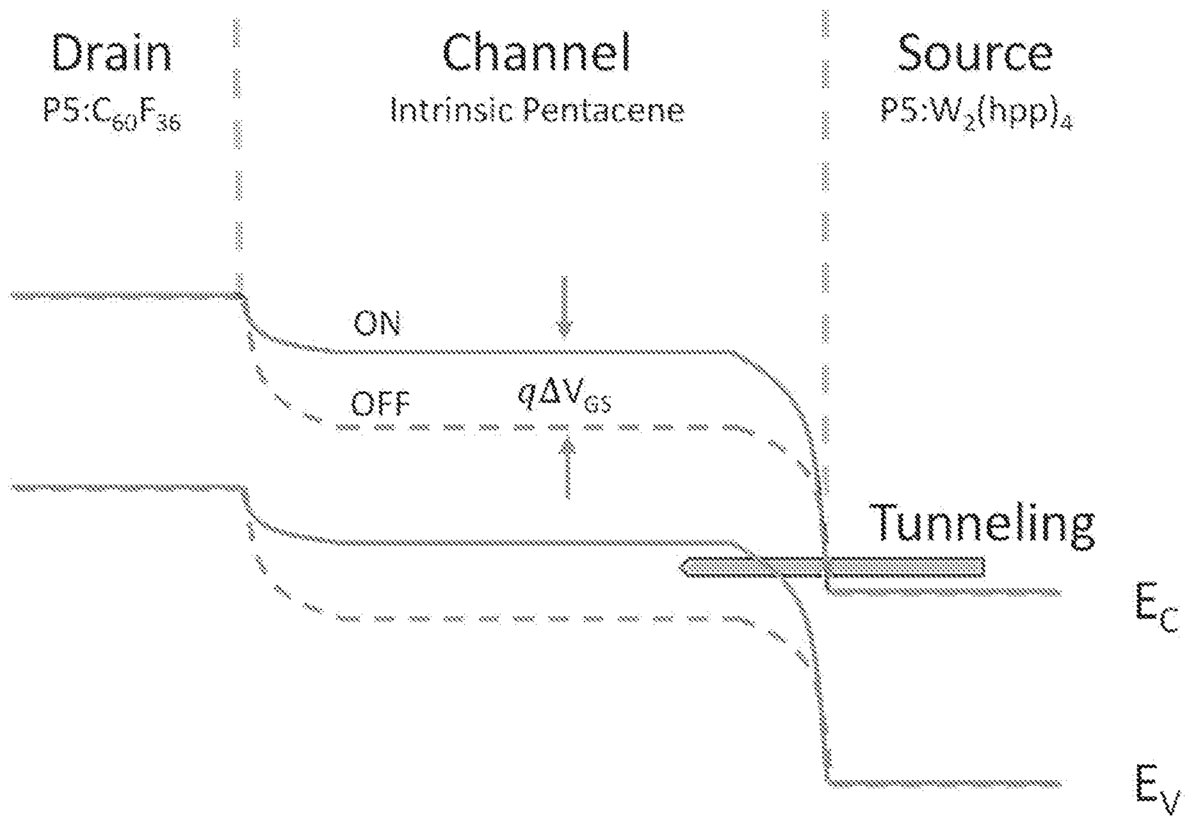

FIG. 1

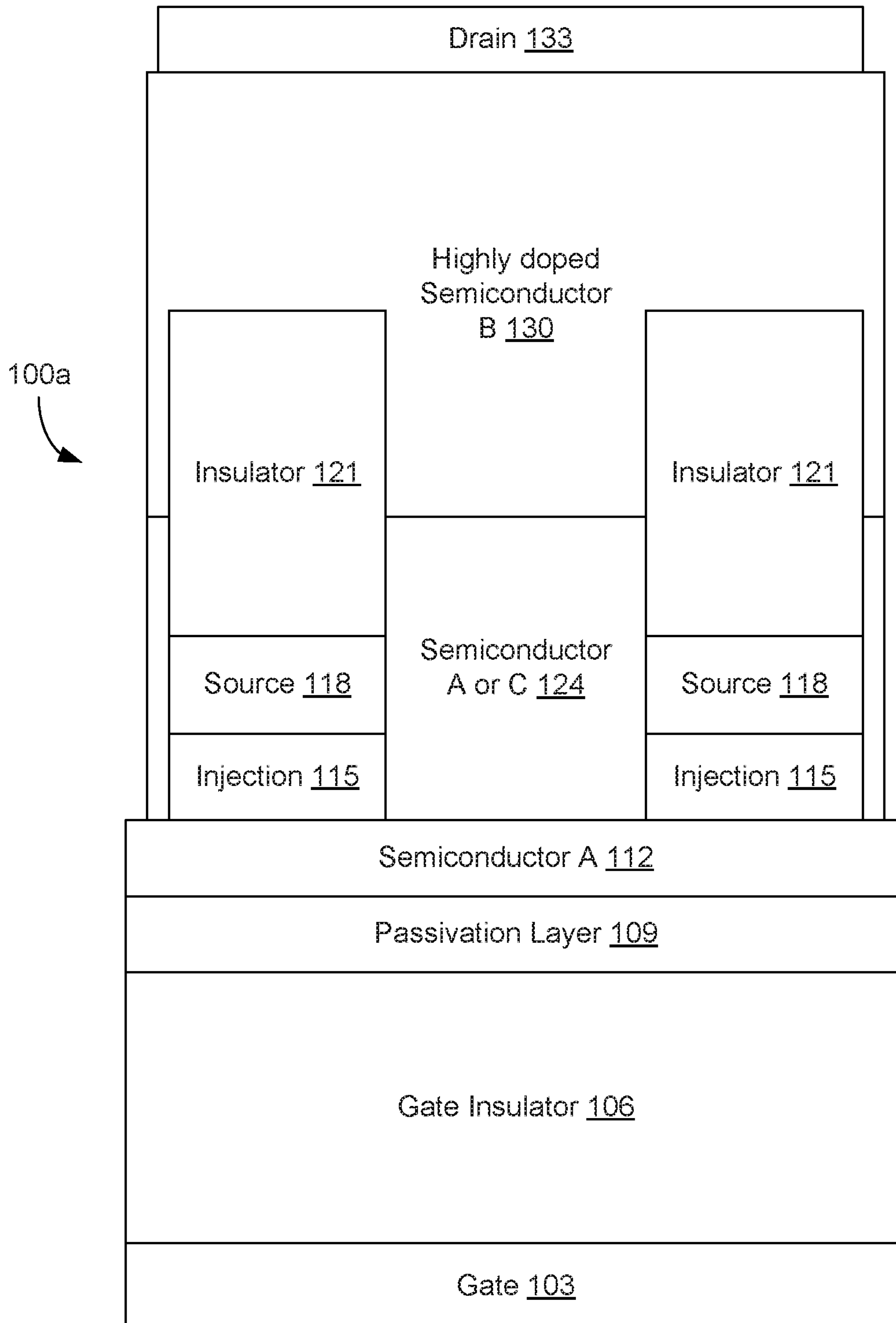

FIG. 2A

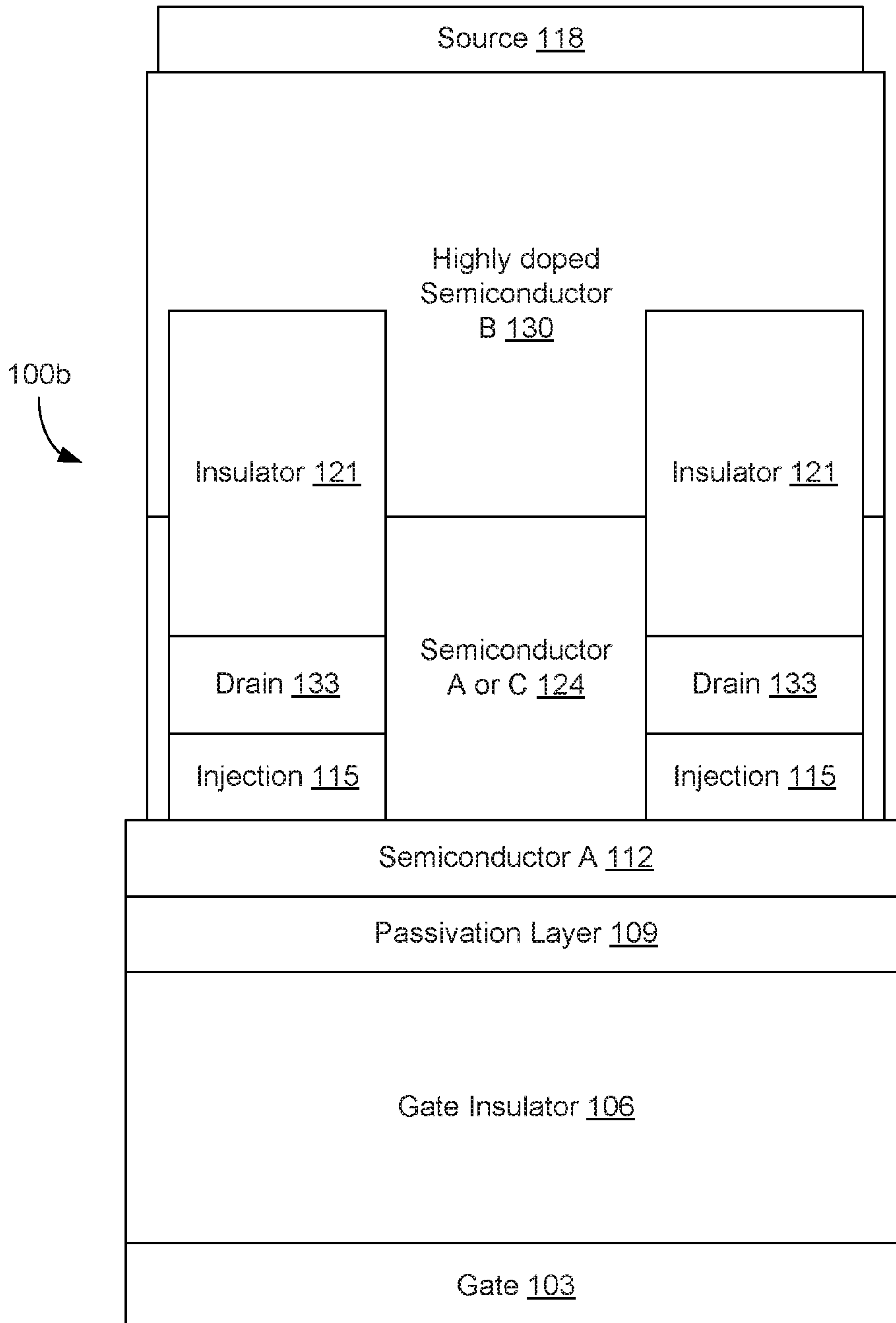

FIG. 2B

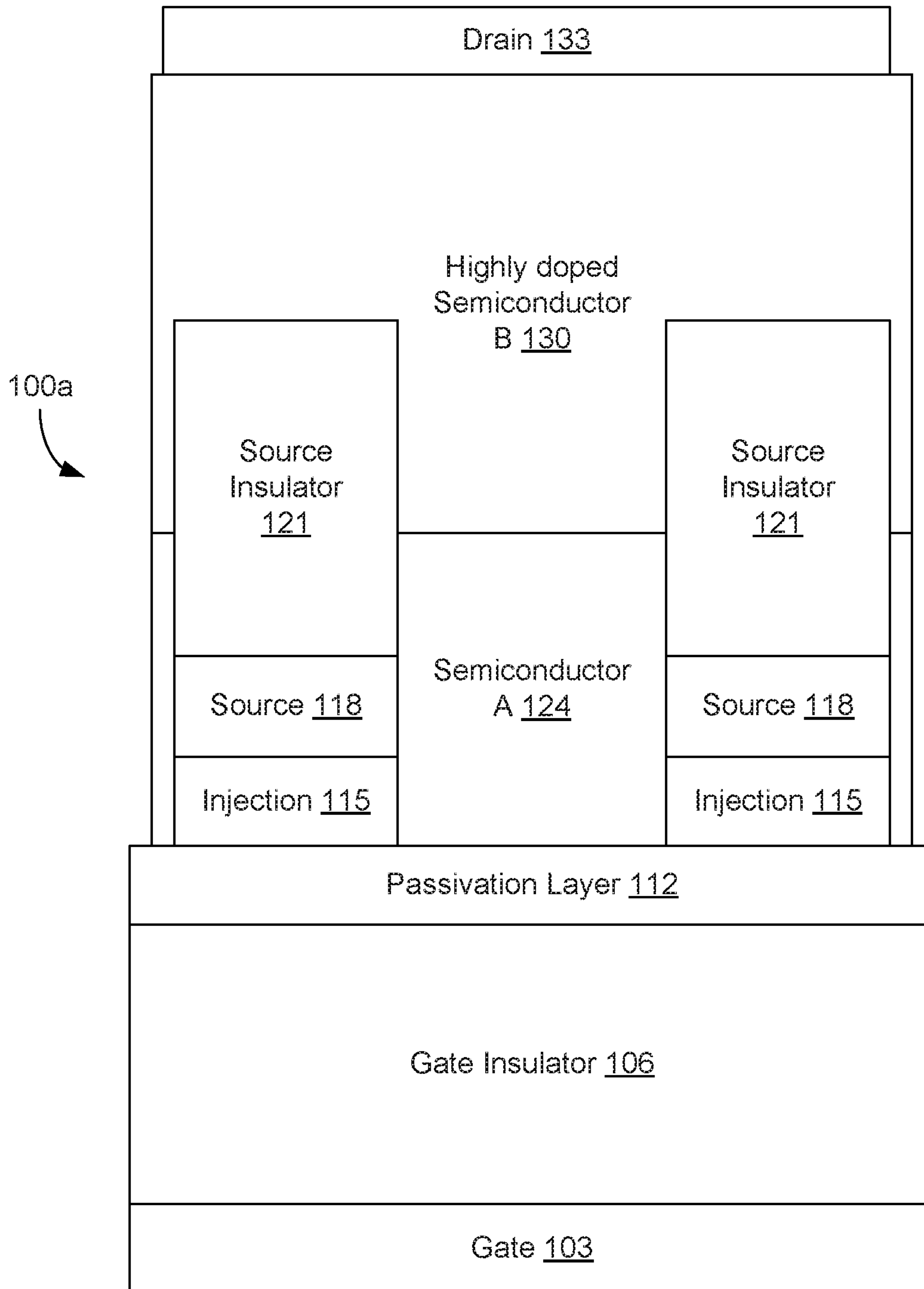

FIG. 3A

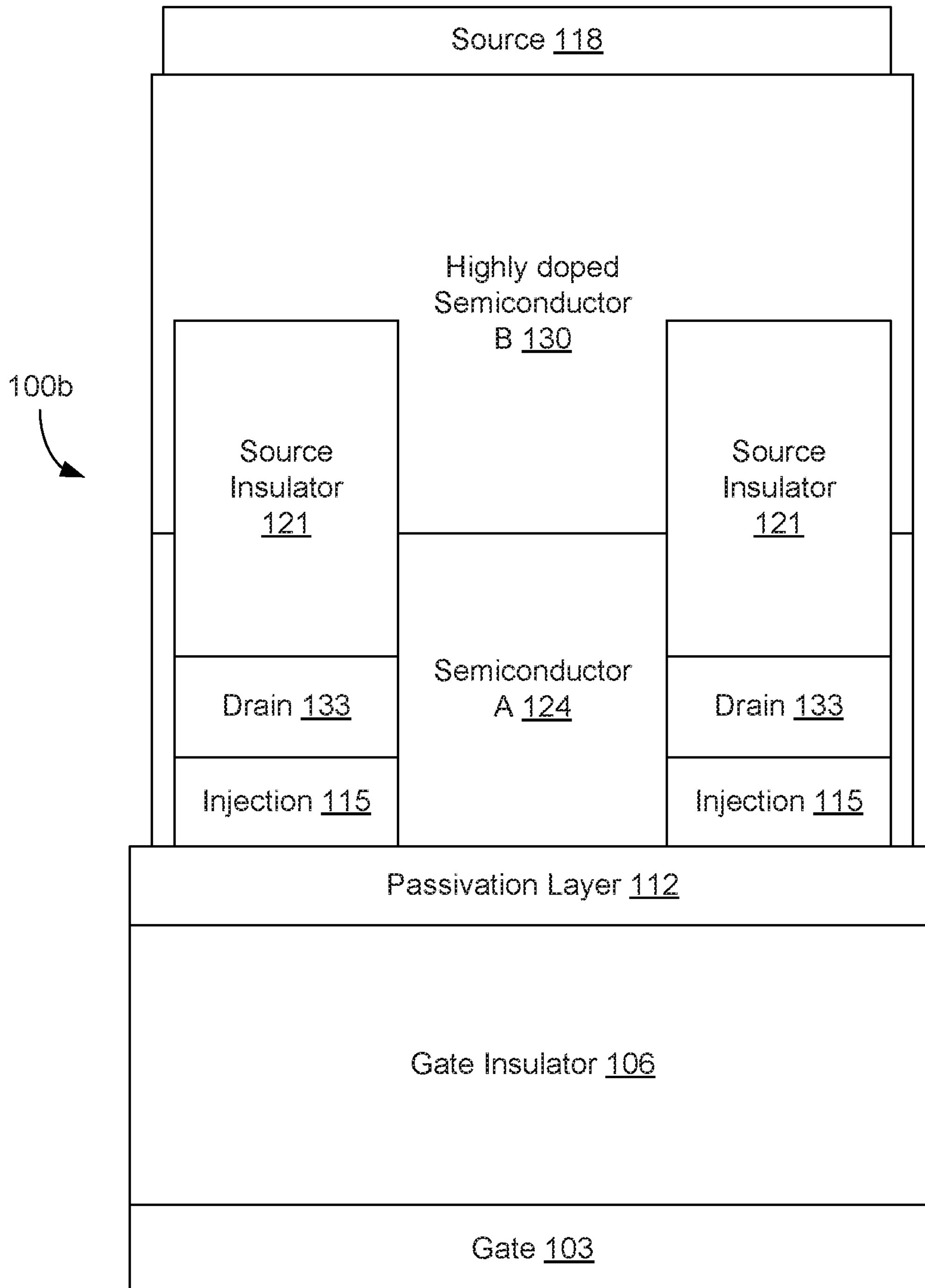

FIG. 3B

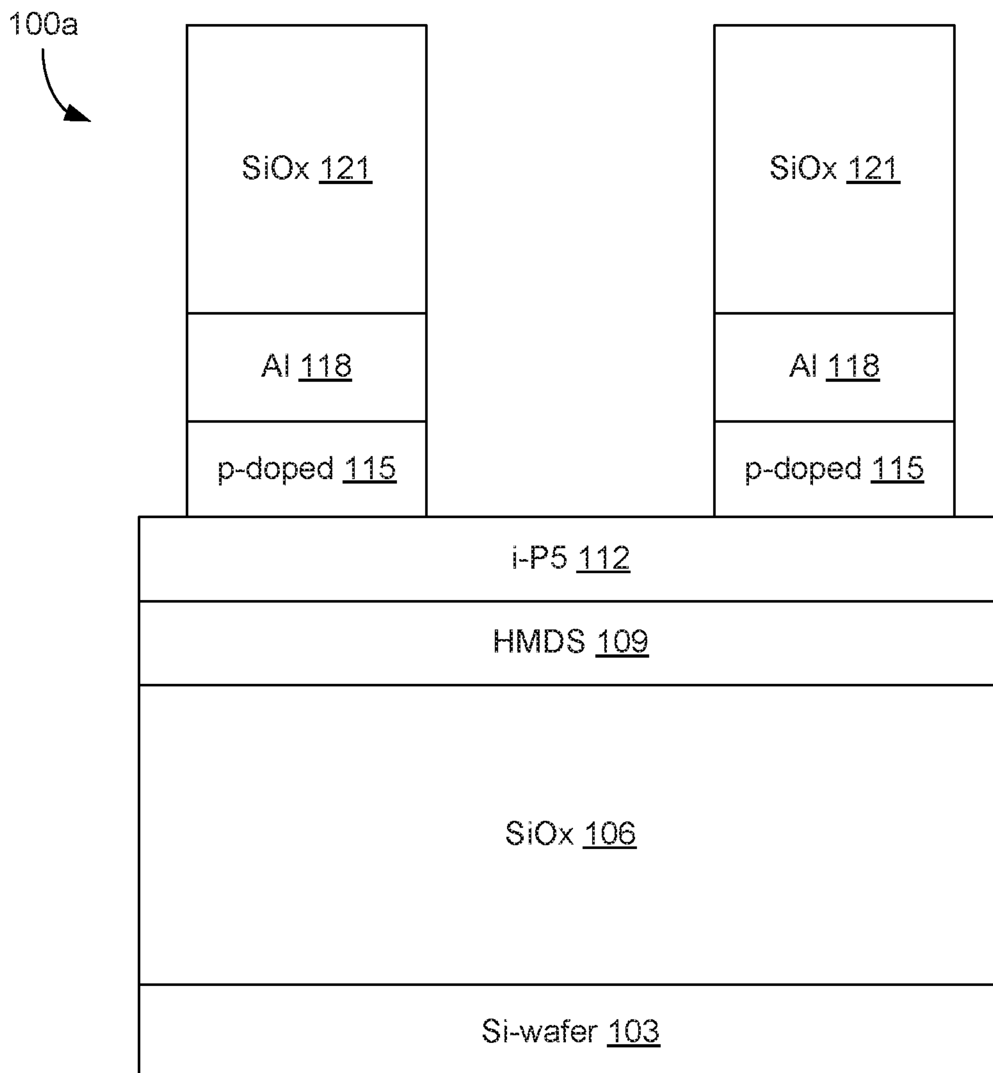

FIG. 4A

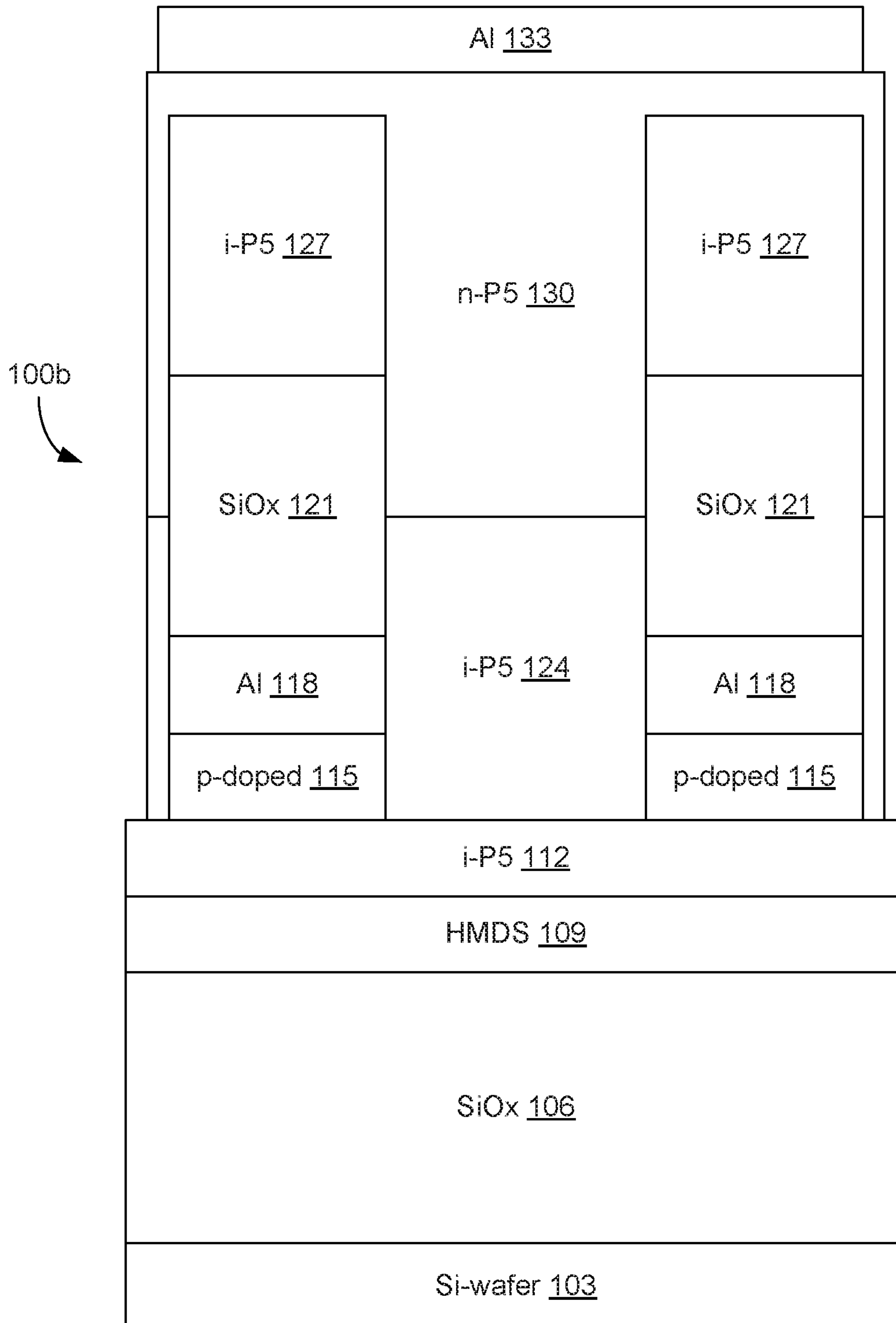

FIG. 4B

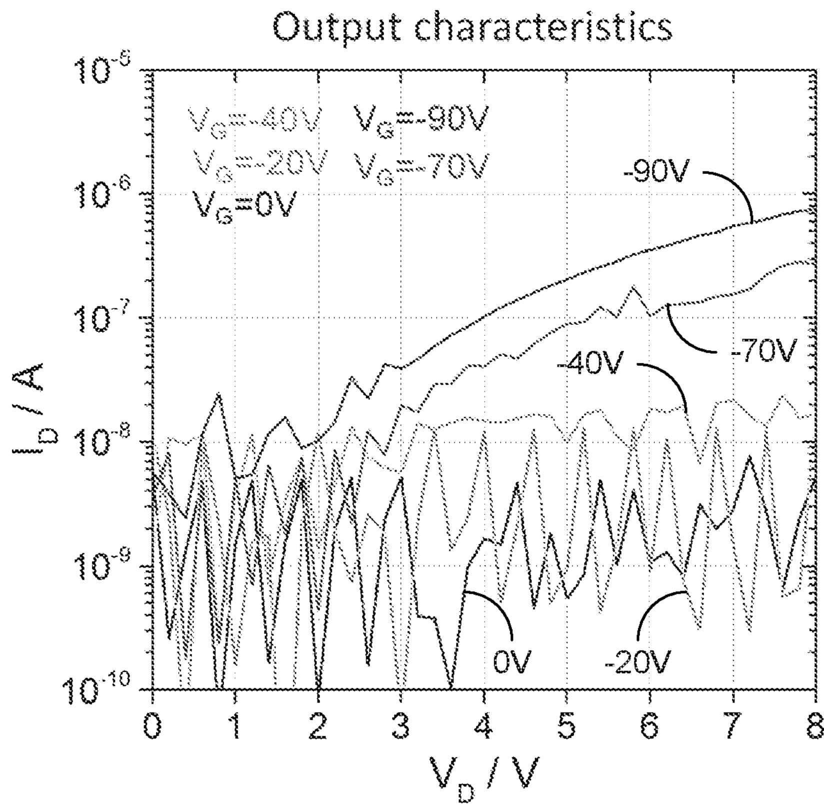

FIG. 5A

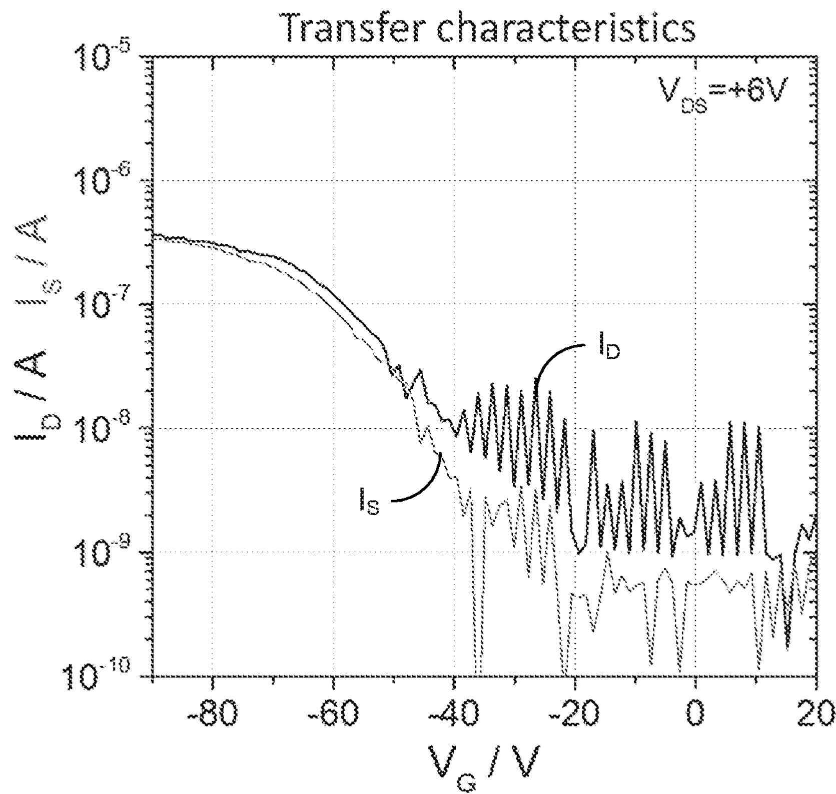

FIG. 5B

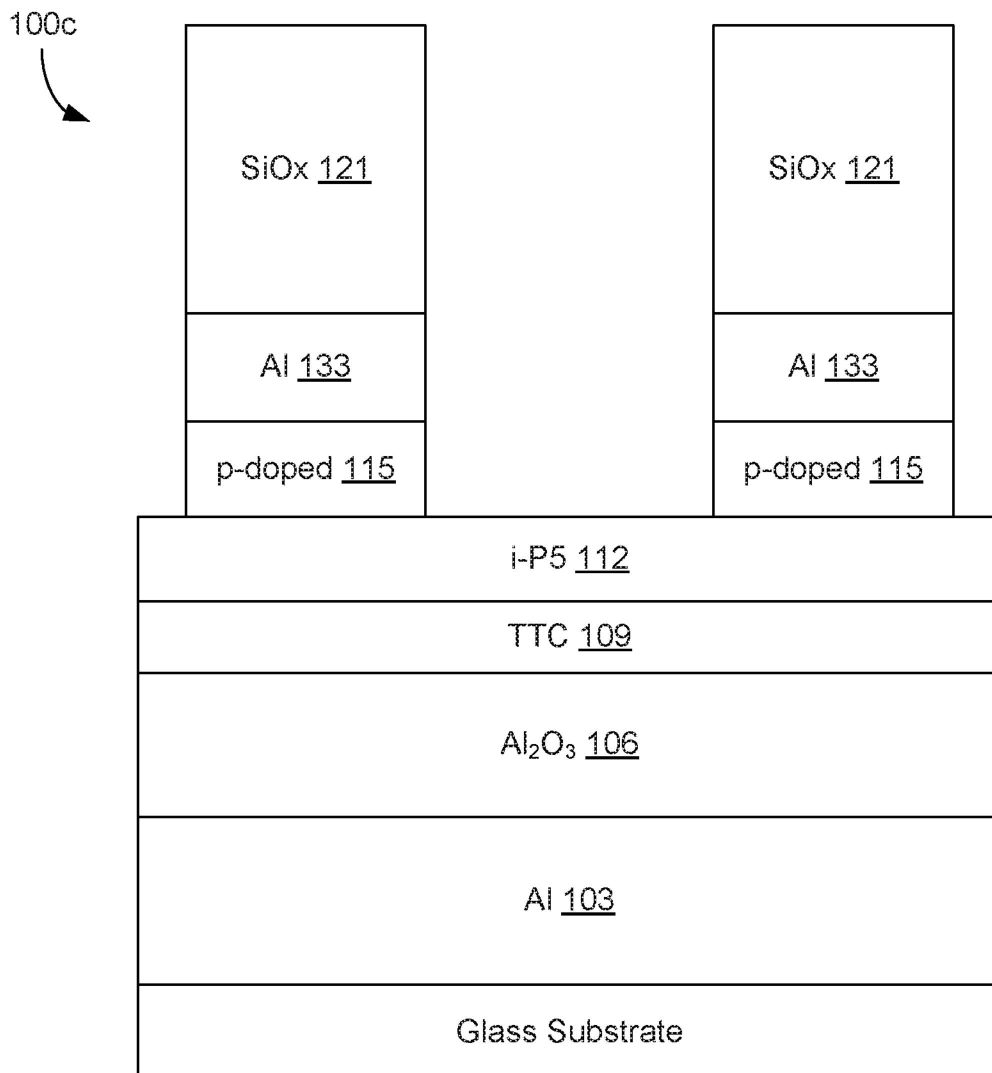

FIG. 6A

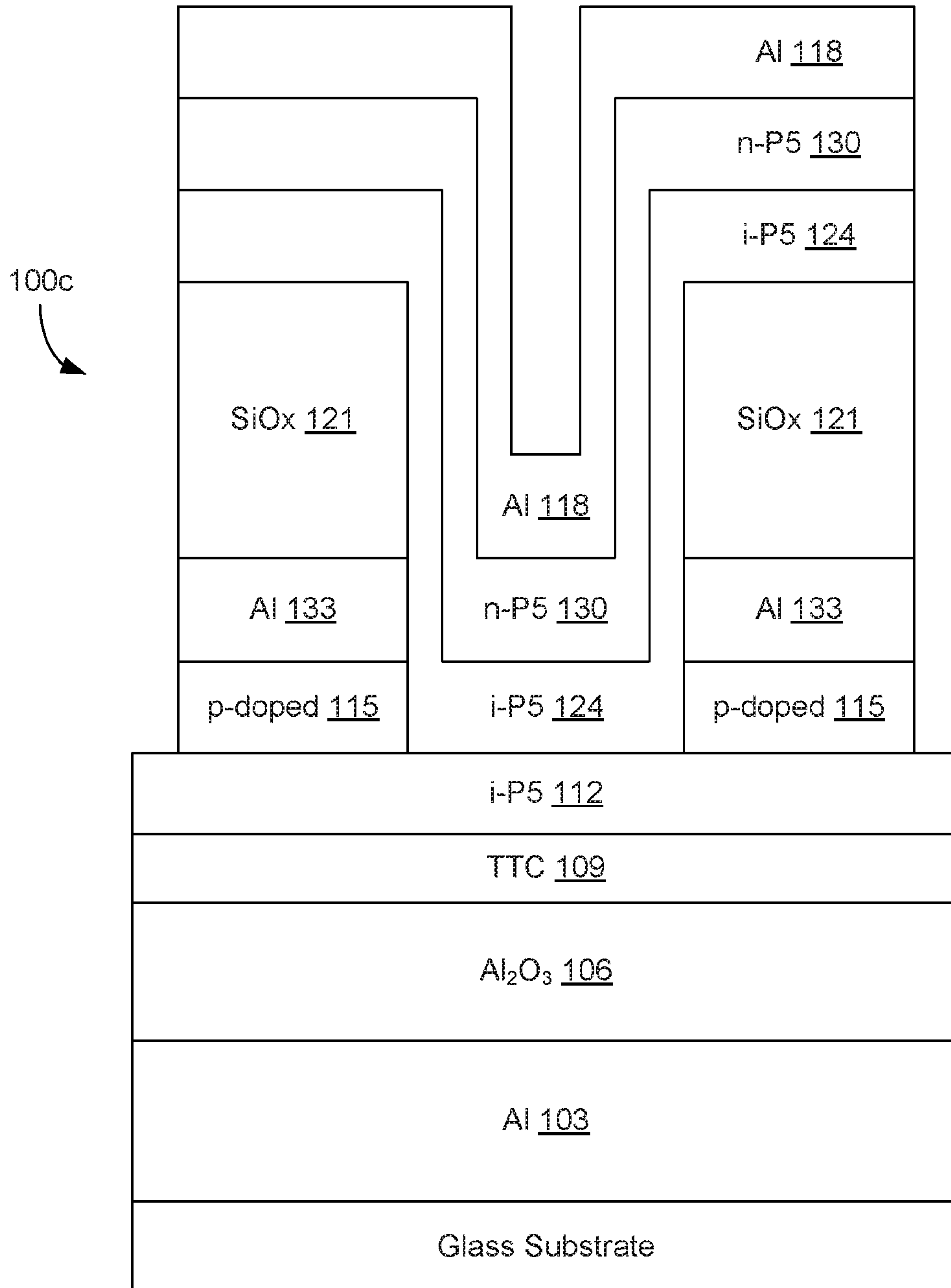

FIG. 6B

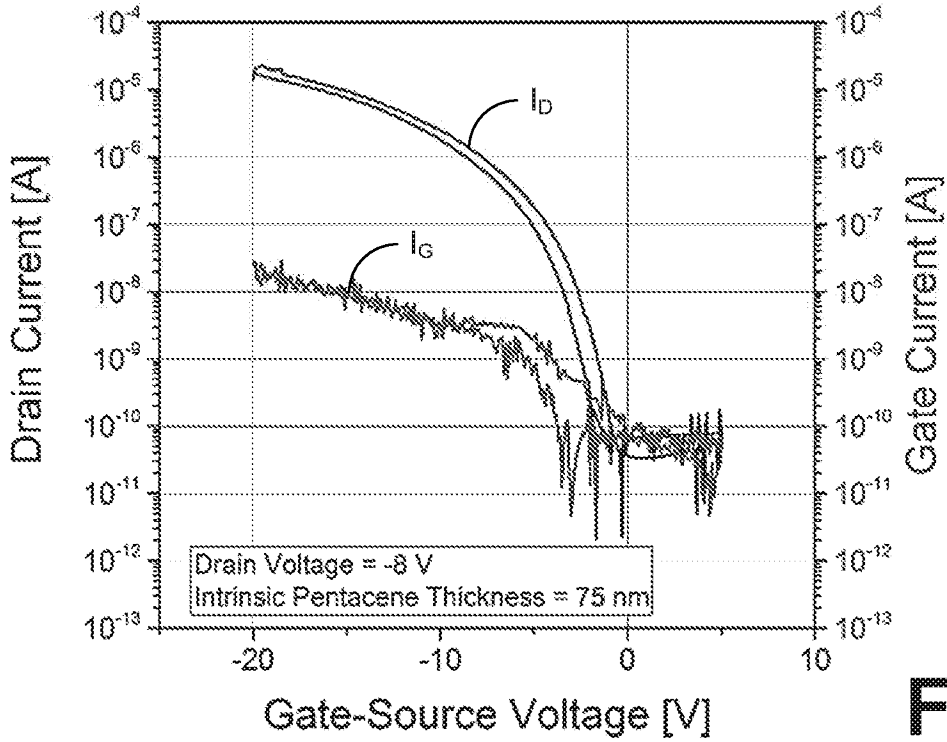

FIG. 7A

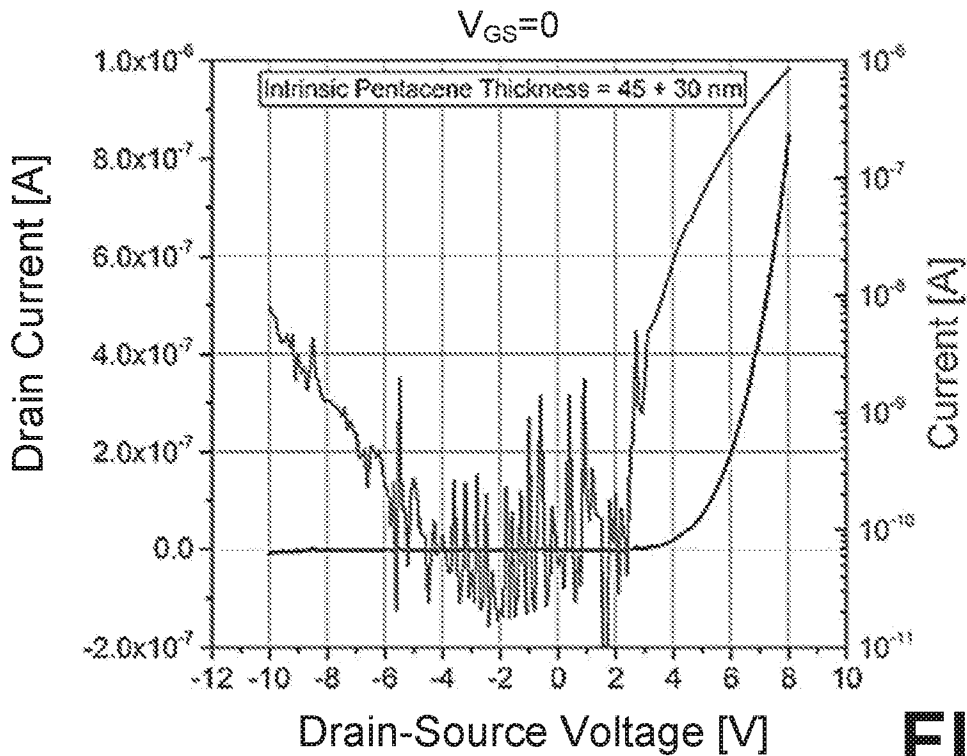

FIG. 7B

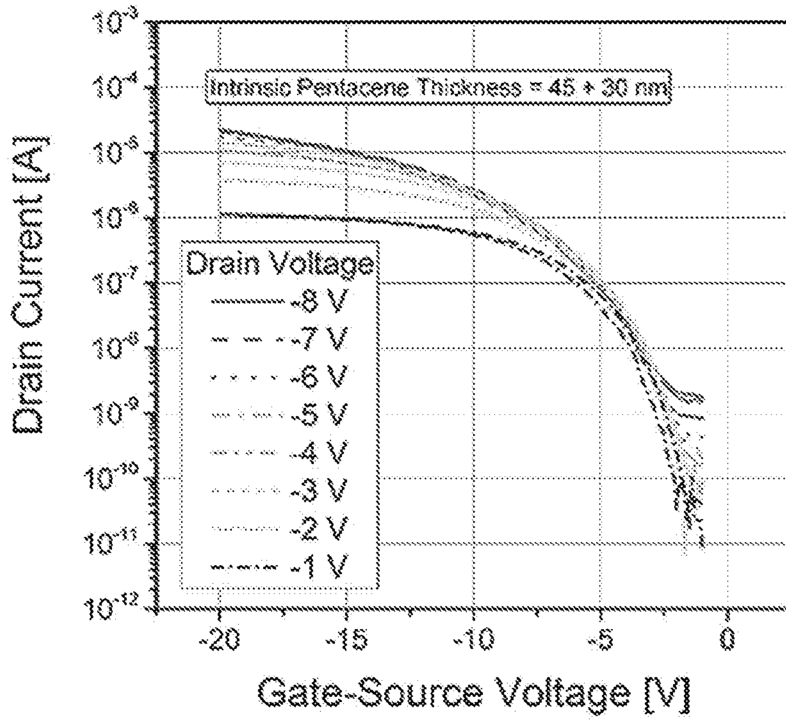

FIG. 8A

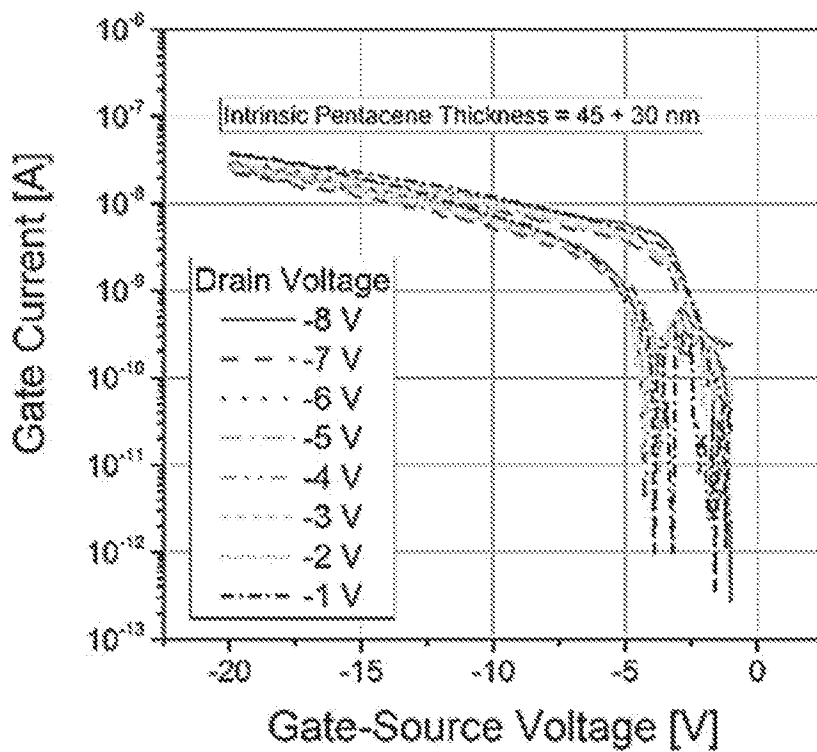

FIG. 8B

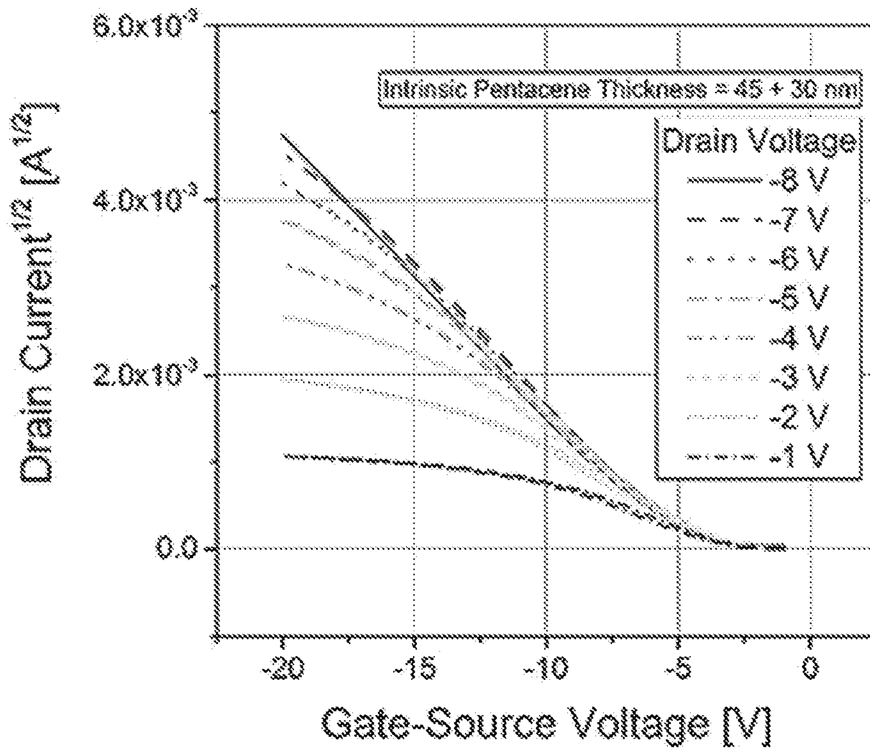

FIG. 8C

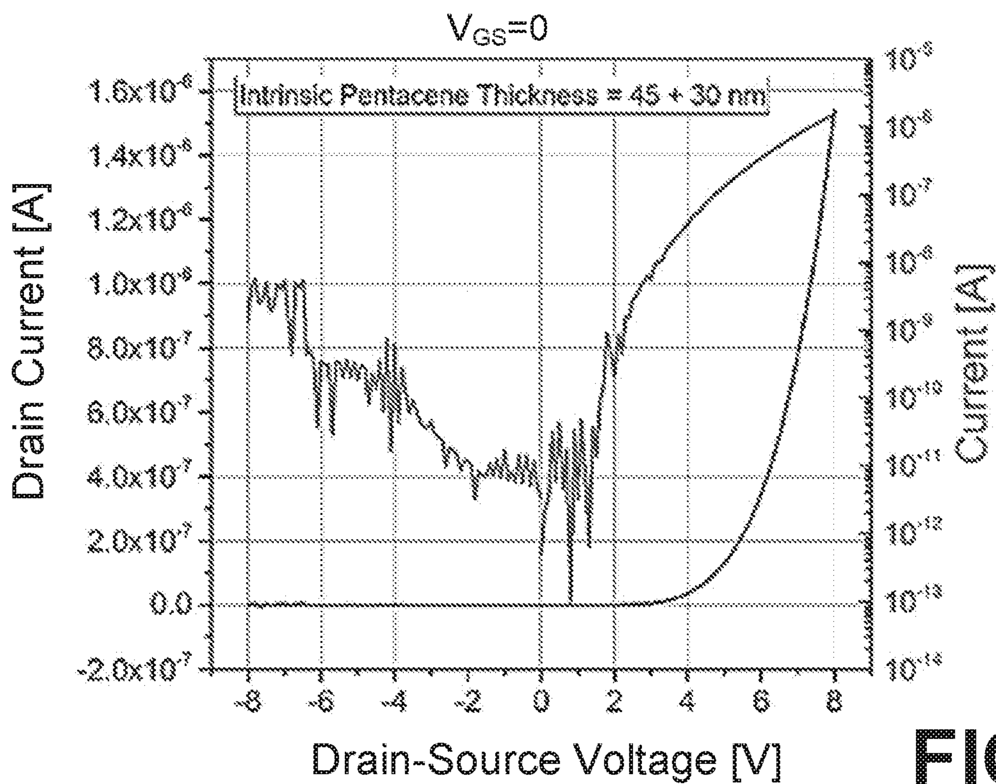

FIG. 8D

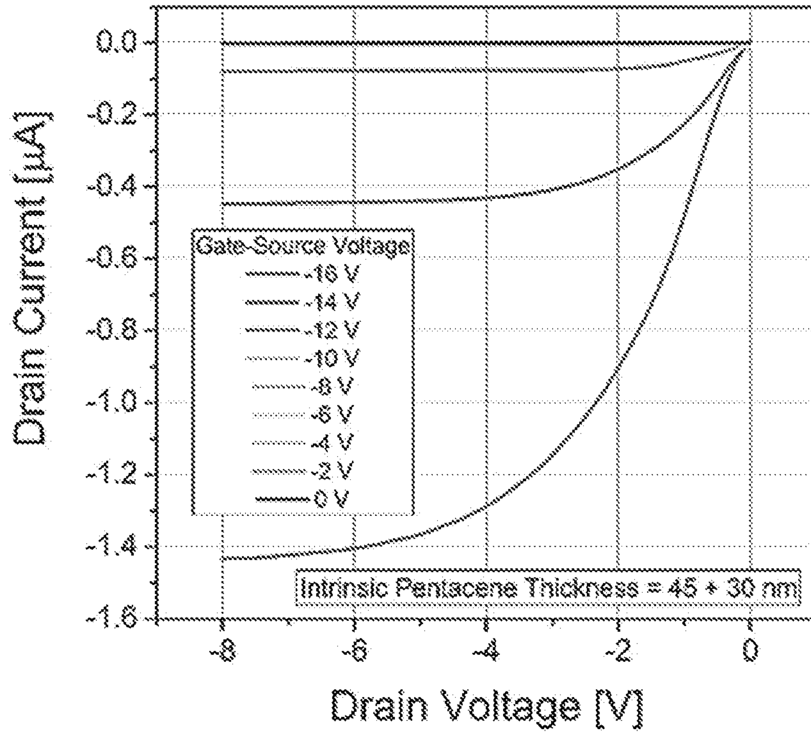

FIG. 8E

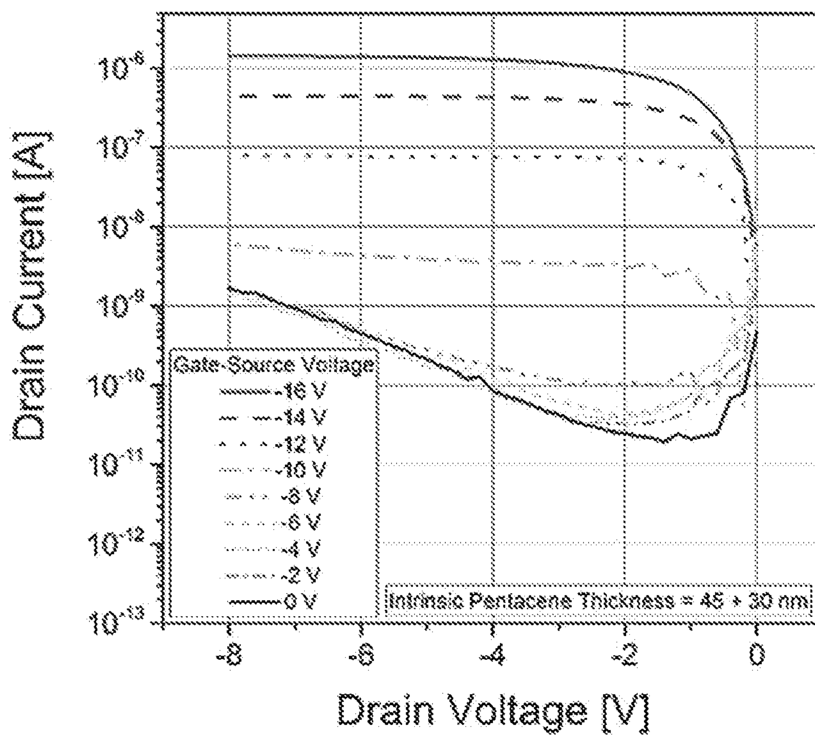

FIG. 8F

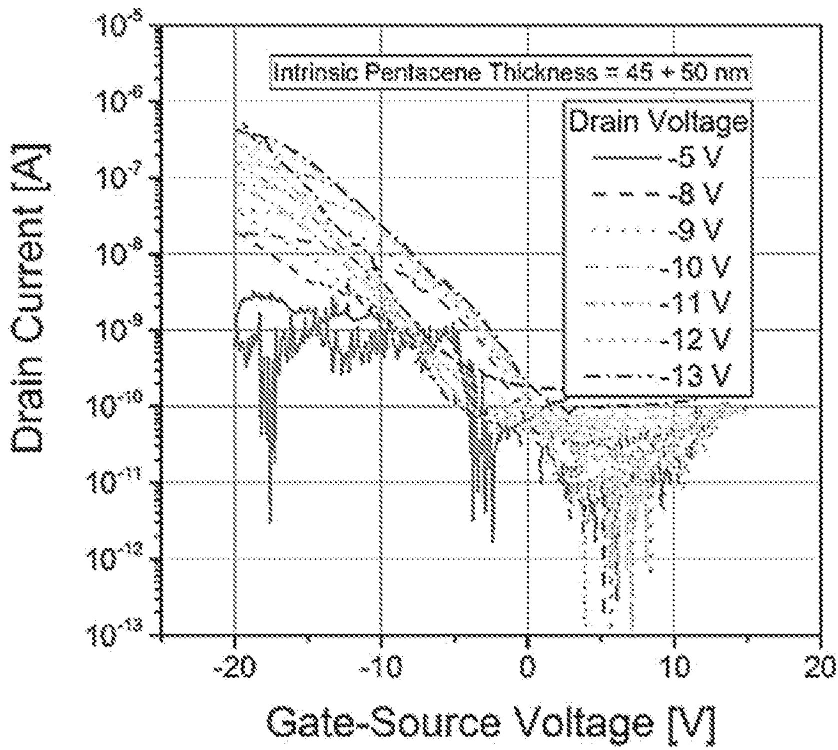

FIG. 9A

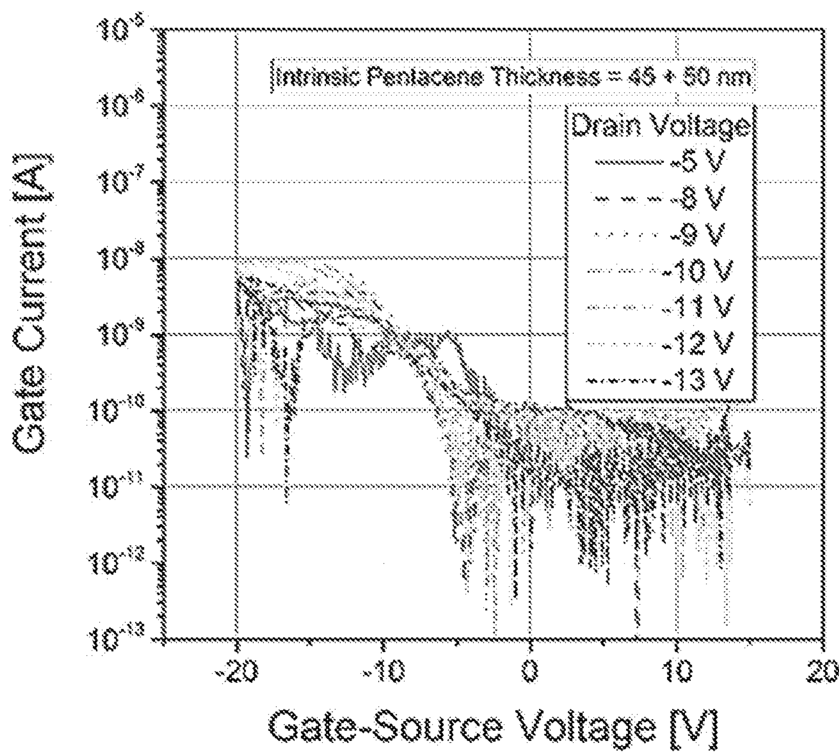

FIG. 9B

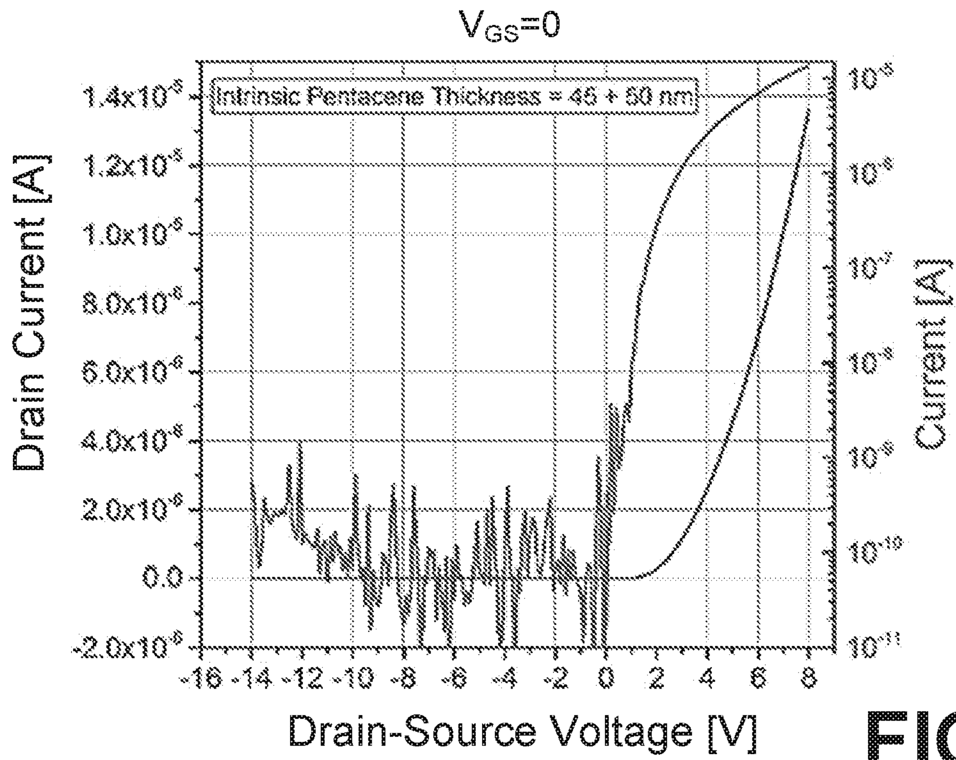

FIG. 9C

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2016/057897

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L51/05 H01L51/10
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 2 797 133 A1 (NOVALED GMBH [DE]; TECH UNIVERSITÄT DRESDEN [DE]) 29 October 2014 (2014-10-29) paragraphs [0042], [0057] - [0064]; figure 1 -----	1-25
A	EP 2 658 006 A1 (NOVALED AG [DE]; UNIV DRESDEN TECH [DE]) 30 October 2013 (2013-10-30) paragraphs [0006], [0039]; figure 2(b) -----	1-25
A	WO 2011/110664 A1 (CONSIGLIO NAZIONALE RICERCHE [IT]; MAIORANO VINCENZO [IT]; GIGLI GIUSE) 15 September 2011 (2011-09-15) page 15, line 2 -----	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 March 2017	17/03/2017

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Fratiloiu, Silvia

2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2016/057897

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