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Stretchable and foldable silicon-based electronics

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Flexible and stretchable semiconducting substrates provide the foundation for novel electronic applications. Usually, ultra-thin, flexible but often fragile substrates are used in such applications. Here, we describe flexible, stretchable, and foldable 500-μm-thick bulk mono-crystalline silicon (100) "islands" that are interconnected via extremely compliant 30-μm-thick connectors made of silicon. The thick mono-crystalline segments create a stand-alone silicon array that is capable of bending to a radius of 130 μm. The bending radius of the array does not depend on the overall substrate thickness because the ultra-flexible silicon connectors are patterned. We use fracture propagation to release the islands. Because they allow for three-dimensional monolithic stacking of integrated circuits or other electronics without any through-silicon vias, our mono-crystalline islands can be used as a "more-than-Moore" strategy and to develop wearable electronics that are sufficiently robust to be compatible with flip-chip bonding. *Published by AIP Publishing.*
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Flexible, stretchable, and foldable electronics especially intended for wearable devices extend the computational functionality into clothing and everyday activities. Wearable electronic systems require both robustness and flexibility. Because of their mechanical properties, polymeric materials seem a logical choice to meet these requirements. However, state-of-the-art organic semiconductors based on polymeric substrates have lower mobility than semiconductors based on conventional substrates do, such as silicon (circa 10 *vs.* 100 $cm^2 V^{-1} s^{-1}$).[1] Moreover, thermally unstable polymeric substrates are often not fully compatible with complementary metal-oxide semiconductor (CMOS) technologies and thus have not attracted interest in the semiconductor industry.

Ninety percent of today's electronics are based on bulk mono-crystalline silicon (100) due to its wide availability and suitable semiconducting, mechanical, and thermal properties, as well as its manufacturing compatibility with CMOS technologies. However, silicon is rigid and its use in flexible and stretchable electronics is restricted unless sophisticated engineering techniques are employed.[2–5] One strategy to make silicon flexible is to reduce its thickness to tens of microns. This volumetric reduction constricts the internal strain of the substrate to the elastic region of silicon. Rojas *et al.* demonstrated a fully CMOS-compatible technology through volumetric reduction by detaching the top 5 μm of silicon from the rest of the bulk substrate with xenon difluoride (XeF_2) and then recycling the remaining wafer.[3] Lee *et al.* used expensive silicon-on-insulator wafers (SOI) that are protected by a pre-stressed polymeric substrate after fabrication.[5] Subsequently, the wafer is submerged in a hydrofluoric (HF) acid solution to dissolve the buried oxide (BOX) layer. In this setup, the device layer remains on the auxiliary substrate and is then transferred to other substrates. This method isolates each discrete device, thus limiting its viability.

Simply thinning the substrate compromises mechanical integrity. Indeed, unprotected flexible silicon substrates are extremely fragile. The large area-to-thickness ratio in such a substrate makes the flexible silicon layer extremely vulnerable to damage during handling, which is why most flexing strategies rely on first building the device and then making it flexible. To circumvent the fragility of Si, we fabricated islands of silicon arrays that are bridged by thin interconnects, making the overall architecture flexible, stretchable, and foldable without compromising its mechanical integrity. In our process, the bending radius of the silicon substrate is independent of the thickness of the device layer.

To fabricate the substrate, we oxidized a 100-mm silicon wafer at a high temperature to obtain a 500-nm-thick silicon oxide (SiO_2) film. We used the atomic layer deposition (ALD) process to deposit 40 nm of alumina (Al_2O_3) as a hard mask onto the SiO_2 film. We used the standard photolithographic processes to create islands and springs. Subsequently, we used the reactive ion etching (RIE) to etch 30 μm thick springs. First, we coated the substrate with 40 nm of Al_2O_3 by ALD for sidewall coverage and then used RIE for directional etching. We then released the springs with XeF_2-based isotropic etching. We back-engraved lines with a 1065 nm

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Ytterbium (Yb) fibre laser along the {110} crystallographic planes to promote fracture initiation and propagation between the islands. We then carefully cleaved the silicon substrates to release the islands. A 3D schematic of the process is presented in Fig. 1, and a 2D cross-section of the flow can be found in Fig. S1 in the supplementary material. To demonstrate the effectiveness of the process, we also integrated the array with micro-light-emitting diodes (μLEDs). We electrically interconnected the islands by sputtering 50 nm of Ti and 100 nm of Au. We used a conductive resin to adhere the LEDs to the Au. The wafer was exposed to vapour HF to remove the silicon dioxide for the in-plane and out-of-plane deformation tests.

This segmentation approach divides the monocrystalline silicon wafer into islands and interconnects that are flexible and stretchable. The silicon islands retain their original thickness, whereas the interconnects are etched with a 2-μm-wide flexible and stretchable pattern. The thickness of the islands provides mechanical support, whereas the thickness of the bridging connectors provides flexibility. To craft this architecture, we selectively fissured the bulk silicon into arrays of islands while leaving the thin bridging silicon undamaged. Thus, the suspended bridges interconnecting the Si islands remained unaffected if fractures between the islands were properly aligned. Fractures in single crystals tend to propagate along favored crystallographic planes.[6] We oriented the silicon arrays along the {110} plane and designed the connectors to withstand the cleaving procedure.

Our strategy required a design of flexible and stretchable springs that would not tangle or self-intersect and that did not have vulnerable components. Previously, we showed that interconnects with spiral shapes can expand over 1300%.[4] However, the distention of spiralled interconnects can lead to self-intersection, and such interconnects may also tangle when bent. We did not use von Koch, Peano, Hilbert, or Moore spring patterns because they blindly follow a fractal pattern without distributing stresses to maximize expandability or flexibility.[7] Rather, we mimicked nature and used chaotic polymeric spherulite and lamellar packing as inspiration

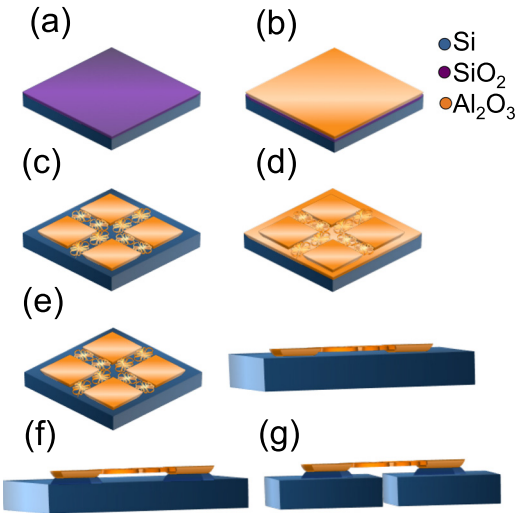

FIG. 1. Processing of the Si wafer. (a) Oxidized wafer, (b) alumina coating over the oxide, (c) photolithography patterning, (d) side and top ALD alumina coating, (e) RIE directional etching, isometric view and side view, (f) isometrical XeF_2 etched wafer, and (g) cleaved substrate.

for our spring design. We reasoned that lamellae would maximize the arc length of the silicon thread in relation to the spring's length, while the repeating pattern of spherulites would spread the lamellae when they were deformed laterally or out-of-plane. We also required that the ratio of the curve to the spring width was 50:1.[4] Thus, the spring not only bent but also twisted, which in turn increased its flexibility. We used the finite element simulations in COMSOL to computationally validate the spring design.

The yield stress of crystalline silicon has been reported to be 7 GPa with a maximum bending strain of 1%.[7] Fabrication processes can introduce imperfections to and additional strains on the crystal. To determine the stretchability of the spring designs, we set the benchmarking von Misses stress to 4 GPa. Fig. 2 shows the final spring architecture (black) and the simulation results including the computed strain. To validate the design, we superimposed the deformation model on a fabricated spring in Fig. S2 in the supplementary material. In that figure, the congruency between the model and the fabricated spring is readily visible. We conducted a subsequent simulation to visualize the folding mechanics of the spring. The ends of the spring were forced to meet as depicted at the top-left corner of Fig. 2. A maximum stress of 0.46 GPa corresponding to a strain of 0.136% was obtained for the fully folded spring at an internal radius of 120 μm.

As observed in Fig. 2, the traditional concept of the "bending radius" is not compatible with our spring-flexing approach. Locally, the spring segments are subject to the traditional bending radius constraint as given by

$$\varepsilon_{\max} = \frac{t}{2R}, \tag{1}$$

where ε_{max}, t, and R are the maximum strain, silicon thickness, and bending radius, respectively. The strains from our spring were lower than the strain predicted by (1). In a typical bending radius, the material should curve continuously in a given plane perpendicular to the bending axis. However, the overall bending radius of our spring is discontinuous, in a given plane of bending because the segments of spring, which are out-of-plane, are twisting. The projection of the whole silicon spring over the plane defined by the bending axis was also shorter than its arc length, as illustrated in Sketch S1 in the supplementary material. In other words, the disparity between the spring's arc length and its linear length (the distance between the anchoring points) decreased the internal strain by spreading the strain across the whole length of the spring. This geometrical advantage tighter bending angles for the interconnects and thus smaller overall bending radii. We define the geometrical advantage factor, G, as the ratio of the arc length to the linear length of the spring. Our spherulite-lamellar design has a geometrical advantage factor of G = 13.64. The overall spring bending radius (R) is derived from the radius of the curve (R_c) as follows:

$$G = \frac{L_C}{L} = \frac{2\pi R_C}{2\pi R} = \frac{R_C}{R} \quad \therefore R_C = G \times R. \tag{2}$$

By inserting R_C into (1), we obtain

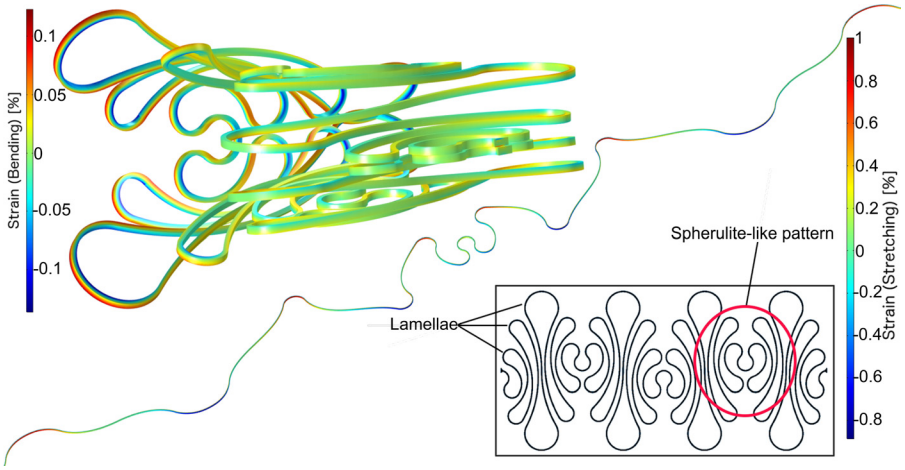

FIG. 2. COMSOL lamellar-spherulite spring design simulation of folding (top-left), stretching (diagonal), and unstrained (lower-right). The strain is given in percentage according to the color bars.

$$\varepsilon_{\max} = \frac{t}{2R_C} = \frac{t}{2G \times R} \quad \therefore R = \frac{t}{2G \times \varepsilon_{\max}}. \tag{3}$$

To demonstrate the validity of this equation, we bent a silicon bar of equal linear length using the same simulation parameters. The strain of the simulated spherulite-lamellar spring was 13.23 times smaller than that of the simulated silicon bar. We found that this strain difference was close to the predicted G value even though the bending strain formula did not account for anisotropy. The experimental proof of the concept is presented in Fig. 3.

In the SEM micrographs presented in Figs. 3(a) and 3(b), islands are folded and pressed against each other, exhibiting upward and downward folding, respectively. There is no space between contiguous islands that are pressed together. This is feasible because the spring lamellae can slide, twist, and contort within the 50-μm cavity created by the patterning of the springs. The bending radius of the spring cannot be the same as the bending radius of the full substrate. Additionally, their bending axes must not coincide. We thus measure the "effective bending radius" by fitting a circular path. When there is upward and downward folding, the effective bending radius alternates between the bending radius of the cavity and the bending radius of the substrate's thickness. Although the bending radius can be anisotropic, creating a design for the largest possible bending radius makes sense. The effective bending radius is thus the substrate's thickness. The effective bending radius of most silicon substrates is less than 1 mm, which is feasible in most foldable electronic applications. To calculate the effective bending radius when bending islands are in the same direction, we need to measure an enclosed area. The enclosed area is independent of the substrate thickness but relies on the area of the islands. Arguably, the simplest enclosed area to measure is an equilateral triangle formed by islands of length L. The circle contained within an equilateral triangle would have an effective radius ($R_{effective}$) of

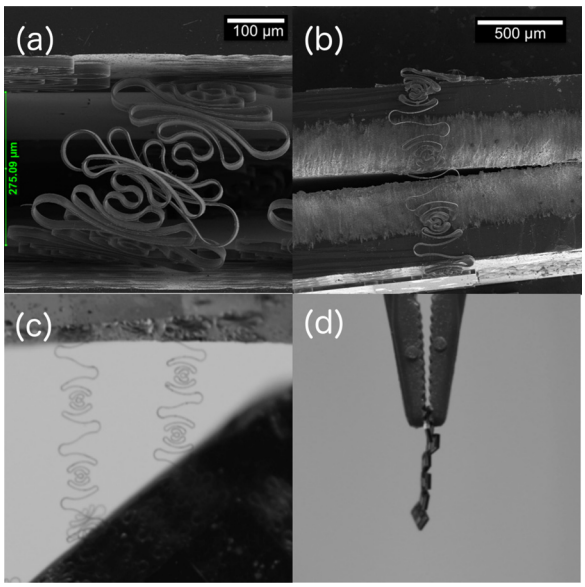

FIG. 3. Scanning electron microscopy micrographs. (a) Islands folded upwards so that the device layers face each other; (b) islands folded downwards so that the unpolished side of the substrates faces each other. Photographs of islands hanging vertically interconnected. (c) Deformed springs between two islands holding over five times the weight of a single island. (d) Array of five islands held vertically.

$$R_{effective} = \frac{L}{2} \times \tan(30^\circ) = \frac{L}{2\sqrt{3}} \approx 0.29 \times L. \tag{4}$$

A 3-mm bending radius suffices for most wearable electronic applications on the human body. Square islands with a maximum length of 1 cm can suffice for most electronic applications including Radio-Frequency Identification (RFID) tags, microprocessors, and energy storage, while still exhibiting an effective bending radius under 3 mm.

To show the effectiveness of our flexing strategy, we designed islands to have an active area of 2.1 mm by 0.85 mm. Springs with an arm width of 2 μm stretched linearly to over 490% of the original length as observed in Fig. S3 in the supplementary material, corresponding to a 24-fold spring area gain and an area gain of the island array of 5.6. Careful cleavage alignment was crucial to obtaining free-standing islands, especially since the spring length was less than 1 mm. The springs possess a remarkable mechanical integrity such that, unlike other flexible approaches, the springs could be spin coated with photoresist, cleaned with organic solvents, and blow-dried with a N_2 gun. Notably, a single spring could sustain the weight of more than one 500-μm island without the aid of any supporting substrate, as shown in Figs. 3(c) and 3(d). Also, a preferred bending direction could be predefined by introducing stress layers over the

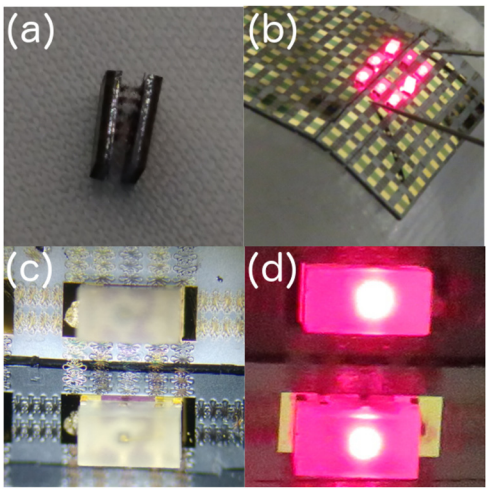

FIG. 4. Flexible Si platform. (a) Vertical freestanding islands with pre-stressed springs. (b) Flexible array with flip-chip bonded LEDs over a surface with a bending diameter of 2.5 cm. Springs interconnecting angled platforms with LEDs (c) OFF and (d) ON.

spring. The in-built strain was enough to maintain freestanding islands in a vertical position as shown in Fig. 4(a). Moreover, by tuning the dimensions of the springs, we could achieve directional stiffness by adjusting the stiffness for the out-of-plane bending and the in-plane stretching by making the springs thicker or wider, respectively. After we characterized the silicon platform, we bonded a LED array with a flip-chip process using a conductive epoxy as the binder over the islands. The array was then placed over a curvature with an approximately 1-cm bending radius, and then the LED array was lit as shown in Fig. 4(b). We used double springs in each connection to reduce the probability of electrical or mechanical malfunction.

The patterning and folding processes in our flexing strategy are compatible with CMOS technologies. It is also possible to pre-pattern the silicon substrate prior to device fabrication and mechanically cleave it in the last step, thus avoiding additional layers or chemicals, which could interfere with device performance. Our strategy could easily be used in the processing of wearable electronics and for the production of extendable, foldable, and reconfigurable applications. A possible application with immediate benefit would be silicon-based solar cells. The rigidity of solar cells normally limits their size in wearable and mobile applications. Our approach has the potential to transform rigid solar cells into body-conforming cells. Moreover, since the device layer resists typical handling pressures, it would be possible to fold tactile display islands like Origami. The portability of displays and devices would be improved through such folding. Electronic components, such as memory and power supply, could even be selectively detached to create destructible electronics.

In summary, a CMOS-compatible integral strategy for stretching and folding thick silicon is described here. We decouple the effective bending radius of the substrate from the device layer thickness. We can then tune the effective bending radius for most wearable applications. We used the finite element analysis to validate the spring design and then we demonstrated experimentally that the spring expands to 490%, which translates to a 5.6-fold gain in area for this particular flexible device assembly. More importantly, the spring design allows the islands to fold elastically on top of one another, which makes our approach a promising replacement for silicon vias. Our monocrystalline silicon platform, unlike other flexing strategies, is sufficiently robust to be compatible with flip-chip bonding. Given the mechanical stability of the islands and interconnectors, this strategy has the advantage that the springs can be patterned before or after device fabrication. Mechanical cleavage adds no trace impurities or additional layers to the fabricated devices. Consequently, no further design considerations are required. Our approach with islands and springs has the potential to be used in applications in compliant electronics.

See supplementary material for a 2D illustration of the fabrication process, a comparison of the spring deformation model and the fabricated spring, and the maximum-recorded spring deformation.

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[1]A. Salleo, Nat. Mater. **14**(11), 1077 (2015).
[2]K. Huang, R. Dinyari, G. Lanzara, J. Y. Kim, J. Feng, C. Vancura, F. K. Chang, and P. Peumans, in *IEEE IEDM* (2007), p. 217.
[3]J. P. Rojas, G. Torres Sevilla, M. Ghoneim, S. Inayat, S. Ahmed, A. Hussain, and M. M. Hussain, ACS Nano **8**(2), 1468 (2014).
[4]J. P. Rojas, A. Arevalo, I. G. Foulds, and M. M. Hussain, Appl. Phys. Lett. **105**(15), 154101 (2014).
[5]K. J. Lee, M. J. Motala, M. A. Meitl, W. R. Childs, E. Menard, A. K. Shim, J. A. Rogers, and R. G. Nuzzo, Adv. Mater. **17**(19), 2332 (2005).
[6]K. E. Petersen, Proc. IEEE **70**(5), 420 (1982).
[7]J. A. Fan, W.-H. Yeo, Y. Su, Y. Hattori, W. Lee, S.-Y. Jung, Y. Zhang, Z. Liu, H. Cheng, L. Falgout, M. Bajema, T. Coleman, D. Gregoire, R. J. Larsen, Y. Huang, and J. A. Rogers, Nat. Commun. **5**, 3266 (2014).