Semiconductor-free non-volatile resistive switching memory devices based on metal nanogaps fabricated on flexible substrates via adhesion lithography

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***Abstract*— Electronic memory cells are of critical importance in modern-day computing devices, including emerging technology sectors such as large-area printed electronics. One technology that has being receiving significant interest in recent years is resistive switching primarily due to its low-dimensionality and non-volatility. Here, we describe the development of resistive switching memory device arrays based on empty aluminium nanogap electrodes. By employing adhesion-lithography, a low-temperature and large-area compatible nanogap fabrication technique, dense arrays of memory devices are demonstrated on both rigid and flexible plastic substrates. As prepared devices exhibit non-volatile memory operation with stable endurance, resistance ratios >10^4 and retention times of several months. Intermittent analysis of the electrode microstructure reveals that controlled resistive switching is due to migration of metal from the electrodes into the nanogap under application of an external electric field. This alternative form of resistive random access memory is promising for use in emerging sectors such as large-area electronics as well as in electronics for harsh environments e.g. space, high/low temperature, magnetic influences, radiation, vibration, pressure.**

***Index Terms*— Flexible electronics, nanogap electrodes, non-volatile memory, resistive switching,**

I. Introduction

EXISTING electronic memory devices typically combine several advantages but also disadvantages. For example, considering memory based on complementary metal oxide semiconductor (CMOS) technology, dynamic random access memory (DRAM) has high capacity and high density but is volatile and must be refreshed every few seconds increasing power consumption, while static random access memory (SRAM) is fast but has low capacity and is also volatile. On the other hand, flash memory has high capacity and is non-volatile, but is characterised by relatively slow operating speed (writing/erasing) [1]. Thus there is a desire to develop new technologies that combine all the advantages of the existing technologies and perhaps offer even more. For example, the ability to demonstrate high-performance memory devices on large-area flexible substrates would be of interest for integration into emerging technologies such as flexible radio frequency identification (RFID) [2]. Amongst emerging technologies, including devices based on ferroelectrics [3], magnetoresistive materials [4], phase-change materials [5] and spin transfer torque memory [6], memristive devices are a prime candidate to fit these requirements. The latter are based on the phenomenon of resistive switching, the effect whereby a solid-state medium exhibits a reversible shift in its bulk resistance on the application of an externally applied electric current or field. The process is often non-volatile and generally observed with materials on the nanoscale, and thus is an interesting avenue of research for potential integration into future technologies.

Broadly speaking, resistive switching occurs by the successive application of electric stress. An initial forming step is required, after which the device enters a low resistance state (LRS). After the forming process, the device in a LRS is switched to a high-resistance state (HRS) by applying a threshold voltage (reset process). Switching back to the LRS (set process) is achieved by applying a threshold voltage that is different to the reset voltage. There is broad discussion on the origin of the switching mechanism, and it varies depending on the material system employed[7]. A popular model is the filament model [8]. In this model, the LRS arises from the formation of a conducting filament through the insulating matrix. Rupture of the filament gives rise to the HRS, but is a reversible process.

Resistive switching is observed in a variety of materials, the majority of research having been carried out on transition metal oxides (TMOs). The first work was carried out in 1960s when Hickmott noticed the effect in a series of binary oxide sandwich structures with different metal electrodes [9]. However, Si based technology took centre stage for several decades until a renewal of interest in the type of switching in the early 2000 was seen as Moore's law called for components on the nanoscale and owing to the advantage of the low power

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consumption of non-volatile devices. Breakthroughs were reported in 2000 by the groups of Ignatiev [10] and Bednorz [11] with reports of reversible and reproducible non-volatile change of the resistance state of two-terminal devices. Since then a range of TMO resistive switching devices have been reported [8] , as well as those based on organic polymer systems [12]–[15] and nanomaterials [16]–[18] to name but a few. In tandem with this progress, the emerging field of flexible electronics has evoked interest in new memory technologies compatible with flexible substrates over the past decade, and several investigations into flexible resistive switching devices have been made [19]–[25].

Traditional memristive devices are built in a vertical metal-insulator-metal structure. As visualisation and measurement of conductive pathways in these sandwich type structures has proven difficult, lateral device architectures have emerged in recent years as a tool for understanding filamentation [26]–[29]. Interestingly, empty lateral electrodes with separation on the nanoscale (nanogap electrodes) have also been shown to exhibit resistive switching behavior [30]–[44]. The concept of using empty nanogap electrodes as switching devices is potentially far more interesting than conventional structures, owing to the simplicity of the system from a fabrication point of view (no insulator/semiconductor material is required) and the possibility of increasing device density. The cause of switching is still debated, being attributed to either conductive filaments forming through the substrate [28], [30]–[33] or changes in the nanogap dimensions leading to different values of tunnel current [34]–[45] .

The apparent bottleneck to the broad adoption of this type of approach however is the difficulty of the fabrication of nanogap electrodes at high throughput and low cost. Nanogap electrode fabrication techniques are traditionally complex and suffer from poor scalability [46]. This has been largely true in the investigation of memristors based on nanogap electrodes, the fabrication techniques employed including electron beam lithography, electromigration and oblique angle evaporation (see **Table 1** for full details). Recently, Cui *et al.* [30] reported the use of atomic layer lithography, a scalable nanogap electrode fabrication technique reported on in recent years [47]–[49], to make arrays of Au nanogap electrodes exhibiting resistive switching effects. While promising, this remains a high temperature fabrication technique, requiring several thermal annealing steps with temperatures up to 500 °C, thus rendering it incompatible with flexible substrates. Furthermore, the choice of Au [34], [39] or Pt [35]–[38] electrodes, commonly used in these studies, may not be a cost effective choice for large scale adoption.

Here, we address these bottlenecks and fabricate, for the first time, nanogap resistive switching devices on flexible substrates. We achieve this by using adhesion lithography (a-Lith), a large-area and high throughput nanogap electrode patterning technique [50]. Despite its simplicity, a-Lith has proven suitable for the manufacturing of high speed nanoelectronic devices on arbitrary substrates including plastic at high yields [51], [52]. Building on this earlier work, we show that patterning of high aspect ratio aluminium (Al) electrodes in close proximity to each other (<10 nm) can lead to interesting resistive switching phenomena which can be exploited for the demonstration of non-volatile memory function. The work can be seen as the first step towards a new type of large-area flexible resistive random access memory (RRAM) technology.

II. Experimental

Initial tests were carried out on borosilicate glass substrates for ease of handling and initial proof of concept. The process of adhesion lithography for the formation of nanogap electrodes is introduced elsewhere [50] . In brief, Al electrodes (2 cm length × 3 mm width × 40 nm height) were patterned via conventional photolithography and wet chemical etching (**Fig. 1a**, step 1). The samples were then immersed in a 1 mMol solution of octadecylphosphonic acid (ODPA)/proan-2-ol (IPA) for 16 hours to allow the formation of a self-assembled monolayer (SAM) on the alumina (AlO_X) native to the Al surface, after which they were washed for 30 seconds in IPA and dried with N_2 (**Fig. 1a**, step 2). A ten minute anneal at 80 °C was employed to ensure complete removal of the solvent. The ODPA was macroscopically observed to attach to the patterned Al electrode only as when a drop of water was applied, this surface was incredibly hydrophobic, while the substrate remained hydrophilic. A global Al electrode was then deposited via thermal evaporation in high vacuum (10^{-6} mbar) (**Fig. 1a**, step 3). This electrode adheres well to the substrate where no ODPA is present, but poorly to the ODPA coated AlO_X/Al surface. On the application and removal of a glue (FirstContact), the poorly adhered Al-on-ODPA is removed, while the strongly adhered Al-on-substrate remains (**Fig. 1a**, step 4). Fracture occurs at the interfaces, and the result is a nanogap (L) typically on the order of <10 nm (**Fig. 1b**). The ODPA SAM was removed using a 10 minute UV-ozone treatment.

After this, a second photopatterning step is employed to achieve an array of nanogap electrodes with varying width (W) (**Fig. 1b**). The entire process was repeated on glass with an interlayer of bisbenzocyclobutene (BCB) (Cyclotene 4000, DOW Chemical Company), and on flexible polyimide substrates. Electrical characterisation was carried out using an B2902A Agilent semiconductor parameter analyser under a nitrogen atmosphere at room temperature. Scanning electron micrographs were taken using a LEO Gemini 1525 field emission scanning electron microscope with the operating voltage at 5 kV.

III. Forming Step

Initial current-voltage (I-V) measurements obtained from the as-developed Al-Al nanogap electrodes show no conductivity at moderate biases of ±12 V (**Fig. 2 (a)**). This is

an impressive demonstration of the applicability of a-Lith as a manufacturing process, as there are no shorts despite the channel width being as large as 5 mm resulting in an aspect ratio for the nanogap on the order of 10^6. At a higher applied bias of 16 V the device shows increased electrical conductivity (**Fig. 2 (b)**). However, switching between high and low resistance states is not observed immediately after this step. A further forming step is thus necessary for the nanogap electrode system to enter a resistive switching state. Understanding the nature of the switching is important in determining the best forming step to employ.

Naitoh *et al*. [53] , who in 2006 first reported resistive switching in empty metal nanogap systems, argued the switching behaviour is not due to the formation of conductive channels, but rather changes in the physical nanogap dimensions. At a low voltage (+3.5 V) field evaporation with electrostatic attraction or field-induced metal migration were said to be candidates for decrease in nanogap size. A competing repulsive force (either Joule heating or electromigration) was proposed to increase the gap size again. The differences in the HRS and LRS were then supposed to be due to tunneling current at different scales. To this end there is significant evidence that the reported nanogap switching behaviour is due to tunnelling current and a change in gap size, namely the temperature independence of the current, multilevel switching, [53] dependence of switching on the electrode material, [41] and independence of the switching behaviour on substrate material [54]. However, there is also significant evidence that switching can be due to a breakdown in the dielectric substrate (often SiO_2), such as an independence of switching on electrode material [33], evidence of damage to the substrate [55], and direct imaging of filamentation taking place [28].

With regards to resistive switching in oxide thin films, the forming step is necessary to create the first filaments through the oxide layer. In general a high bias is applied to the system with a compliance current set to prevent complete breakdown [56]. For nanogap electrodes on SiO_2, the forming voltage has been found to be 12 V for a 15 nm gap [28], 29 V for a 50 nm gap [33] and 1.6 V for 2 nm gaps [57]. These values would indicate a dielectric strength of SiO_2 in the range 6-8 MV cm^{-1}, a value on par with those reported in the literature [58]. This further implies a breakdown of a-Lith nanogaps, whose separation is on the order of 10 nm, to be on the order of $|10|$ V. However, the applied voltage may need to be higher than this value if there is some voltage drop in the system e.g. due to the presence of a native Al_2O_3 layer.

For nanogap dimension change, the forming step is required to decrease the size of the nanogap since its initial dimension is ~10 nm while tunnelling occurs at length scales <2 nm. This occurs due to migration or field evaporation of material into the gap which reportedly occurs at field strengths of 10 MV cm^{-1} [59] . This would correspond to an applied voltage of ~10 V and has been achieved in other cases where starting nanogap electrodes are on the same scale as those used here by applying a 10 V pulse [34], [53] or several sweeps between ±10 V [60]. Thus regardless of the mechanism, the forming step should be fairly similar.

Furthermore, the post-forming I-V characteristics are expected to look similar, with a roughly Ohmic current at low voltages and an apparent negative differential resistance (NDR) effect kicking in at somewhere in the 4-6 V range, followed by a flattening out of current. This voltage range tends to be the set voltage, while a higher (>10 V) value is used as the reset voltage. The only difference in the reported mechanisms is that for nanogap dimension change due to material migration switching, a sweep about the set voltage (e.g. +10 V → -1 V, [54] or +9 V → + 3 V [53]) is employed, whereas for oxide switching, a pulse at the set voltage suffices [28], [31], [33], [55], [57].

In activating switching behaviour in Al-Al nanogap electrodes fabricated via a-Lith, the use of a forming step based on high voltage sweeps was rarely successful. In some cases, the characteristic NDR effect was observed after dozens of sweeps at or above ±12 V. As an alternative, a fixed voltage was applied for up to 30 seconds while monitoring the current (**Fig. 3a**). It was found empirically that when the current levels reached 1 µA, the characteristic NDR peak was observed in I-V sweeps (see **Fig. 3b**). Voltage pulses of increasing current were applied until there was an observed change in current. Values of 14 –16 V were found to be sufficient to observe the desired increase in current. Nanogap electrode pairs of differing widths were investigated, from 2 µm up to 5 mm. A successful forming step was seen in devices with widths of 250 µm and above, though not for those of smaller widths. This is believed to be due to as of yet insufficient understanding and optimisation of the forming step, and there should be no physical reason why switching with much smaller device widths is not possible. The shall be further discussed in section V.

IV. Switching Characteristics

In some cases (< 5 %), the application of high bias (16 V) led to a visible destruction of the nanogap interface, thus no switching was observed. In all other cases resistive switching was observed.

Following successful activation the switching characteristics of the nanogap device were investigated. When the device was scanned from high to low voltage potential, it was found to be in a LRS, and remained in this state when voltages below ~3 V were applied. Current flow of about 20 µA was observed at a bias voltage of 2 V, and characteristics were independent of bias direction implying unipolar functionality. Applying higher bias voltages led to the device entering a HRS, where the low voltage current levels were below the detection limits of the measurement setup. It was possible, but not completely reliable, to set the devices (i.e. switch back to the LRS) by applying a voltage pulse in the range 3 – 8 V. A more reliable method was sweeping from high to low voltage, as reported

previously for nanogap switching.

To measure the endurance of the devices, a repeated waveform as shown in **Fig. 4** was applied to the devices. A 1 ms 12 V pulse was used as reset voltage and an 8 to 3 V sweep was used as a set voltage. The current was then measured between 0-2 V. **Fig. 5** shows I-V characteristics of a nanogap device in the HRS and LRS in this voltage range. The measured current levels in the LRS are at the detection limit of the setup, implying extracted resistances in the HRS are an underestimation of their true value. The device resistances were extracted at an arbitrary voltage of 0.2 V and are plotted in **Fig. 6**. Evidently, the nanogap devices exhibit good endurance over 100 cycles with a measured resistance ratio on the order of 10^4. While certain devices exhibit stable endurance over several hundred cycles, most show some degradation in performance after ~ 100 cycles, with device operation showing a greater tendency not to enter the LRS. Interestingly, stopping the scan and running several high voltage I-V sweeps can restore the high quality switching characteristics for a time, implying that with optimisation during the forming step and the set and resest voltage steps, a greater endurance could potentially be achieved. Finally, devices were left in the LRS and HRS and measured after several months showing no change in resistance levels, indicating an extremely good retention time.

V. Switching Mechanism

To examine the cause of the switching behaviour, SEM images of the devices were taken. For reference, **Fig. 1b** shows the SEM image of an Al-Al electrode nanogap before bias application (as-prepared). After the forming step has been performed, a definite alteration in the electrode conformation is observed. **Fig. 8** show representative SEM images of Al-Al nanogaps in the LRS **(a)** and HRS **(b)** states, respectively, immediately after forming. Clearly there has been severe alteration of the nanogap electrode geometry, especially when compared to the as-prepared device shown in **Fig. 1b**. In parts the gap has significantly widened, while in others the electrodes remain in close proximity to each other. Closer examination of several SEM micrographs, reveal the presence of small bridging points (a few nanometres across) along the nanogap electrodes in the LRS state (**Fig. 8a**), which cannot be observed in the electrodes in the HRS state (**Fig. 8b**). Such metal bridging of electrodes has been observed before, though previously given the presence of a solid electrolyte between the electrodes [61].

These electrical ‘bridges’ appear to be relatively sparse which may explain the fact that switching behaviour is mainly observed in nanogap electrodes with widths ≥250 μm. In smaller width nanogap electrodes the density of migrated Al clusters may be too random for reliable switching behaviour to be observed. However, as an exact mechanism for the formation of these bridges is not explored in this study, we posit that the realisation of smaller width and thus higher density nanogap memory devices should in principle be possible.

There is thus evidence to support the migration of Al into the gap during the forming step, with some points resulting in a breakdown of the electrodes in the vicinity due to heating, and some points approaching each other significantly so as to cause electrical switching. While this switching mechanism is supported by several SEM images, the proof is not definitive and further experimental work will be required to either support or refute the assumed mechanism. As there is much debate on the topic (see for example **Table 1**), filamentation due to fused Si through the glass substrate could not be ruled out at this stage.

One way to determine which switching mechanism is dominant is to change the substrate material and monitor the impact on the electrical characteristics of the nanogap and the microscopic changes in its geometry. To this end, Al nanogap electrodes were prepared on glass substrates with a BCB interlayer. This polymer interlayer should be ideal for quenching switching behaviour arising from SiO_2 filamentation. While resistive switching in polymers has been reported, this should not be possible in the case of BCB as it has been noted that it is crucial that the polymer be π-conjugated for switching to arise [62]. Switching is indeed observed on these BCB substrates, with identical characteristics to nanogap devices made on glass substrates.

As a final step, Al-Al nanogap electrodes on polyimide substrates (**Fig. 9**) were tested for switching behaviour and resultant characteristics mimic both those tested on glass and on BCB coated glass substrates. This gives a strong indication that the switching mechanism is due to the migration of material from the Al electrodes into the nanogap to form conductive filamentary pathways similar to those shown in **Fig. 9a**. This is a very interesting finding because, firstly, it demonstrates the compatibility of the nanogap memory technology with plastic substrates, and secondly it represents the first demonstration of a nanogap memristive device on a flexible substrate. Further test must be carried out on the effect of bending on these substrates, where it will be useful to have the device positioned in the substrate centre to directly determine the applied bending radius.

VI. Conclusion

We developed and studied co-planar metal nanogap resistive switching memory devices fabricated using adhesion lithography on arbitrary substrate materials including plastic. We demonstrated that the use of a-Lith enables large-area and low-temperature processing of large nanogap arrays with excellent resistive switching characteristics, the operation of which appears to be independent of the substrate material employed. Using aluminium as the electrode material has led to a further reduction in the cost and fabrication complexity of this rather interesting device concept. As-prepared nanogap devices exhibit robust conductivity switching with resistance

ratios of $>10^4$, excellent endurance and retention times in excess of several months. For successful device operation, an electroforming step based on the application of a 14 – 16 V bias for up to 30 seconds was found to be necessary. SEM imaging of the programmed nanogap devices and the independence of the electrical switching behaviour on the substrate material suggest formation of conductive channels due to Al migration into the nanogap as the cause of switching rather than filamentation through the substrate. An understanding of the specific switching mechanism, as well as the first demonstration of the devices on plastic substrates, is an important stride in the adoption of this interesting technology for non-volatile memory applications on large-area flexible substrates.

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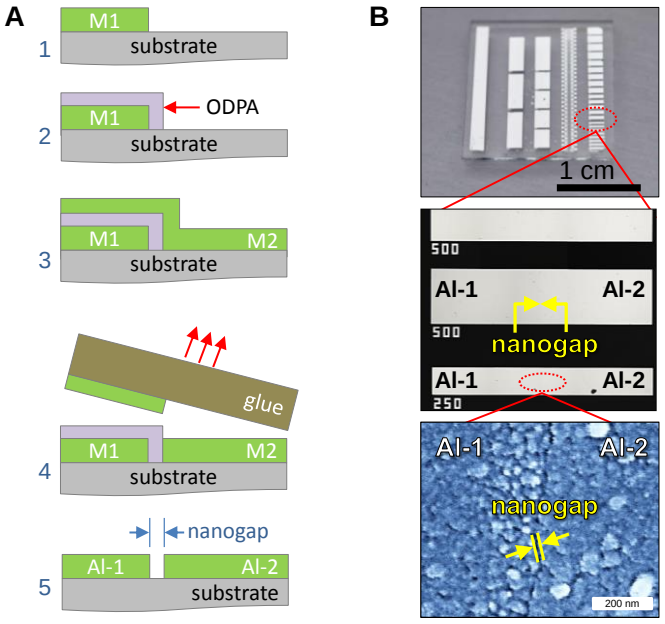

Fig. 1. (a) Schematics of the various pattering steps employed during a-Lith. (b) Aluminium nanogap (NG) electrodes (Al 1 and Al 2) fabricated via a-Lith on glass substrate with electrode widths ranging from 2 µm up to 5,000 µm. Micrograph images show the array with electrode widths of 250 µm and 500 µm. Scanning electron micrographs show the NG interface between Al 1 and Al 2. Determination of exact gap dimensions is difficult due to resolution limits but it appears to be <10 nm.

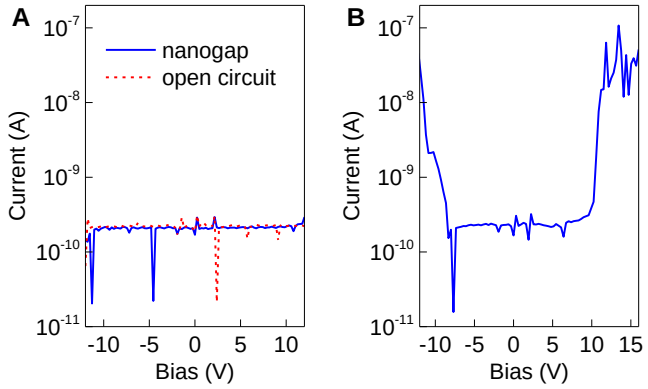

Fig. 2. I-V characteristics of empty nanogap electrodes prior to forming step showing (a) no conductivity up to 12 V applied bias (an open circuit measurement is shown here also for reference) (b) onset of some current flow with bias of 16 V but no switching behaviour is observed after the sweep. Small voltage spikes in both cases are due to system noise.

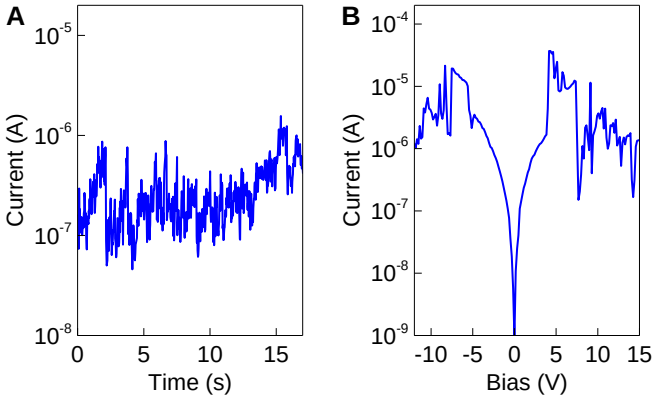

Fig. 3. (a) Forming step for the resistive switching behaviour. Current is plotted vs. time at an applied bias of 14 V. The bias application is stopped after the current exceeds 1 µA. (b) I-V characteristics of the nanogap electrodes after the forming process showing the expected NDR characteristics.

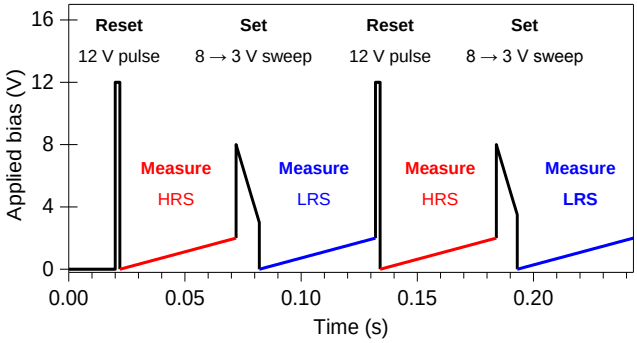

Fig. 4. Applied bias waveform used to evaluate the device endurance. The reset voltage (12 V pulse) applied for 1 ms puts the device into the HRS, after which the current is measured between 0 V and 2 V. The set voltage (8 – 3 V sweep) puts the device into the LRS, after which current is again measured in the range between 0 V and 2 V.

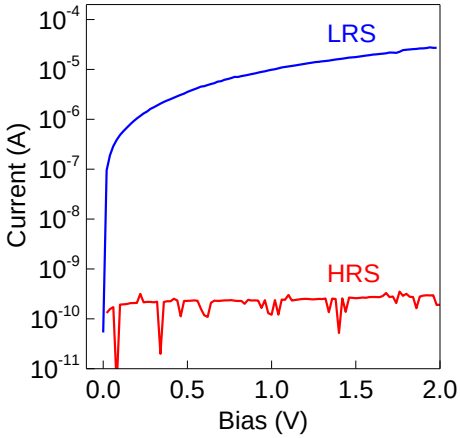

Fig. 5. I-V characteristics of nanogap electrodes in the HRS and LRS using the waveform in Fig. 4 to switch between states and measure. Currents of ~ 20 µA are observed at 2 V in the LRS. Measured current levels in the HRS are at the detection limit of the measurement setup, implying the real values are lower than those shown here.

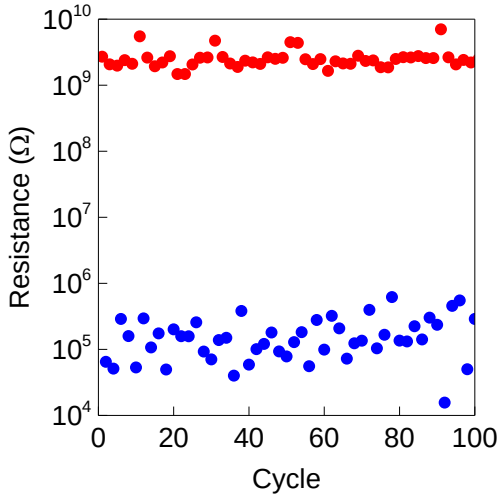

Fig. 6. Endurance of the nanogap electrode memristor over 100 cycles showing uniform repeatability and resistance ratios on the order of 10^4.

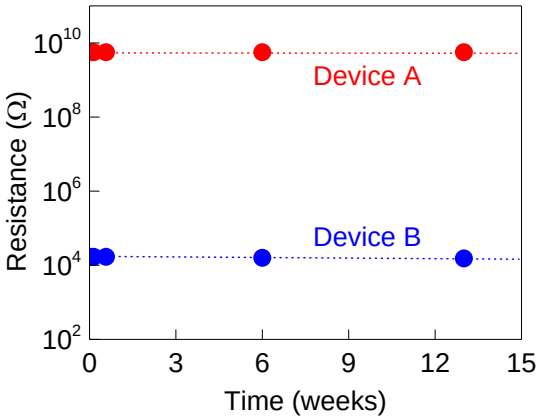

Fig. 7. Retention time for two devices, Device A and Device B held in the HRS and LRS respectively. Both devices show little change in resistance values measured at 2 V over the course of 13 weeks.

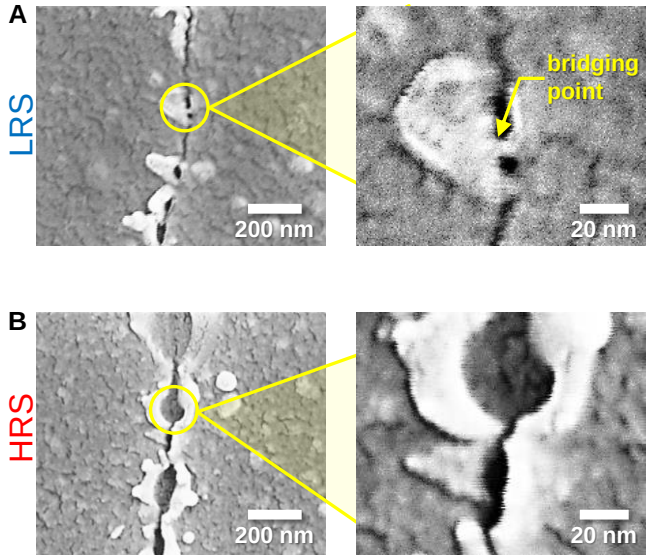

Fig. 8. SEM micrographs of an Al-Al electrode nanogap post forming in the (a) LRS (b) HRS. The higher magnification images reveal evidence of conductive bridges present for devices in the LRS which are absent in the magnified image of the device in the HRS. The images presented here are representative of several dozen images analysed in both the LRS and HRS.

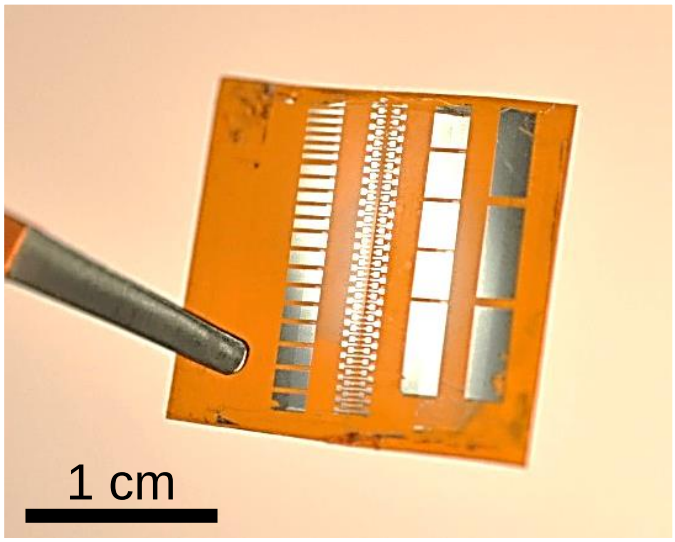

Fig. 9. Array of nanogap electrodes fabricated on flexible polyimide substrate with widths ranging from 2 μm up to 5,000 μm.

Table 1: Summary of nanogap switching characteristics of devices developed in this work compared to those reported in the literature.

Electrode type	Electrode fabrication route	Substrate type	Proposed switching mechanism	Endurance cycles	Resistance ratio	Retention time	Ref
Pt	Oblique angle deposition	Si/SiO_2	Electrode migration	35	10^5		[34]
Au	EBL + Electroless plating	Si/SiO_2	Electrode migration	10	10^2		[35]
Au	Oblique angle evaporation	Si/SiO_2	Electrode migration	200	10^6		[36] [37]
Pt	EBL + electromigration	Si/SiO_2	Electrode migration	50	10^6		[38]
Au	Oblique angle evaporation	Si/SiO_2	Electrode migration	11	$10^2 – 10^4$		[39]
Pt	EBL	Si/SiO_2	Electrode migration	5	10^2		[40]
Au Pd Pt Ta	Oblique angle evaporation	Si/SiO_2	Electrode migration				[41]
Si	Electromigration	Si/SiO_2	Electrode migration	100	10^4		[42]
Au	Lithographicall patterned nanowire electrodeposition + Electromigration	Si/SiO_2	Electrode migration				
Ni	EBL	Si/SiO_2	Electrode migration	100	10^3		[43], [44]
Pt	EBL + electromigration	Si/SiO_2	Electrode migration	100	10^4	8 hours (at high temp.)	[45]
Au	Atomic layer lithography	Si/SiO_2	Substrate effect	100	10^4	16 hours	[30]
Au	EBL + electromigration	SiO_2 TiO_2	Substrate effect				[31]
Au	EBL + Oblique angle deposition	Al_2O_3	Substrate effect		10^3		[32]
Amorphous carbon	Electromigration	Si/SiO_2	Substrate effect	100	10^5		[28], [33]
Al	**Adhesion lithography**	**Glass (SiO_2) BCB Polyimide**	**Electrode migration**	**100**	**10^4**	**3 months**	**This work**