Wide-Range Highly-Efficient Wireless Power Receivers for Implantable Biomedical Sensors

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ABSTRACT

“Wide-Range Highly-Efficient Wireless Power Receivers for Implantable Biomedical Sensors”

Mahmoud Hamdy Ouda

Wireless power transfer (WPT) is the key enabler for a myriad of applications, from low-power RFIDs, and wireless sensors, to wirelessly charged electric vehicles, and even massive power transmission from space solar cells. One of the major challenges in designing implantable biomedical devices is the size and lifetime of the battery. Thus, replacing the battery with a miniaturized wireless power receiver (WPRx) facilitates designing sustainable biomedical implants in smaller volumes for sentient medical applications.

In the first part of this dissertation, we propose a miniaturized, fully integrated, wirelessly powered implantable sensor with on-chip antenna, designed and implemented in a standard 0.18\(\mu\)m CMOS process. As a batteryless device, it can be implanted once inside the body with no need for further invasive surgeries to replace batteries. The proposed single-chip solution is designed for intraocular pressure monitoring (IOPM), and can serve as a sustainable platform for implantable devices or IoT nodes. A custom setup is developed to test the chip in a saline solution with electrical properties similar to those of the aqueous humor of the eye. The proposed chip, in this eye-like setup, is wirelessly charged to 1V from a 5W transmitter 3cm away from the chip.

In the second part, we propose a self-biased, differential rectifier with enhanced efficiency over an extended range of input power. A prototype is designed for the medical implant communication service (MICS) band at 433MHz. It demonstrates an efficiency improvement of more than 40% in the rectifier power conversion efficiency
(PCE) and a dynamic range extension of more than 50% relative to the conventional cross-coupled rectifier. A sensitivity of -15.2dBm input power for 1V output voltage and a peak PCE of 65% are achieved for a 50kΩ load. In the third part, we propose a wide-range, differential RF-to-DC power converter using an adaptive, self-biasing technique. The proposed architecture doubles the dynamic range of conventional rectifiers. Unlike the continuously self-biased rectifier proposed in the second part, this adaptive rectifier extends the dynamic range while maintaining both the high PCE peak and the sensitivity advantage of the conventional cross-coupled scheme, and can operates in the GHz range.
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TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Examination Committee Approval</td>
<td>2</td>
</tr>
<tr>
<td>Table of Contents</td>
<td>7</td>
</tr>
<tr>
<td>List of Abbreviations</td>
<td>10</td>
</tr>
<tr>
<td>List of Figures</td>
<td>11</td>
</tr>
<tr>
<td>List of Tables</td>
<td>14</td>
</tr>
<tr>
<td><strong>1 Introduction</strong></td>
<td>15</td>
</tr>
<tr>
<td>1.1 Biomedical Implantable Devices</td>
<td>16</td>
</tr>
<tr>
<td>1.2 Wireless Powering Link</td>
<td>18</td>
</tr>
<tr>
<td>1.3 Thesis Contributions</td>
<td>19</td>
</tr>
<tr>
<td>1.4 Thesis Outline</td>
<td>19</td>
</tr>
<tr>
<td><strong>2 Background and significance</strong></td>
<td>22</td>
</tr>
<tr>
<td>2.1 WPT system overview</td>
<td>22</td>
</tr>
<tr>
<td>2.1.1 Wireless power transfer methods</td>
<td>23</td>
</tr>
<tr>
<td>Near-field reactive coupling</td>
<td>24</td>
</tr>
<tr>
<td>Far-field electromagnetic radiation</td>
<td>25</td>
</tr>
<tr>
<td>2.2 Wireless power receivers</td>
<td>27</td>
</tr>
<tr>
<td>2.2.1 WPRx Specifications</td>
<td>28</td>
</tr>
<tr>
<td>Sensitivity ($P_{RF_{min}}$)</td>
<td>28</td>
</tr>
<tr>
<td>Efficiency ($\eta = P_{DC}/P_{RF}$)</td>
<td>29</td>
</tr>
<tr>
<td>Input impedance</td>
<td>29</td>
</tr>
<tr>
<td>Output DC voltage</td>
<td>30</td>
</tr>
<tr>
<td>Output DC current (loading)</td>
<td>30</td>
</tr>
<tr>
<td>2.2.2 WPRx design challenges</td>
<td>30</td>
</tr>
<tr>
<td>On-chip antenna</td>
<td>30</td>
</tr>
<tr>
<td>RF Matching</td>
<td>31</td>
</tr>
<tr>
<td>RF Rectifier</td>
<td>31</td>
</tr>
<tr>
<td>DC Voltage regulations</td>
<td>31</td>
</tr>
<tr>
<td>2.2.3 WPRx Design Tools</td>
<td>32</td>
</tr>
<tr>
<td>Stage Architecture</td>
<td>32</td>
</tr>
<tr>
<td>Number of stages</td>
<td>32</td>
</tr>
<tr>
<td>Circuits design parameters</td>
<td>32</td>
</tr>
<tr>
<td>Antenna resistance ($R_A$)</td>
<td>33</td>
</tr>
<tr>
<td>2.3 Literature review and rectifier topologies</td>
<td>33</td>
</tr>
</tbody>
</table>
3 5.2 GHz On-chip RF Power Harvesting Module

3.1 System Level Design
3.1.1 System Operation
3.1.2 Design consideration
  Frequency selection
  Technology Selection
  Link Budget Calculations
3.2 Antenna Design
3.3 Circuits Design
  3.3.1 RF to DC Voltage Rectifier
  3.3.2 DC Voltage Limiter
  3.3.3 Low Dropout (LDO) Voltage Regulator
  3.3.4 Voltage Sensors
3.4 Experimental Results
  3.4.1 Test Setup to Emulate Eye Environment
  3.4.2 DC Measurements
  3.4.3 RF Measurements

4 Self-Biased Differential Rectifier with Enhanced Dynamic Range

4.1 Introduction
4.2 RF-to-DC power converters
4.3 Proposed RF-to-DC Power Converter
  4.3.1 Proposed Architecture
  4.3.2 Operational Concept
4.4 Prototyping and Measurements
  4.4.1 Measurement methodology
  4.4.2 Measurement Steps
    Probe calibration :
    Measuring the input S-parameter and output DC voltage
    Deducing the power conversion efficiency
4.5 Results and Discussion (Data analysis)
4.6 Conclusion

5 Wide-Range Adaptive RF-to-DC Power Converter for UHF RFIDs

5.1 Introduction
5.2 Self-Adaptive Rectifier
5.3 Experimental Results
5.4 Conclusion

6 Conclusion & Future Work
6.1 Future Directions

References
# LIST OF ABBREVIATIONS

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>Complimentary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>EIRP</td>
<td>Effective Isotropically Radiated Power</td>
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<tr>
<td>EM</td>
<td>Electromagnetic</td>
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<tr>
<td>EPC</td>
<td>Electronic Product Code</td>
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<tr>
<td>ER</td>
<td>External Reader</td>
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<tr>
<td>FIB</td>
<td>Focus Ion Beam</td>
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<tr>
<td>GHz</td>
<td>Giga Hertz</td>
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<tr>
<td>IOPM</td>
<td>Intraocular Pressure Monitoring</td>
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<tr>
<td>IoT</td>
<td>Internet of Things</td>
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<tr>
<td>LDO</td>
<td>Low Dropout Voltage Regulator</td>
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<tr>
<td>MCU</td>
<td>Micro-Controller Unit</td>
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<tr>
<td>MICS</td>
<td>Medical Implant Communication Service</td>
</tr>
<tr>
<td>MIMCAP</td>
<td>Metal-Insulator-Metal Capacitor</td>
</tr>
<tr>
<td>MOSCAP</td>
<td>Metal Oxide Semiconductor Capacitor</td>
</tr>
<tr>
<td>OFDM</td>
<td>Orthogonal frequency-division multiplexing</td>
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<tr>
<td>OOK</td>
<td>On-Off Keying</td>
</tr>
<tr>
<td>PCE</td>
<td>Power Conversion Efficiency</td>
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<tr>
<td>PIE</td>
<td>Pulse Interval Encoding</td>
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<tr>
<td>PLF</td>
<td>Polarization Loss Factor</td>
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<tr>
<td>Q</td>
<td>Quality Factor</td>
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<tr>
<td>Rx</td>
<td>Receiver</td>
</tr>
<tr>
<td>SoC</td>
<td>System on Chip</td>
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<tr>
<td>SSP</td>
<td>Space Solar Power</td>
</tr>
<tr>
<td>SWIPT</td>
<td>Simultaneous Wireless Information and Power Transfer (SWIPT)</td>
</tr>
<tr>
<td>Tx</td>
<td>Transmitter</td>
</tr>
<tr>
<td>UHF</td>
<td>Ultra High Frequency</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
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<tr>
<td>VLSI</td>
<td>Very-large-scale integration</td>
</tr>
<tr>
<td>VNA</td>
<td>Vector Network Analyzer</td>
</tr>
<tr>
<td>WPRx</td>
<td>Wireless Power Receiver</td>
</tr>
<tr>
<td>WPT</td>
<td>Wireless Power Transfer</td>
</tr>
<tr>
<td>WSAN</td>
<td>Wireless Sensor/Actuator Network</td>
</tr>
</tbody>
</table>
## LIST OF FIGURES

2.1 Tesla demonstrating the transmission of electrical energy without wires during a lecture at Columbia College, New York, in 1891 [48]. 23
2.2 Typical block diagram of wireless power transfer systems. 24
2.3 RFID frequency bands and the power transmission method for each [33]. 26
2.4 Typical block diagram of wireless power receiver (WPRx). 27

3.1 The implantable wireless sensor chip position in the anterior chamber. 40
3.2 5.2GHz on-chip RF power harvesting module utilized in an implantable sensor. 41
3.3 System operation for the proposed implantable SoC [1]. 43
3.4 Structure of the on-chip receive antenna [2]. 46
3.5 (a) Simulated 3D radiation pattern of the antenna with -14.3 dBi of gain, and (b) Simulated far-field radiation pattern in the E-H-planes for the on-chip receive antenna [2]. 46
3.6 Five stages of synchronous rectifier used as a voltage multiplier. 48
3.7 Simulated RF to DC power efficiency and the DC output voltage of the rectifier versus the RF input power. 49
3.8 Simulated input impedance versus input RF power. 49
3.9 Schematic of the input matching network between the rectifier and the antenna. 50
3.10 DC Voltage Limiter Schematic. 50
3.11 Low Dropout Regulator Schematic. 52
3.12 Simulated Quiescent Current ($I_Q$) and Dropout Voltage ($V_{do}$). 52
3.13 VDD and VDDA Voltage Sensors Schematic. 53
3.14 The die microphotograph of the sensor chip. 54
3.15 A cross sectional view of the implantable IOP monitoring SoC test setup mimicking the anterior chamber of the eye. [1, 3]. 55
3.16 Measured VDDA (the LDO output) and VDDA_GD versus the input VDD. 57
3.17 Measured VDDA_GD and VDD_GD versus the varying input VDD. 57
3.18 Immersed Setup for RF measurement. 58
3.19 (a) Simulated and measured S11 and (b) 2D normalized far-field radiation pattern when the chip is immersed in saline solution and wire-bonded to PCB [2]. 59
3.20 Measured harvested DC voltage (VDD) versus the available power to the on-chip antenna (wireless powering). 60
3.21 Measured harvested VDD charging wirelessly versus different distances (wireless powering) .................................................. 61
3.22 Output voltage for two input power levels relative to other reported RF power harvesters .................................................. 62
3.23 Efficiency for two input power levels relative to other reported RF power harvesters .................................................. 62

4.1 Block diagram of a wireless power receiver ........................................ 65
4.2 (a) Schematic of a Dickson rectifier and (b) a conventional FX rectifier. 66
4.3 (a) Conventional FX rectifier efficiency versus RF power and (b) its alternating current, output DC voltage, and RF voltage. ............ 67
4.4 Schematic of the proposed self-biased cross-coupled rectifier ............. 68
4.5 Equivalent circuits of the proposed rectifier at (a) DC and (b) RF. ........ 69
4.6 Operating point of the rectifying device (MP1) configured (a) as a diode-connected transistor (Dickson rectifier); (b) as a cross-coupled transistor; and (c) as a self-biased transistor (proposed rectifier) .... 70
4.7 Simulation of (a) the dropout voltage \( V_{SD} \), and (b) drain current \( I_{DP} \) in the rectifying PMOS devices of the Dickson, conventional FX, and proposed rectifiers at 37\( \mu \)W input power level. ................. 72
4.8 (a) Simulated output voltage, (b) alternating charges flowing into MP1 per RF cycle (\( Q_p \)), and (c) power conversion efficiency (PCE) for the Dickson, conventional FX, and proposed rectifiers versus RF input power. 73
4.9 Transient simulation of the charging time of the proposed (solid) and conventional FX (dashed) rectifiers for load capacitances (a) 0.5\( nF \) and (b) 0.1\( nF \). .............................................................. 76
4.10 Die microphotograph of (a) the proposed self-biased rectifier and (b) an enlarged view of active area with the feedback resistors. ............ 77
4.11 (a) Photo and (b) diagram of the RF-measurement setup ................. 78
4.12 Calibrating the differential dual microwave probe: (a) GSGSG dual (b) Probe planarization (c) Probe calibration using impedance probe standard substrate (ISS). ................................................. 80
4.13 Simplified program flowchart of the automated RF testing ............. 81
4.14 Measured PCE of the proposed (solid) and conventional FX (dash) rectifiers versus input power for three loads. ......................... 83
4.15 Measured output DC voltage of the proposed and conventional FX rectifiers at 433MHz versus RF input power for various loads. ....... 84
4.16 (a) Measured ratio of the proposed rectifier PCE relative to the conventional FX rectifier PCE for three different loads, and (b) measured dynamic range of the proposed and conventional rectifiers. ........ 85
4.17 Measured input (series) resistance of the proposed and conventional FX rectifiers at 433MHz versus RF input power for various loads. 87
4.18 Measured input (series) capacitance of the proposed and conventional FX rectifiers at 433MHz versus RF input power for various loads. 87
5.1 (a) Schematic of a single-stage, conventional cross-coupled rectifier and (b) its power conversion efficiency versus RF input power.

5.2 Schematic of the proposed adaptive rectifier.

5.3 (a) Simulated currents, and (c) voltage drops of the rectifying PMOS in the conventional and proposed rectifiers.

5.4 Charges per RF cycle in conventional and proposed rectifiers for 1.6V output DC voltage.

5.5 Simulated standby (a) current and (b) power of the sensing branch MN3,4 in the proposed rectifier versus the output voltage.

5.6 (a) Microphotograph of the realized adaptive rectifier on CMOS 0.18 µm with test pads and (b) an enlarged view of the active area.

5.7 Simulated (dashed) and measured (solid) power conversion efficiency versus RF input power for the proposed and conventional rectifiers.

5.8 Simulated (dashed) and measured (solid) output DC voltage of the proposed and conventional rectifiers versus RF input power.

5.9 (a) Measured output DC voltage of the proposed (solid) and conventional (dashed) rectifiers versus RF input power for different loading conditions, and (b) the relative improvement percentage ($\Delta V_o$) for three different power levels.

5.10 Measured power conversion efficiency versus RF input power for the proposed (solid) and conventional (dashed) rectifiers for different loading conditions.

5.11 Measured power conversion efficiency of the proposed (solid) and conventional (dashed) rectifiers versus the output DC voltage.

5.12 Measured PCE peak efficiency of the proposed (solid) and conventional (dashed) rectifiers versus different loads.

5.13 Measured dynamic range of the proposed (solid) and conventional (dashed) rectifiers versus different loads.

5.14 Measured power conversion efficiency (PCE) of both the proposed adaptive and self-biased rectifiers, and the conventional rectifier versus RF input power levels at UHF band.

5.15 Measured input (series) resistance of the proposed (solid) and conventional (dashed) rectifiers versus RF input power for different loads.

5.16 Measured input (series) capacitance of the proposed (solid) and conventional (dashed) rectifiers versus RF input power for different loads.

6.1 Power conversion efficiency versus RF input power for state-of-the-art UHF rectifier [4].

6.2 Potential blocks and techniques for further enhancement in the wireless power receiver front end.
LIST OF TABLES

2.1 Comparison of the RF rectifiers according to I-V characteristics . . . 35
2.2 Selected RF to DC converters with $V_{IN} < V_{OUT}$ from recent publications 37
3.1 Comparison of RF Power Harvester for Implantable Sensors . . . . . 63
4.2 Self-biased rectifier performance summary and comparison. . . . . . 88
5.1 The performance of the adaptive rectifier versus the self-biased rectifier and state of the art UHF rectifiers. . . . . . . . . . . . . . . . . 107
Chapter 1

Introduction

Wireless power transfer (WPT) is the key enabler technology for a myriad of applications across a very diversified scale. In terms of power levels, wireless powering applications start from $\mu W$-levels as in radio frequency identification (RFID) tags [5–7] and mm-sized bio-implants [3, 8, 9] and grow to wirelessly-powered smart-home appliances [10, 11] and electric vehicles that are charged wirelessly on the road [12–16]. Furthermore, $Giga W$-scale wireless powering has been investigated since the 1970s [17, 18] and has a potential to wirelessly power cities from space-based solar cells [19].

Besides being the most common WPT application, RFID paves the way for the Internet-of-things (IoT), where computing devices, machines, objects, animals, and people are connected to the Internet with unique identifiers. According to the research firm IDTechEx, the total RFID market size in 2015 was $10.1$ billion, and is forecast to be $18.68$ billion by 2026 [20]. Although 80% of RFID tags are used for tracking retail apparel and footwear, the use of RFIDs in other vital applications such as biomedical implants [21, 22] and wireless sensors [23] is rapidly growing. Currently, RFID smart cards [24] are used to go beyond the traditional access control by enabling contactless payment through “wave and pay” transactions [25]. In industry, RFID is utilized for contactless wafer probing to replace the traditional wafer probe cards, increasing yield and accelerating production testing [26].

The recent fast scaling in nano-electronics enables a high level of integration and
thus smarter RFID systems empowered with low-energy wireless MCUs, larger memory, various sensors, and therefore more capabilities. Instead of only being interrogated by a base station (reader), wireless sensors are able to communicate with each other, forming various network topologies in multihop communication schemes [27]. Consequently, wireless sensor/actuator networks (WSAN) are growing across diverse markets including home and building automation, health care, lighting, automotive, and oil and gas industries. However, the main limiting factors for RFID technology to be utilized in more potential WSAN applications are the size and cost of the RFID tags and the communication data rate, which is currently limited up to 640 kbit/s for the UHF EPC standard [28]. Many applications would adopt RFID technology if the tag size became smaller and/or the data rate was increased while maintaining the same cost per tag.

1.1 Biomedical Implantable Devices

Biomedical implantable devices become advanced in accuracy and performance with the rapid progress in nanoelectronics and sensing technologies. This progress meets high demand for medical solutions that are more convenient for doctors and less painful for patients. Telemedicine is a very promising approach to enable remote health-care solutions in which the patients’ physical data (such as temperature, pressure, glucose level, etc.) are monitored (at home or work and while running or at rest) using implantable devices and transmitted to their medical doctors or, if needed, to emergency services. Bioimplants are not only for sensing and diagnosing, but also can deliver an appropriate drug dose as an autonomous implantable treatment [29]. Furthermore, implantable devices can send electric signals directly to the brain or to body organs with next generation bioelectronic treatments [30,31].
The most challenging aspects of these implantable microsystems are the device lifetime and size, which are actually determined by the battery lifetime and the battery size, respectively. The external battery can be replaced by an integrated wireless power receiver that can collect electromagnetic energy and convert it to a DC supply voltage, powering the circuits of the implant. This enables a miniaturized, batteryless (passive) device that is powered wirelessly from a remote reader, similar to the RFID systems.

Passive RFID technology at UHF band achieved robust identification up to a range of $10m$ with inexpensive tags, and got well established standards [28, 32] that assure compatibility between tags and readers from different manufacturers. However, the RFID tag chip still needs to be attached to an external off-chip antenna, increasing the size and cost of the tag. Currently, RFID die costs less than $0.05$ per $1mm^2$ [33–35] (considering a typical production cost of a $1000$ per processed wafer [33, 36], which contains more than $22,000$ working die –considering $90\%$ yield and $85\%$ for the ratio of dies fitting onto the wafer net area, after subtracting $3mm$ of useless edge from the $200mm$ wafer [33]). On the other hand, the off-chip antenna can cost as much as $0.12$ with current technology plus a $0.033$ assembly cost [35]. In addition, operating at UHF band requires bulky RFID readers with big antennas. Thus, a significant impact on the RFID tag size and cost can be achieved by integrating a miniaturized on-chip antenna with the RF-power receiver in a single chip. This eliminates the need for the off-chip antenna and the external battery. By such system integration, a pinless, self-contained, CMOS-only tag can be achieved with no external off-chip components [37], and thus neither wire bonding nor special chip packaging is required. Consequently, this tiny miniaturized system enables an implantable sensing platform for several biomedical applications.
1.2 Wireless Powering Link

All of these WPT applications utilize wireless power transfer link, which consists of wireless power transmitter and receiver. Each application has specific requirements (and constraints) that define the power levels and frequency bands used for the wireless powering link. However, for all wirelessly powered systems, the main target is to maximize the output power and range of the link. Given that transmitted power from the source is fixed, minimizing the link losses maximizes the output power delivered to the load, and consequently the link efficiency is maximized. By the same token, in order to extend the wireless powering range, the link efficiency has to be maximized across the input power levels that are available away from the source across the entire operating range. Therefore, minimizing the losses in the wireless power receiver (WPRx) front end across different RF power levels will boost and extend the efficiency over wide range of RF power levels.

There are three main loss components in the WPRx. The first component is formed by the losses in the matching network including the mismatch reflection loss and the internal losses in the matching network elements. The second component is the dissipation loss in the devices of the RF-to-DC power converter. The third component is the reverse leakage loss of the harvested energy from the output storage capacitor to the antenna, through the RF-to-DC power converter. The second and third components are completely controlled by the RF-to-DC power converter architecture. The fully cross-coupled (FX) rectifier is commonly used in RFID and wireless powered sensors [38, 39] due to its sensitivity at low RF power levels. However, the FX rectifier suffers from a high reverse leakage loss at high RF power levels. In this work, we propose new architectures for the RF-to-DC power converter to minimize the reverse leakage loss of the conventional FX rectifier without losing its
sensitivity advantage. As a result, the proposed architectures operate efficiently over wide range of input RF power levels.

1.3 Thesis Contributions

The contributions of the thesis can be summarized as:

1. Designing and implementing a fully integrated, miniaturized, wirelessly powered implantable sensor with on-chip antennas as a single-chip solution [1–3, 40].

2. Building a custom test setup emulating the human eye, and in-vitro testing the wireless chip inside this eye-like lossy environment [1–3, 40].

3. Proposing and prototyping a self-biased RF-to-DC power converter with an input power range extension of more than 50% relative to the conventional cross-coupled rectifier [41].

4. Proposing and prototyping a wide-range RF-to-DC power converter using an adaptive self-biasing technique that doubles the range of conventional wireless power receivers without sacrificing the peak efficiency or the sensitivity [42].

5. Automating and accelerating the RF chip testing, including RF differential measurements of the nonlinear rectifier circuits using single-port VNA versus massive sweeps of RF-power levels, frequencies, and loading conditions [41–43].

1.4 Thesis Outline

This chapter presents the motivation and summarizes the thesis contributions.

Chapter 2 presents an overview of wireless powering systems and methods; a background on wireless power receiver’s architectures and operation and performance metrics used for evaluation. These are followed by a discussion about the main design
parameters utilized to optimize the performance in view of the input and output conditions.

Chapter 3 presents a miniaturized, fully integrated wireless power receiver [3] with an on-chip antenna [2], designed as a part of an implantable intraocular pressure monitor (IOPM) [1,3] for Glaucoma patients. The full system operation is explained and accompanied by the design considerations [40]. Afterwards, the design of the wireless power receiver is described in detail, including that of the 5.2GHz five-stage rectifier matched to an on-chip antenna and a DC-power management unit, which is composed of a DC voltage limiter, two voltage sensors, a low-dropout voltage regulator, and a MOSCAP-based on-chip storage. The custom test setup is presented and followed by the measurements’ results. In-vitro measurements show that in the lossy medium the proposed chip can be wirelessly charged to 1V from a 5W transmitter 3cm away from the harvester chip. The 2.5nJ energy stored on the 5nF on-chip capacitor, when charged to 1V, is sufficient to drive an arbitrary 100µW load for 9µs at regulated 0.8V. The simulated efficiency of the RF rectifier is 42% at −7dBm of input power.

Chapter 4 presents a self-biased RF-to-DC power converter with enhanced power conversion efficiency [41]. The range of the proposed architecture is wider than the range of both the diode-connected and cross-coupled rectifiers. A prototype of the proposed architecture is designed for UHF 433MHz RF powering applications and is implemented using 0.18µm CMOS technology. The operational concept is explained in details, and an automated test setup is proposed and discussed with the measurement methodology. Finally, the experimental results are presented and compared to the recent work in literature. The proposed architecture demonstrates an improvement of more than 40% in the power conversion efficiency (PCE) and an input power range extension of more than 50% relative to the conventional cross-coupled rectifier. A sensitivity of -15.2dBm (30µW) input power (for 1V output) and a peak
power-conversion efficiency of 65% are achieved for a 50kΩ load [41].

Chapter 5 presents a wide-range RF-to-DC power converter using an adaptive self-biasing technique to suppress the reverse leakage at high RF power levels without decreasing the PCE peak [42, 43]. The proposed architecture is presented, and a prototype is designed for UHF RFID applications using 0.18µm CMOS technology. The on-chip measurements demonstrate a sensitivity of −18dBm for 1V output over a 100kΩ load and a peak RF-to-DC power conversion efficiency of 65%. A conventional, fully cross-coupled rectifier is fabricated alongside for comparison, and the proposed rectifier shows more than a 2× increase in dynamic range and a 25% boosting in output voltage compared to that of the conventional rectifier [42, 43].

Chapter 6 concludes the dissertation. The contribution of this work is summarized and an outlook for the future work is presented.
Chapter 2

Background and significance

Wireless power transfer (WPT) is the transmission of electrical energy from a power source to an electrical load across an air gap (or free space), without connectors or electric conductor. Within three years of the discovery of radio waves by Heinrich Hertz in 1880 [44, 45], wireless power transfer was demonstrated by Nikola Tesla using the setup shown in Fig. 2.1 [46–48]. Since then, WPT has gained a lot of research interest in maximizing the efficiency of energy transfer, and thus to maximize the power delivered to the load. This chapter presents an overview of the WPT process and its stages, followed by a brief discussion about possible methods for WPT. Then, a further discussion focused on the wireless power receiver architecture and its specifications is presented.

2.1 WPT system overview

As shown in Fig. 2.2, the WPT process consists of four stages: (1) RF power generation, or DC-to-RF power conversion; (2) RF power transmission through space; (3) RF power collection; and (4) RF-to-DC power conversion to power the electrical load [18]. Enhancing any of these stages improves the overall efficiency of the WPT process. For instance, generating (and transmitting) an optimal RF waveform (e.g., multi-sine signals with high peak-to-average power ratio) is demonstrated to improve the RF-to-DC conversion efficiency of rectifier circuits at the receiving end of the
WPT system [49]. In that work [49], the optimal waveform is composed of individual signals that are amplified, radiated through multiple antennas, and then combined in the air. For simultaneous wireless information and power transfer (SWIPT), the RF waveform can be optimized such that both the communication rate and energy are maximized for OFDM-based SWIPT systems, such as the work in [50,51]. Furthermore, a joint beamforming algorithm is proposed in [52] for multiuser wireless information and power transfer (MU-WIPT) system that is compatible with the conventional multiuser multiple input multiple output (MU-MIMO) systems.

2.1.1 Wireless power transfer methods

The wireless energy can be transferred in the air interface of a WPT system by using near-field reactive coupling or far-field electromagnetic radiation. Each method has its own characteristics, advantages, and limitations.
Near-field reactive coupling

In the near-field coupling, power can be transferred either via electrostatic induction (alternating electric-field) between metal electrodes, as in the capacitive coupling, or via electromagnetic induction (alternating magnetic fields) between coiled wires, as in the inductive coupling [53]. Although the first WPT demonstration (by Tesla) utilized capacitive coupling, as shown in Fig. 2.1 [46–48], inductive coupling attracted more interest, as demonstrated later by Tesla, also [54]. Through the following research works across the 1900s, inductive coupling showed advantages of higher power handling and longer air distance than capacitive coupling. Recent advances in capacitive coupling, however, show high efficiency and high power handling that are comparable to, or even higher than, inductive coupling across very short gap distances (i.e., <1mm) [54]. Accordingly, capacitive coupling represents a better choice for very small gap (contactless charging) applications [55] such as wirelessly charging laptops or kitchen appliances while standing freely on the table, or inter-chip data and power transfer across dies in 3D VLSI [56]. However, the capacitive coupling efficiency significantly drops for air gaps >1mm, while inductive coupling maintains a 90% efficiency for air gaps >1mm to 10s of centimeters at the same power levels.
and coupling area. Therefore, inductive coupling is a better choice than capacitive coupling to power biomedical devices implanted deeply inside the body.

It should be noted that handling higher power levels requires larger coupling surfaces for both capacitive and inductive coupling. In terms of operating frequencies, inductive coupling can utilize a broader range (i.e., 10s kHz to 10s MHz) than capacitive coupling, which requires higher operating frequencies (i.e., 100s kHz to 10s MHz [54]). Generally, near-field reactive coupling is non-radiative (i.e., the energy is highly confined in the air gap [near transmitter] between the coupling elements) and hence near-field reactive coupling achieves higher efficiency across short gaps than radiative far-field transmission. The reactive (non-radiative) near-field distance is commonly less than $0.62\sqrt{D^3/\lambda}$ for most antennas, or less than $\lambda/2\pi$ for very short dipole (or equivalent radiators), where $D$ is the largest dimension of the antenna [57].

**Far-field electromagnetic radiation**

Far-field (Fraunhofer) region is defined as the region of the field of an antenna where the angular field distribution is independent of the distance from the antenna and is commonly taken to exist at distances greater than $2D^2/\lambda$ from the antenna, where $D$ is the largest dimension of the antenna [57]. Unlike the energy confinement of the near-field coupling, the transmitted power ($P_t$) in the far-field electromagnetic (EM) radiation is spread over radiated spheres ($P_t/4\pi R^2$), decaying by square of the distance ($R$) away from the antenna, and is enhanced (shaped) relative to isotropic radiation by the gain (directivity) of the transmitting ($G_t$) and receiving ($G_r$) antennas. Overall, the received power ($P_r$), in the far-field wireless power transfer can be expressed by Friis transmission equation [57]:
Although having less transmission efficiency, the far-field radiation propagates across longer distances than near-field coupling, allowing several long-range wireless powering applications such as RFIDs or even microwave power channels from space solar power (SSP) [17, 19]. Additionally, the near-field inductive coupling requires fixed orientation between coils, however the far-field EM transmitting and receiving antennas do not have to be in a fixed orientation, particularly if the antennas are circularly polarized [57]. This advantage makes the far-field EM radiation more suitable for powering floating implantable devices with a dynamic orientation inside the body, and enables an arbitrary position of the external hand-held reader (the wireless power source). Generally, inductive coupling is the realistic choice at low frequencies, longer wavelengths, and longer reactive near-field region, while the far-field radiation becomes adequate with reasonable antenna size at higher frequencies, as shown in Fig. 2.3.

For these advantages, far-field radiation is selected for powering the biomedical...
After generating the optimal RF power signal and transmitting it either via near-field coupling or far-field radiation, the next stage is the wireless power reception. The function of the wireless power receiver is to pick-up the RF power and convert it to DC power for an electrical load, or store it in an energy storage. A typical block diagram of an RF power receiver is shown in Fig. 2.4. It is comprised of an antenna, an input RF matching network, an RF-to-DC power converter (RF rectifier), a storage capacitor, and an optional DC power management to generate and control specified voltage rails according to the requirements of the system-on-chip (SoC).

There are two main specifications of the wireless power receiver (WPRx) that affect the entire WPT chain. The first is the sensitivity of the WPRx front-end, which determines the wireless range of the WPT process. The second is the efficiency of the WPRx, which is mainly defined by the RF-to-DC power conversion efficiency (PCE).
2.2.1 WPRx Specifications

Sensitivity ($P_{RFmin}$)

The minimum RF power ($P_{RF}$), available at the WPRx antenna, that is required by the WPRx to generate the minimum usable DC voltage for the load. After incorporating the reflection mismatch at the transmitting ($\Gamma_t$) and receiving ($\Gamma_r$) antennas and polarization loss factor ($PLF$) into equation 2.1, the RF power available at the WPRx antenna can be calculated by:

$$P_{RF} = P_t G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2 (1 - |\Gamma_t|^2)(1 - |\Gamma_r|^2) \times PLF$$  (2.2)

As expressed in equation 2.2, the available RF power $P_{RF}$ depends upon the RF link budget starting from the available effective isotropic radiated power ($EIRP$), which is the transmitted power ($P_t$) times the gain of the transmitting antenna ($G_t$). Then, multiplied by the receiving antenna gain ($G_r$) and the path loss, which is a function of the utilized RF frequency (or the wavelength, $\lambda$) and the communication distance ($R$).

After all, the RF matching network is utilized to produce the highest possible RF voltage from such low received RF power ($P_{RFmin}$) to turn on the rectifying devices of the RF-to-DC power converter. Also, the matching network is optimized to minimize the reflection mismatch ($\Gamma_r$) between the RF rectifier and the antenna. Consequently, the system can function at a very low received RF power and hence from a long communication distance from the transmitter.

In summary, the minimum available RF power from the link budget and the turn-on voltage of the rectifying devices are the main parameters for the sensitivity of the WPRx frontend and thus the wireless powering range. There have been many recent research works to improve the sensitivity of the RF power harvester and hence the communication range.
Efficiency \( (\eta = \frac{P_{DC}}{P_{RF}}) \)

The efficiency of the WPRx front end is the ratio of the output DC power \( P_{DC} \) delivered to the load relative to the available RF power \( P_{RF} \) from the antenna. It is mainly determined by the RF-to-DC power conversion efficiency \( (PCE) \) of the rectifier and the efficiency of the RF matching network, which can be neglected for lossless (and perfect) matching network. The RF to DC power conversion efficiency \( (PCE) \) can be expressed by equation 2.3

\[
PCE = \frac{P_{DC}}{P_{RF}} = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{in} + P_{loss}} \tag{2.3}
\]

\[
P_{loss} = P_{FWD} + P_{RVS} \tag{2.4}
\]

Where \( P_{loss} \) is the power loss of the rectifier stages, and is mainly due to the resistive (dissipation) loss \( P_{FWD} \) in the rectifying devices during the forward (conduction) period and due to the reverse leakage loss \( P_{RVS} \), emerging from the reverse current, flowing from load to the antenna when the instantaneous RF voltage drops lower than the output DC voltage [38,58].

Input impedance

The input impedance of the RF-to-DC power converter must be conjugately matched to the impedance of the on-chip antenna. At the same time, the input resistance determines the quality factor of the circuit and hence the bandwidth of the RF front end. As the rectifier is essentially a nonlinear circuit, its input impedance greatly varies with RF input power levels. A common practice by RFID designer is to design the matching network at the input impedance of the lowest RF power level (the
rectifier sensitivity) that provides acceptable output DC voltage. Then, the nonlinear mismatch occurring at higher power levels is compensated by the excess input power.

**Output DC voltage**

It depends upon the application requirements. Multistage configuration of voltage multipliers can be used to raise the output voltage to the required level. However, adding more stages decreases the overall power conversion efficiency due to the added losses. Also, increasing number of stages lowers the RF input impedance of the rectifier (i.e., it lowers the input resistance and increases the input capacitance).

**Output DC current (loading)**

It also depends upon the application requirements. Normally, it is the leakage current of the complete system on-chip in standby (sleep) mode during the charging time.

### 2.2.2 WPRx design challenges

In order to design a miniaturized WPRx front end for biomedical implantable devices, there are some challenges that should be addressed.

**On-chip antenna**

Designing on-chip antenna has two challenges. First, on-chip antennas are inefficient and have low gain due to the silicon substrate leakage. Second, miniaturized antennas are inefficient due to operation out of resonance. Moreover, the on-chip antenna has small impedance that adds more challenges to the RF matching network between the on-chip antenna and the RF rectifier.
RF Matching

In addition to the nonlinear variation of the rectifier input impedance with the RF power levels, the on-chip matching elements have very low quality factors due to substrate leakage, and are very sensitive to process variations.

RF Rectifier

The minimum voltage required to turn on the rectifying devices sets the WPRx sensitivity and hence the wireless range of the WPT system. Also, the rectifier PCE and total WPRx efficiency is highly affected by the rectifier losses. Furthermore, the rectifier specs are highly dependent upon the loading condition as well as on the RF input power levels. It is worth mentioning that output loading would vary due to the adopted power sequence of the SoC from standby mode to full running mode.

These challenges should be addressed with regards to the available power, which is limited by FCC regulation for health concerns and further attenuated through the lossy on-chip antenna and matching network. Another power constraint, which is addressed in the next chapter, is the in-vivo operation of the implantable chip within the lossy medium inside the human body.

DC Voltage regulations

The output DC voltage from the rectifier is not stable, as the input RF power level can vary due to the variations in the distance to the external reader (RF power source). This necessitates adding “inefficient” voltage regulation, which limits the overall performance of the battery-less system.
2.2.3 WPRx Design Tools

The design process of an RF power receiver module utilizes the following degrees of freedom to achieve the required specifications for a certain application:

Stage Architecture

Several circuits’ architectures have been utilized for RF-to-DC power conversion. Starting with the most early cited Greinacher voltage multiplier (known also as Cockcroft-Walton Multiplier) \[59\], then moving to the Dickson voltage multiplier \[60\], then a lot of modifications have been proposed and developed to enhance the performance of these architectures.

Number of stages

Cascaded series of rectifier stages are utilized to increase the output DC voltage to satisfy the application requirements. However, by adding more stages in series in the DC path, all their RF inputs are all shunted to the RF input. This significantly lowers the input impedance and hence the sensitivity and the efficiency of the complete multi-stage voltage multiplier. Also, it increases the high frequency substrate losses by the chip area.

Circuits design parameters

The rectifier specs is designed and optimized using the geometry of the MOS devices such as the width (W), the length (L) and number of fingers (nf), and the pumping capacitors at the RF input.
Antenna resistance ($R_A$)

In some cases it is a design parameter as pointed in [61]. For a sensitive (low-power) RF power harvesting module, the rectifier has to work with very low input RF power and thus a large $R_A$ to raise the input RF voltage to the rectifier so the rectifier can produce a high output DC voltage with a high power conversion efficiency. However, usage of high $R_A$ increases the circuit quality factor $Q$ and hence reduces the bandwidth [61].

2.3 Literature review and rectifier topologies

On-chip and off-chip RF power harvesters are widely used in many applications. Off-chip RF power harvesters have discrete off-the-shelf components and are bulky. On the other hand, the on-chip RF power harvester is an essential module for passive RFID tags that are running without a battery. However, most of the on-chip RFID power harvesters have to be attached to an off-chip antenna such as in [5, 7, 62] and this makes it inadequate for biomedical implantable devices and other applications that require a very miniaturized system.

RF power can be wirelessly transmitted to the RF power harvester by either a near-field magnetic coupling or a far-field electromagnetic coupling. The boundary between the near-field and the far-field is $\frac{\lambda}{2\pi}$ where $\lambda$ is the wave length of the RF signal [63].

RF power harvester can be classified in terms of the RF frequency bands such as HF (13.56 MHz) RFID, which use near field magnetic coupling for wireless powering and communication. This limits the communication range to less than 1m and it requires perfect alignment between the transmit and receive coils. As the RF frequency increases the harvester can utilize the far-field electromagnetic wave transmission,
and thus it has a longer communication range, higher data rate, smaller antenna
dimension, and more immunity to misalignment between the transmitter and the re-
ceiver as in the UHF and higher RF frequencies such as ISM 900MHz [38] and 2.4GHz
bands and mm-wave 60GHz as in the mm-wave RFID (MMID) [37,64–66]. So, the
proposed RF power harvesting module, in the next chapter, is running in far-field
operation mode and is utilizing the low gigahertz range, which are suitable for most
of the biomedical tissues based on the recent study by A. Poon et al. [67].

Many researches have been done to enhance either the efficiency or the sensitivity
of the RF power harvesters at a specific frequency for certain application requirements.
Choosing the suitable architecture for the RF rectifier stage or modifying it can lead
to a significant improvement for the required specs. As mentioned in the previous
section 2.2.3, the Dickson voltage multiplier is one of the most common rectifier
architectures. Architectures used for RF to DC power converter (RF rectifier stage)
can be classified according the I-V characteristic of their operations as shown in table
2.1 [61]

The Dickson voltage multiplier is implemented with normal diodes or Schottky
diodes to minimize the drop voltage and hence leads to high efficiency. Also, the
Dickson multiplier can be implemented on a standard CMOS technologies by diode-
connected MOSFETs, but with the main drawback of a higher voltage drop of at
least one threshold voltage, which lowers the power conversion efficiency especially
at low input RF voltage. Some other modified Dickson architectures are reviewed
in [63] such as the Dickson multiplier with static charge transfer switches [77] and
the Dickson with bootstrapped gate transfer switches. A self-driven synchronous
rectifier (fully cross coupled differential) is also proposed in [39], which can work on
a lower RF input power with a high relative power conversion efficiency as the cross-
coupled MOS devices are working in triode (linear) region, holding a smaller drop
<table>
<thead>
<tr>
<th>Architecture I-V Characteristic</th>
<th>Implementation</th>
<th>advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
</table>
| **Exponential I-V curve**       | - Schottky diode [68]Karthrus 03 [69]Barnett 09  
- p-n junction diode [70]Vita 05a  
- Diode-connected low-Vth MOS transistor working in sub-threshold region [71]Teh 09 | -Rectifier using Schottky diode could work at very low input voltage below 150mV with reasonable efficiency of about 10%. With larger input voltage, the efficiency will become much higher. | -Schottky diode is usually not available in standard CMOS process  
-Suffer from process and temperature variations |
| **Square-law I-V curve**         | -Diode-connected zero-Vth MOS transistor [5]  
Curty 05 [72]Yi 07  
-Diode-connected normal-Vth MOS transistor with Vth compensation [73]Umeda 06 [74]Nakamoto 07  
-Diode-connected low-Vth MOS transistor working in strong-inversion region [75]Yeoh 05 | -Rectifier using zero-Vth MOS transistor and normal-Vth transistor with Vth-compensation could achieve good efficiency of 20-60% with input voltage amplitude of 150-500mV | -Zero-Vth MOS transistor suffers from process and temperature variations. The same may be true for normal-Vth transistor with Vth-compensation, depending on the compensation method. |
| **Linear I-V curve**             | -Normal-Vth or low-Vth MOS transistor working in linear region, i.e., turned on completely as a switch [76]Driscoll 08 [38]Kotani 09 | -Rectifiers using MOS transistor as switch could achieve high efficiency > 60% with input voltage amplitude higher than Vth+400mV or so. | -Requires very high antenna resistance for small input power, reducing the bandwidth. |

Table 2.1 – Comparison of the RF rectifiers according to I-V characteristics
voltage and hence lower power losses in the rectifier itself and higher overall power conversion efficiency. Threshold cancellation techniques are developed and proposed with external sources as in [73], or with internal biasing such as in [74] to improve the sensitivity. Further studies and analyses of different potential rectifier architectures are discussed in Chapter 4.

An important reason for low power conversion efficiency of multistage voltage multipliers is the propagation of high-frequency signals throughout the circuits and hence with higher substrate losses. In [78] proposed is a single-stage RF rectifier to generate the DC voltage and then boost this DC voltage by a charge-pump and a low frequency VCO on chip.

Active rectifiers are proposed to improve the efficiency by driving the MOS devices into linear region with high VGS by fast comparator as in [79–81] or an inverter as in [82]. This decreases the ON resistance of the MOS devices and its drain-source drop voltage and hence lowers its losses.

In [38], a high-efficiency CMOS rectifier circuit for UHF RFID's is presented with a cross-coupled bridge configuration and is driven by a differential RF input. A differential drive active gate bias mechanism simultaneously enables low ON-resistance and small reverse leakage of diode-connected MOS transistors, resulting in large power conversion efficiency (PCE), especially under small RF input power conditions. At the single-stage configuration, 67.5% of PCE was achieved under conditions of 953 MHz, 12.5 dBm RF input, and 10 k output load.

In [9,76], an adaptive RF matching is presented for mm-size implantables at 915 MHz to account for the variability of the RF link inside the body. In [79,80] an adaptive reconfigurable active voltage doubler/rectifier is proposed to improve the efficiency of an inductive coupling of 13 MHz under variable input voltage levels. Some representative RF to DC power converters running in low microwave range
<table>
<thead>
<tr>
<th>Reference</th>
<th>PIN</th>
<th>VIN</th>
<th>Frequency</th>
<th>Efficiency</th>
<th>VOUT</th>
<th>Technology</th>
<th>Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>[74] Nakamoto07</td>
<td>450 μW</td>
<td>0.95</td>
<td>953 MHz</td>
<td>&gt; 40 %</td>
<td>&lt; 3</td>
<td>0.35 μm CMOS</td>
<td>internal VTH cancellation, ferroelectric C, large R, Greinacher</td>
</tr>
<tr>
<td>38] Kotani09</td>
<td>225 μW</td>
<td>1.2*</td>
<td>953 MHz</td>
<td>65 %</td>
<td>2.6</td>
<td>0.18 μm CMOS</td>
<td>self-driven synchronous</td>
</tr>
<tr>
<td>9, 76] O’Driscoll09</td>
<td>200 μW</td>
<td>0.75</td>
<td>915 MHz</td>
<td>65 %</td>
<td>1.5</td>
<td>0.13 μm CMOS</td>
<td>self-driven synchronous</td>
</tr>
<tr>
<td>[83, 84] Le08</td>
<td>160 μW</td>
<td>0.71*</td>
<td>900 MHz</td>
<td>60 %</td>
<td>6</td>
<td>0.25 μm CMOS</td>
<td>floating gate with one time charge injection, Greinacher</td>
</tr>
<tr>
<td>[68] Karthaus03</td>
<td>28 μW</td>
<td>0.69</td>
<td>868 MHz</td>
<td>28 %</td>
<td>1.5</td>
<td>0.5 μm CMOS</td>
<td>schottky diodes, Greinacher</td>
</tr>
<tr>
<td>6] Kocer06</td>
<td>11 μW</td>
<td>0.09</td>
<td>450 MHz</td>
<td>9 %</td>
<td>1</td>
<td>0.00 μm CMOS</td>
<td>low VTH devices, Greinacher</td>
</tr>
<tr>
<td>[39] Mandal07</td>
<td>8.5 μW</td>
<td>0.36</td>
<td>950 MHz</td>
<td>23.5 %</td>
<td>0.5</td>
<td>0.18 μm CMOS</td>
<td>self-driven synchronous</td>
</tr>
<tr>
<td>[68] Karthaus03</td>
<td>7.5 μW</td>
<td>0.36</td>
<td>868 MHz</td>
<td>10 %</td>
<td>1.5</td>
<td>0.5 μm CMOS</td>
<td>schottky diodes, Greinacher</td>
</tr>
<tr>
<td>[39] Mandal07</td>
<td>6 μW</td>
<td>0.29</td>
<td>950 MHz</td>
<td>16.7 %</td>
<td>0.4</td>
<td>0.18 μm CMOS</td>
<td>self-driven synchronous</td>
</tr>
<tr>
<td>[83, 84] Le08</td>
<td>5.5 μW</td>
<td>0.13*</td>
<td>900 MHz</td>
<td>10 %</td>
<td>1</td>
<td>0.25 μm CMOS</td>
<td>floating gate with one time charge injection, Greinacher</td>
</tr>
<tr>
<td>5] Curty05a</td>
<td>2.7 μW</td>
<td>0.074</td>
<td>2.4 GHz</td>
<td>37 %</td>
<td>0.882</td>
<td>0.5 μm SOI</td>
<td>SOI, low VTH, Greinacher</td>
</tr>
<tr>
<td>73] Umeda06</td>
<td>40 μW</td>
<td>0.5</td>
<td>950 MHz</td>
<td>1.2%</td>
<td>1.5</td>
<td>0.3 μm CMOS</td>
<td>dynamic gate-drain biasing</td>
</tr>
<tr>
<td>73] Umeda06</td>
<td>250 μW</td>
<td>0.5*</td>
<td>950 MHz</td>
<td>11%</td>
<td>1.8</td>
<td>0.3 μm CMOS</td>
<td>dynamic gate-drain biasing</td>
</tr>
<tr>
<td>7] Shih11b</td>
<td>89 μW</td>
<td>-</td>
<td>2.4 GHz</td>
<td>-</td>
<td>1.5</td>
<td>0.13 μm CMOS</td>
<td>zero VTH</td>
</tr>
</tbody>
</table>

Table 2.2 – Selected RF to DC converters with $V_{IN} < V_{OUT}$ from recent publications
with far-field operation are compared in Table 2.2 from recent published data and from [85]. Also, these RF-to-DC converters are generating an output DC voltage higher than the input voltage. As mentioned earlier, low gigahertz operations with far-field are the most potential mode of operation for miniaturized wireless powering systems.
Chapter 3

5.2 GHz On-chip RF Power Harvesting Module

In this chapter, we present a 5.2 GHz on-chip RF power harvesting module [3] designed for an implantable wireless sensor system for intraocular pressure monitoring (IOPM) [1] with an on-chip antenna [2]. The complete system is implemented as a 1.4 $mm^3$ single chip on standard 0.18$\mu m$ CMOS process. The implantable sensor chip position in the anterior chamber is shown in Fig.3.1. The full System-on-Chip (SoC) is briefly presented in the following sections with the system design consideration. Then, a custom test setup is presented to mimic the bio-environment for a biomedical implantable IOPM inside the human eye. The on-chip receive antenna is then briefly discussed. Following this, the RF power harvesting module design is discussed in detail.

3.1 System Level Design

The proposed IOPM SoC is designed as a self-sufficient implantable device. Thus, it does not need any off-chip components or external pins for either powering or communication. A simplified block diagram of the entire system is shown in Fig.3.2. The system consists of an RF power harvesting and storage module with an on-chip receive antenna, control, and power management module; sensors module, and transmitter module. It has separate on-chip transmit and receive antennas. The system is designed at a 5.2$GHz$ license free UNII band [86], which is widely used for
Figure 3.1 – The implantable wireless sensor chip position in the anterior chamber.

indoor biomedical applications. The frequency is selected to facilitate on-chip antenna integration with usable gain while having appreciable signal penetration inside the eye.

The presented RF power harvesting module includes an on-chip receive antenna [2] for wireless powering and communication, an RF matching network, a multistage differential RF rectifier (as a voltage multiplier) to generate sufficient DC voltage from the incoming RF signal, a DC voltage limiter for over-voltage protection, a low-dropout regulator (LDO) to produce a cleaner analog power rail (VDDA) for circuits sensitive to voltage variations, voltage references for LDO and voltage sensors, and a MOSCAP-based on-chip energy storage.

3.1.1 System Operation

For efficient and secure communication without adding much complexity, the system is designed to communicate with an external reader using a simple on-off keying (OOK) modulation. The incoming 5.2 GHz RF carrier generated by the external reader is modulated by a 20 MHz clock and the unique ID of the addressed chip in the form of OOK data symbols. The implanted system is designed to maintain a communication
distance \( (R) \) of 10\( \text{cm} \) outside the eye to the external reader, as shown in Fig.3.3a, with a communication cycle designed using the modified EPC class 1, generation 2.0 protocol [28]. The communication data sent by the reader is encoded in pulse-interval encoding (PIE) format where zero and one corresponds to duty cycles of 80 and 50, respectively.

As a battery-less, implantable sensor, the system is designed to be wirelessly powered by RF energy from the external reader \((ER)\) during the first mode of operation. During this 'charging mode,' the external reader sends a continuous RF signal modulated by zero bits to the chip. The on-chip antenna receives this RF power, and the RF power harvesting module starts charging the MOSCAP storage with a DC voltage untill it reaches a specified level of 1.3\( \text{V} \). At this point the DC voltage sensor sends a power good signal \((VDD \ GD)\) to the control unit, and the system moves to the 'addressing mode' which enables the demodulator and the decoder. A start command is sent to the SoC from the \(ER\), which prevents interference with undesirable external devices working at the same frequency. The start command is followed by
a transmission of a 4 bit ID. The system remains in the 'addressing mode,' until the incoming ID is matched with the originally programmed ID on the SoC. Once the ID is matched, the system enters in the 'reading mode,' which activates the sensor and the ADC. The reading mode lasts for $2\mu s$ and the ADC data is read and stored in a register.

This is followed by the transmission mode in which the oscillator-based transmitter sends the SoC ID and ADC data to the ER in OOK format through a $2.4\,GHz$ Tx antenna. In all operating modes, the system resets to 'charging mode' in case of insufficient power. A state diagram for the four modes of operation is shown in Fig. 3.3b [1].

### 3.1.2 Design consideration

#### Frequency selection

The system is designed for license free ISM frequency bands at $2.4\,GHz$ and $5.2\,GHz$ for transmit and receive operations, respectively. Two different operating frequencies are used to reduce complexity and achieve good isolation between the Rx and Tx paths. The choice of these frequencies provides a good balance between the total size of the SoC, the dimensions of on-chip antennas, the communication range, and the power consumption among the others.

#### Technology Selection

For energy harvesting systems-on-chip designs, the leakage current of the devices is of prime importance. At the selected frequency range, the best technology node with minimum leakage is around $0.15\mu m$ [87, 88]. Hence from the available options it was chosen to design the system in a standard $0.18\mu m$ CMOS process with thick top
Figure 3.3 – System operation for the proposed implantable SoC [1]

(a) Basic operation and communication protocol utilized in the SoC

(b) State diagram for the SoC modes of operations
metal to achieve the highest possible quality factor ($Q$) for the antenna. Additionally, the MOSCAPs available in this technology have an eight times higher capacitance ($\sim 8fF/\mu m^2$) than MIMCAPs. This enables a comparatively large on-chip storage, which is necessary for the energy harvesting SoC.

### Link Budget Calculations

The implanted IOPM SoC is required to communicate at a 10cm distance from the external reader with an effective isotropically radiated power ($EIRP$) of 4W from the reader. The power density of the 5.2GHz signal at this distance from the reader can be calculated by the following equation considering an isotropic antenna:

\[
\text{power density} = \frac{EIRP}{4\pi R^2} = \frac{(4W)}{4\pi(10cm)^2} = 31.83 W/m^2 \tag{3.1}
\]

which is lower than the FCC limit of 50W/m$^2$ for human body continuous exposure averaged over six minutes of EM waves for occupational use [89–91]. Note that the real power density in the proposed design will be several orders of magnitude lower as the ER reader will send the powering signal only for a very short time ($t_p = 1ms$) for a few times a day to receive the pressure measurements on-demand. Hence, the real power density averaged over a 6 minute period as per FCC rules in [89,90] will be:

\[
\text{Average power density}_{(6\text{min})} = \frac{EIRP}{(6*60s)4\pi R^2} * t_p = 0.88 \mu W/m^2 \tag{3.2}
\]

For a 1ms communication cycle, the power density will be 0.88$\mu W/m^2$ at a distance of 10cm from the ER. This value is very low compared to the FCC limit and is safe to use for the implanted IOPM. The initial simulations in the selected technology have revealed that the on-chip RF rectifiers require at least -17dBm power at their input to function. Hence the minimum antenna gain for the Rx antenna, $G_r$, can be
calculated using the Friis equation as follows:

\[ P_r = P_t G_t G_r \left( \frac{\lambda}{4\pi R} \right)^2 \]  

(3.3)

\[ G_r = \frac{P_r (4\pi R)^2}{P_t G_t \lambda^2 \rho \tau} = \frac{(-17dBm)(4\pi \times 10cm)^2}{(4W)(c/5.2G)^2(0.5)(0.5)} = -20dBi \]  

(3.4)

Where \( P_r \) is the received power at IOPM, \( P_t \) is the transmitted power from ER, \( R \) is the distance between ER and the IOPM, \( \rho \) is the polarization loss, and \( \tau \) is the antenna mismatch loss. Using 4W (36 dBm) EIRP, 84 μW (-17 dBm) \( P_r \), 10cm distance, 50% (0.5) polarization, and 50% (0.5) antenna mismatch loss factors, the gain required for the receive antenna at \( f = 5.2GHz \) is -20dBi.

### 3.2 Antenna Design

Since the chip is for an eye implant, due considerations must be taken for the design and subsequent characterization. A bio-compatible package is necessary and must be added around the chip for a safe implant. The chip must be placed 5 mm inside the anterior chamber of the eye, as shown in Fig. 3.15. Due to the size limitations, integration of the antenna on the chip is quite challenging. However, the high permittivity aqueous humor inside the eye (\( \epsilon_r = 68 \)) aids in antenna miniaturization. On the other hand, the loss of this medium (\( \tan \delta = 0.2677 \)) seriously affects the antenna efficiency.

According to [92], with an EIRP of 4 W, a wireless IOPM device should be able to communicate with an external reader placed 10 cm away from the eye. The gain required for the antenna can then be calculated using the Friis equation [57]. The minimum voltage needed at the input of the rectifier to function is 0.4 V, which corresponds to roughly 21μW for the rectifiers in the design. The gain of the antenna
(a) 5.2 GHz differentially feed monopole antenna structure (in red) within the pad frame of the chip, designed in top metal (M6).

Figure 3.4 – Structure of the on-chip receive antenna [2]

(b) 0.18μm CMOS process stackup

Figure 3.5 – (a) Simulated 3D radiation pattern of the antenna with -14.3 dBi of gain, and (b) Simulated far-field radiation pattern in the E-H-planes for the on-chip receive antenna [2]

must be equal to or larger than -20 dBi.

The antenna is designed to receive a 5.2 GHz RF signal from an external source and feed it to the energy harvesting and storage unit. The antenna needs to be matched to the rectifier circuit, which has a complex input impedance of $Z_{rect} = 11.1 - j233.3$ Ω at 5.2 GHz. The design of the antenna must provide an input impedance of $Z_{Rx}$ that is the conjugate of $Z_{rect}$. In addition, the antenna geometry should leave enough space to design capacitors in the top metal (M6) layer.

A custom monopole is designed in the top metal layer, as shown in Fig. 3.4a.
Inductive feeding is used to provide the required, large inductance for matching with a highly capacitive impedance of the rectifier circuit. Furthermore, an inductive load is added at the other end to reduce the antenna size. A parasitic element near the monopole helps increase the gain. The input impedance of the monopole is $Z_{Rx} = 27.4 + j60 \ \Omega$ at 5.2 GHz. Despite considerable inductive antenna impedance, the large capacitive part of the rectifier could not be matched completely. A matching network composed of an on-chip inductor and two capacitors is thus utilized to provide the required conjugate match. Further details of the impedance matching follow in the next section. Fig.3.5 presents the simulated 3D radiation pattern and gain of the antenna. It can be observed that a maximum gain of -14.3 dBi is obtained along the plane of the substrate.

3.3 Circuits Design

3.3.1 RF to DC Voltage Rectifier

A multistage voltage multiplier is used as an RF-to-DC power converter to provide the complete system with a DC supply voltage (VDD) from an extremely low level RF power signal that is available from the on-chip antenna. As discussed in the previous section, the rectifier should work with an input RF power of $21\mu W (-16.7dBm)$. A circuit schematic of the five-stage voltage multipliers used in the power harvesting module is shown in Fig.3.6. A differential drive synchronous rectifier topology is selected to have high efficiency and to minimize the effect of threshold voltage in CMOS rectifiers [38].

In this work, the voltage multiplier is successfully operating at 5.2 GHz with a minimum input received RF power of $-17dBm$ (20 $\mu W$) to supply $1.3V$ DC output voltage as a global $VDD$ rail. Simulation of the RF-to-DC power conversion efficiency and the DC output voltage of the rectifier versus the input RF power in $dBm$ is shown
in Fig. 3.7. The designed rectifier achieved an RF-to-DC power conversion efficiency of 28% at 5.2GHz with the minimum received RF power condition of −17dBm and 42 as the maximum efficiency at −7dBm input RF power.

As a typical nonlinear circuit, the input impedance of the rectifier varies with respect to the input RF power, as shown in Fig. 3.8. This effect complicates the power matching circuit design and highly affects the overall sensitivity of the RF-power harvesting module. To achieve the highest sensitivity from the rectifier topology, a matching network has been designed to match the input impedance of the on-chip antenna to the input impedance of the rectifier at the minimum input RF power with which the rectifier can generate the minimum accepted DC voltage. An on-chip inductance and RF metal-insulator-metal capacitors (MIMCAP) are utilized to build the required matching network \( (C_m=0.2pF, L_m=3.54nH) \), as shown in Fig. 3.9.

### 3.3.2 DC Voltage Limiter

For short range communications, RF power can reach high levels that can generate DC voltage higher than the breakdown of the remaining circuits of the chip. So, a DC voltage limiter has been designed to clip the generated DC voltage to maximum 1.6V,
Figure 3.7 – Simulated RF to DC power efficiency and the DC output voltage of the rectifier versus the RF input power.

Figure 3.8 – Simulated input impedance versus input RF power.
and it is shown in Fig. 3.10. This voltage limiter acts as an over-voltage protection for the whole circuits supplied from the rectifier output voltage $VDD$. This DC voltage limiter works to drain the excess power in case of high RF power is received within a short reading distance, for example.

### 3.3.3 Low Dropout (LDO) Voltage Regulator

A low dropout (LDO) voltage regulator is designed to supply a clean analog power rail $VDDA$ for the sensitive blocks, such as the transmitter VCO and the intraocular pressure sensor, which can be significantly affected by supply voltage variations. The
LDO schematic is shown in Fig. 3.11. In this work, LDO is operating on the $VDD$ full input range ($1V - 1.6V$) to supply a constant output voltage $VDDA = 1V (+/ - 0.1)$ with a line regulation of $30mV/V$ when it is loaded by $0.5mA$ and with a load regulation of $15mV/0.5mA$. A load condition of $0.5mA$ is considered for the VCO transmitter and the sensing circuits during the LDO design process.

Low quiescent currents $I_Q = 2\mu A$ and $3.7\mu A$ are internally consumed by LDO at input voltages of $VDD = 1.1$ and $1.6V$, respectively (with load condition $= 0.5mA$). The simulated quiescent current $I_Q$ and LDO output voltage $VDDA$ are shown in Fig. 3.12. To cut down this quiescent current from the standby current, LDO has been designed to be completely switched off during charging mode. This switching is achieved by the “enable” signal applied to M6, M7, M8 in Fig. 3.11. This enable signal is raised high only when the input VDD charged to a sufficient level for the LDO to work properly. To generate this signal, a voltage sensor has been designed with a specific hysteresis and will be discussed in the following subsection. LDO stability analysis resulted in a gain margin of $35.6 \text{ dB}$ at $f = 12.7MHz$ and a phase margin of $76.65 \text{ (deg)}$ at $f = 804kHz$ at input voltage $VDD$ of $1.2V$ and load condition of $0.5 \text{ mA}$.

### 3.3.4 Voltage Sensors

In order to enable power management for the complete SoC, voltage sensors are utilized to generate power good signals. These signals are raised high when the main power rail VDD is charged to a level sufficient for the system components. The system remains in sleeping (charging) mode until it receives these power good signals. When these signals are received, the system moves to the active mode. For stable transitions between these modes, the voltage sensor is required to have hysteresis thresholds (i.e., different high level input voltage $[V_{IH}]$ and low level input voltage $[V_{IL}]$. This is
Figure 3.11 – Low Dropout Regulator Schematic

Figure 3.12 – Simulated Quiescent Current ($I_Q$) and Dropout Voltage ($V_{do}$)
Figure 3.13 – VDD and VDDA Voltage Sensors Schematic
to avoid system instability, which can take place by moving back and forth to the charging mode. Two different voltage sensors have been designed to generate two separate power good signals (VDD_GD and VDDA_GD). Schematics of the voltage sensors are shown in Figs. 3.13a and 3.13b. The VDD_GD signal is the main power good signal for the entire system and its range is $V_{IH} = 1.2\,V$, $V_{IL} = 0.8\,V$, while the VDDA_GD signal is generated to enable the LDO as discussed in subsection 3.3.3, and it has a narrower hysteresis of $V_{IH} = 1\,V$, $V_{IL} = 0.925\,V$.

### 3.4 Experimental Results

The on-chip RF power harvesting module is implemented in 0.18µm CMOS with a chip size equal to $1.5 \times 3.2\,mm^2$. The chip microphotograph is shown in Fig. 3.14. Both DC and RF measurements have been performed and are discussed in the following subsections.

#### 3.4.1 Test Setup to Emulate Eye Environment

A custom setup is designed to mimic the real operation of the sensor inside the human eye, as illustrated in Fig. 3.15. The chip is designed to be tested through 5mm of saline solution and 10cm of air. This medium emulates the attenuation from aqueous
Figure 3.15 – A cross sectional view of the implantable IOP monitoring SoC test setup mimicking the anterior chamber of the eye. [1,3]

humor in the eye and the distance from the eye to the external reader. The chip is wire bonded to a custom designed PCB and coated with 20µm thick Parylene-C, which is a widely used organic bio-compatible organic material. The chip is then immersed into a (1 × 1 × 0.5 cm³) Plexiglass cavity, filled with saline solution with ε_r = 68 at 5.2 GHz which is similar to that of the aqueous humor in human eye [93,94]. All of the materials utilized for test setup design including PCB (Rogers Duroid RT5880, ε_r = 2.2), Plexiglass (ε_r = 2.2), and Parylene-C (ε_r = 2.9) have low dielectric constants to have a minimal effect on the high-frequency test environment.

3.4.2 DC Measurements

On-chip DC measurements have been done using a micro probe-station for the LDO and the two voltage sensors. The results validate the proper operation of these circuits. The regulated output voltage of the LDO (VDDA) versus the unregulated voltage rail (VDD) is shown in Fig.3.16. The voltage sensor control signal (VDDA_GD) is also measured versus the unregulated input VDD, and it is shown as a dotted line in Fig. 3.16. As discussed before in subsection 3.3.4, VDDA_GD is used as an
enable signal for the LDO to disable it during the charging mode. This saves the LDO’s quiescent current. VDDA_GD is raised high when the VDD is sufficient for the LDO to generate 1 V. As shown in Fig. 3.16, when VDDA_GD raised high, the LDO provides a regulated VDDA of 1 V (+/-0.1). It is to be noted that VDDA_GD high value equals the VDD (not VDDA) as the voltage sensor itself is supplied from the unregulated voltage (VDD).

In order to test the voltage sensors’ thresholds (high level input voltage \([V_{IH}]\) and low level input voltage \([V_{IL}]\)) and their hysteresis, a ramp input voltage is supplied to the VDD power rail, and the voltage sensor outputs are measured and plotted in Fig. 3.17. The measured thresholds for VDD_GD are \(V_{IH} = 1 \text{ V}, V_{IL} = 0.740 \text{ V}\), while the measured hysteresis for the VDDA_GD is narrower as designed for the sensitive analog power rail VDDA with \(V_{IH} = 1.14 \text{ V}\) and \(V_{IL} = 0.960 \text{ V}\).

3.4.3 RF Measurements

RF measurements have been conducted in the proposed bio-environment test setup as previously explained before in section 3.4.1. The implemented test setup is shown in Fig. 3.18 where the chip is wire bonded to the Duroid PCB and immersed in a Plexiglass box filled with a saline solution. The on-chip antenna is immersed in the saline solution, thus it can not be directly accessed with RF probes.

For antenna testing, a PCB balun has been implemented to feed the differential on-chip antenna from an SMA connector, as shown in Fig. 3.18. The simulated and measured S11 for the on-chip antenna is shown in Fig. 3.19. For this antenna testing, the on-chip metal wires between the on-chip antenna and the harvester circuits have been cut using a focused ion beam (FIB).

A microstrip patch antenna (with 5 dB gain) is used as a transmitting antenna to wirelessly power the whole immersed on-chip module (on-chip antenna and rectifier).
Figure 3.16 – Measured VDDA (the LDO output) and VDDA_GD versus the input VDD

Figure 3.17 – Measured VDDA_GD and VDD_GD versus the varying input VDD
The available power at the top of the immersed on-chip antenna \( P_{\text{available}} \) can be calculated by equation (3.5):

\[
P_{\text{available}} = P_t G_t \left( \frac{\lambda}{4\pi R} \right)^2 \tag{3.5}
\]

where \( P_t \) is the transmitted RF signal power, \( G_t \) is the transmitting antenna gain =5 dB, \( \lambda=5.765 \) cm, and \( R \) is the communication distance between transmitting antenna and the immersed on-chip antenna.

Using variable \( P_t \) and fixing the communication distance, the wirelessly harvested DC voltage (VDD) is plotted in Fig 3.20 versus \( P_{\text{available}} \). Then, the communication distance is tested using constant \( P_t=35 \) dBm. The immersed on-chip power harvesting module was able to charge the on-chip storage capacitor \( (C_L = 5nF) \) and build up VDDs of 1.15V and 560mV at distances of 3cm and 10cm, respectively. Different wirelessly charging cases are shown in Fig. 3.20 for different communication distances.
Figure 3.19 – (a) Simulated and measured S11 and (b) 2D normalized far-field radiation pattern when the chip is immersed in saline solution and wirebonded to PCB [2] of [3, 7 and 10cm]. These measurements demonstrate that the proposed on-chip power harvester is able to wirelessly charge to 1.0V from a transmitter with an EIRP of 5W (37dBm) at a distance of 3cm (which corresponds to 200mW available power at the immersed antenna).
Figure 3.20 – Measured harvested DC voltage (VDD) versus the available power to the on-chip antenna (wireless powering)
Figure 3.21 – Measured harvested VDD charging wirelessly versus different distances (wireless powering)
Figure 3.22 – Output voltage for two input power levels relative to other reported RF power harvesters

Figure 3.23 – Efficiency for two input power levels relative to other reported RF power harvesters
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*a* simulated  
*b* calculated  
*c* including on-chip antenna  
*d* estimated based on published data  
*e* very low loss assumed in [95]
Chapter 4

Self-Biased Differential Rectifier with Enhanced Dynamic Range

4.1 Introduction

The RF-to-DC power-converter is the core of any wireless power receiver which supplies usable DC power out of the incoming RF power to the antenna, as shown in Fig.4.1. The wireless power receiver of the IOPM proposed in Chapter 3 utilizes a fully cross-coupled (FX) rectifier as an RF-to-DC power converter. Due to its sensitivity at low RF power levels, the FX rectifier is commonly used in RFIDs and wirelessly powered sensors [38,39] instead of diode-connected rectifiers. However, the FX rectifier suffers from a high reverse leakage, which rises at high RF power levels and degrades its RF-to-DC power conversion efficiency. As a result, the input dynamic range for efficient power conversion becomes narrower than that of diode-connected rectifiers [38].

In this chapter, we propose and experimentally validate a self-biased, cross-coupled, differential CMOS rectifier with enhanced efficiency over wider input range than both diode-connected and cross-coupled rectifiers [41]. This facilitates reliable and efficient RF-to-DC power conversion at varying RF power levels, and thus adds more spatial freedom (in distance and orientation) between the wireless power transmitter and receiver, allowing for reliable wireless power transfer in harsh conditions and unstable environments.
Prior RF-to-DC power converter architectures are discussed in Section II and the proposed architecture is illustrated along with its operational concept in Section III. In Section IV, the experimental results are discussed and compared with measurements of a fabricated conventional rectifier. Finally, the conclusion is drawn in Section V.

4.2 RF-to-DC power converters

The RF-to-DC power converter performance is evaluated in terms of two main parameters: 

a) sensitivity, which defines the minimum input RF power required to generate a specific DC output voltage, and

b) power-conversion efficiency (PCE), which is the ratio of the usable output DC power, $P_o$, to the input RF power, $P_i$, and can be expressed by (1):

$$PCE = \frac{P_o}{P_i} = \frac{P_o}{P_o + P_{diss} + P_{r_{us}}}, \quad (4.1)$$

Where the input power, $P_i$, equals the summation of the output DC power, $P_o$, the dissipated power in rectifying devices, $P_{diss}$, and the reverse-leakage power, $P_{r_{us}}$, which is caused by the non-idealities in the reverse characteristic of the rectifying
Traditionally, AC-DC power converters were realized using diode-based architectures, such as the Greinacher cell, the Dickson multiplier [60], or a full-wave bridge rectifier [99]. Diode-based rectifiers were simply implemented in CMOS technology using diode-connected transistors, such as the Dickson rectifier shown in Fig. 2a. However, they suffer from poor sensitivity at low input power and from high dropout voltage that degrades their power conversion efficiency at mid-high input power. Enhanced sensitivity can be achieved either by using Schottky diodes that require additional fabrication steps and hence are seldom offered in conventional CMOS processes, or by using integrated step-up transformers occupying a large area [100]. On the other hand, the differential, fully cross-coupled (FX) rectifier [38], shown in Fig. 4.2b, is widely used in RFID applications due to its improved sensitivity and high peak efficiency. However, this improvement is gained at the expense of the reverse characteristic of the rectifying devices, as the rectifying cross-coupled transistor is still a bidirectional
device—unlike diodes or diode-connected transistors. Hence, it conducts in a reverse direction once the instantaneous value of the RF signal, $V_{RF}$, becomes lower than the output DC voltage, $V_{DD}$, in every RF cycle, as shown in Fig.4.3a. This periodic reverse leakage is exacerbated as the RF power level grows, degrading the rectifier conversion efficiency at high input power, as shown in Fig.4.3b. Consequently, the rectifier operates efficiently within a limited range of input power. To evaluate different rectifier architectures, a dynamic range is defined as the input-power range at which the rectifier maintains PCE higher than 80% of its peak efficiency [101].

In [80,102], a low MHz adaptive architecture reconfigures the rectifier stage as a diode-connected voltage doubler or as a half cross-coupled rectifier based on the input power level. However, it requires active diodes driven by fast comparators that are not power efficient at high RF frequencies, i.e. UHF 433MHz or higher. A multistage configuration is presented in [101,103] to enhance the efficiency of the cross-coupled rectifier by rewiring stages as a series or parallel multistage rectifier. Although this technique extends the efficiency of the cross-coupled rectifier over a wide range of input power, it requires multiple stages with high input capacitance and low input
resistance, thus complicating the matching network design. In [104], an adaptive offset calibration technique is presented to compensate for the threshold voltage, $V_{th}$, in the diode-based rectifiers to improve their sensitivity. However, it requires two more auxiliary, multistage rectifiers to compensate the $V_{th}$ of the main rectifier. Thus, the total architecture occupies a large area, adding more losses, and degrading the PCE.

### 4.3 Proposed RF-to-DC Power Converter

#### 4.3.1 Proposed Architecture

A schematic of the proposed self-biased cross-coupled rectifier is shown in Fig. 4.4. The rectifier utilizes the cross-coupled configuration with the differential-drive capability to maintain good sensitivity at low input power by operating in the linear region and holding low dropout voltage. Moreover, a self-biasing mechanism is added to limit the reverse leakage at the sense of high input power. The proposed self-biasing
mechanism controls the conduction of the rectifying devices by raising their effective turn-on voltage at high RF power levels.

A simple implementation of this mechanism is achieved by applying the output DC voltage ($V_{DD}$) directly to the controlling gates of the rectifying transistors (MP1,2) without disturbing the RF signal at the differential inputs. This is accomplished by decoupling the DC voltage of the rectifying PMOS MP1,2 gates apart from their corresponding NMOS MN1,2 using CP3,4 and then applying the DC self-bias using an RF choke (RFC) coil that is DC short circuit and AC open circuit.

It is worth noting that the self-biasing branch is connected to a MOSFET gate; hence, no DC current passes through it, whereas the self-biasing RFC branches can be simply replaced by high feedback resistors ($R_{FB1}$, $R_{FB2} \sim 100k\Omega$) without loading the RF inputs, as shown in Fig.4.4. Similar to the standard RF choke circuit, the feedback resistor is an RF open circuit, due to its relatively large value, and a DC short circuit due to the fact that no current flows in the resistor.

The equivalent circuits of the proposed rectifier at DC and RF are shown in Figs. 4.5a and 4.5b, respectively. At steady state, RFB passes the output DC voltage
Figure 4.6 – Operating point of the rectifying device (MP1) configured (a) as a diode-connected transistor (Dickson rectifier); (b) as a cross-coupled transistor; and (c) as a self-biased transistor (proposed rectifier).

(labeled VDD) to the gate, since no DC current flows to the MOSFET gate nor through the coupling capacitors, as shown Fig.4.5a. On the other hand, the large feedback resistor, ideally, has no effect on the RF operation, as shown in Fig.4.5b.

4.3.2 Operational Concept

The operating point of the proposed self-biased cross-coupled rectifying device is compared to the conventional cross-coupled and diode-connected rectifying devices in Fig.4.6. Each rectifying device connects the AC-coupled RF node (RF superimposed on a common mode $V_{CM} = V_{DD}/2$) at its input terminal to the output $V_{DD}$ point. As shown in Fig.4.6a, the gate and drain of the diode-connected device are tied to the output $V_{DD}$ to act as a two-terminal diode. In the case of the conventional cross-coupled device, the gate is attached to the $RF_N$ node ($= -V_{RF}/2$ superimposed on $V_{DD}/2$), as shown in Fig.4.6b. However, in the proposed self-biased cross-coupled device, the gate $RF_N$ signal is superimposed on $V_{DD}$, as shown in Fig.4.6c. Note that both the proposed self-biased cross-coupled device and the diode-connected device need minimum turn-on RF voltage, $V_{RFmin}$, equal to threshold voltage, $V_{th}$, plus $V_{DD}/2$. This is unlike the conventional cross-coupled device, which requires $V_{th}$ only.
Moreover, the proposed device conducts in the linear region and holds a dropout voltage of less than or equal to its overdrive voltage, $V_{\text{eff}}$. Thus, it passes a higher output voltage than the diode-connected device, which requires a dropout of $V_{\text{th}}+V_{\text{eff}}$. As a result, the proposed self-biased cross-coupled device retains moderate sensitivity (i.e. it generates a higher output voltage at the same RF input power) compared to the diode-connected device. This is derived from the operating points shown in Fig.4.6, and it matches the simulated dropout voltages ($V_{SD}$) of the three rectifiers at the same input power, as shown in Fig.4.7a.

During the periodic RF signal transitions, the reverse leakage of the diode-connected device is negligible, while the conventional cross-coupled device is strongly biased by $V_{SG(RVS)} = V_{RF}/2 + V_{DD}/2$ in the reverse direction, as derived from Fig.4.6. Accordingly, the reverse current lobes increase, as shown in Fig.4.7b. On the other hand, as depicted in Fig.4.6, the proposed device is biased only at $V_{SG(RVS)} = V_{RF}/2$, leading to reduced reverse current lobes, as shown in Fig.4.7b. It worth noting that, during the negative RF half cycle, the gate of the MP1 in the conventional FX and proposed rectifiers is positively biased, shutting down its current completely, similar to the reverse-biased, diode-connected device.

Fig.4.8a shows the simulation of the output voltage versus the input power for all three rectifiers for a load of 50 kΩ. At low RF power, the proposed rectifier outperforms the Dickson rectifier and outperforms the FX rectifier at high RF power. This can be explained by plotting both the forward harvested charges and the reverse leakage charges per RF cycle ($T_{RF\text{ cycle}}$) at three distinct RF power levels, as shown in Fig. 4.8b. As indicated on top of each bar, the net forward charges ($\Delta Q_f$) are equal for architectures that produce the same output voltage ($V_o$) for specific load ($R_L$), thus:

$$\Delta Q_f = \frac{V_o}{R_L} \times \frac{T_{RF\text{ cycle}}}{2}.$$  \hspace{1cm} (4.2)
Figure 4.7 – Simulation of (a) the dropout voltage ($V_{SD}$), and (b) drain current ($I_{DP}$) in the rectifying PMOS devices of the Dickson, conventional FX, and proposed rectifiers at $37\mu W$ input power level.
Figure 4.8 – (a) Simulated output voltage, (b) alternating charges flowing into MP1 per RF cycle (Qp), and (c) power conversion efficiency (PCE) for the Dickson, conventional FX, and proposed rectifiers versus RF input power.
Obviously, at mid-power level, the proposed rectifier provides more net charges (thus higher output voltage) than the other two rectifiers.

The simulated PCE of the three rectifiers versus input power is plotted in Fig 4.8c. As shown in Fig. 4.8, the conventional FX rectifier has a peak PCE at low RF power, but it falls off rapidly due to its high reverse leakage current, which is shown in Fig. 4.7b. On the other hand, the Dickson (diode-based) rectifier displays a moderate PCE at the high RF power levels, but suffers from poor efficiency at low input power due to its high dropout voltage (shown in Fig. 4.7a). Conversely, the proposed rectifier achieves wider dynamic range with a slight decrease in its peak PCE relative to the conventional FX rectifier.

During start up, the output voltage \(V_{DD}\) charges the PMOS gate (the adaptive bias node) through the feedback resistors \(R_{FB}\) with a time constant \(\tau_{bias}\) calculated as:

\[
\tau_{bias} = R_{FB} \times (C_{gs_{PMOS}} / \parallel C_p).
\]  

Where \(-C_{gs_{PMOS}}\) is the PMOS gate capacitance in order of \(fF_{arads}\), while \(C_p\) is the coupling capacitor in order of one \(pF_{arads}\). For proper operation, the time constant, \(\tau_{bias}\) should be smaller than the output charging time constant, \(\tau_{charging}\), given as:

\[
\tau_{charging} = R_{out} \times C_L.
\]  

Where \(C_L\) is the load/storage capacitance and \(R_{out}\) is the driving output resistance of the rectifying device. For most applications the load/storage capacitance, \(C_L\), is in order of nF (on-chip) or \(\mu F\) (off-chip). Thus, for a typical rectifier circuit, it is guaranteed that the \(\tau_{charging} \gg \tau_{bias}\). At the same time, the feedback resistance is too high (almost open circuit) for the RF signal coming through the coupling capacitor \(C_p\), as shown in the RF equivalent circuit in Fig. 4.5b. Hence, the RF signal at the
PMOS gate is isolated from the loading at the output node.

Furthermore, the transient simulation of the output charging of the proposed and conventional FX rectifiers to the same DC voltage is shown in Fig. 4.9a for a load capacitance of 0.5\text{nF} and in Fig.4.9 for 0.1\text{nF}. It is worth mentioning that during the start-up time, as the output voltage $V_{DD}$ grows, the conductance of the rectifying device decreases (intentionally to limit the reverse leakage), and the output resistance $R_{out}$ increases as follows:

$$R_{out_{\text{pmos}}} = \frac{1}{K_p W/L (V_{RF} - V_{DD}/2 - V_{th})} \quad (4.5)$$

Consequently, the output charging time for the proposed rectifier becomes longer than the conventional rectifier at the high output voltage (i.e. high input RF power levels), as shown in Fig.4.9a and 4.9b. This delay is strongly dependent on the output voltage (and thus the output resistance $R_{out}$) rather than the feedback resistance $R_{FB}$. Note that the proposed rectifier manages to reach the same output voltage at lower than half the input RF power needed by the conventional rectifier, as indicated in the legend of Figs.4.9a and 4.9b.

A comparison of the three rectifying devices is summarized in Table I, where the proposed self-biased rectifying device shows a competitive advantage of low dropout voltage, as shown in Fig.4.7a. Hence, the proposed rectifier has low dissipation loss and better sensitivity than the diode-connected device. At the same time, the proposed rectifying device shows lower reverse leakage and wider input range than the conventional cross-coupled device, as shown in Fig.4.7b and 4.8 respectively.
Figure 4.9 – Transient simulation of the charging time of the proposed (solid) and conventional FX (dashed) rectifiers for load capacitances (a) $0.5\text{nF}$ and (b) $0.1\text{nF}$. 
Table I
Comparison Of Rectifying Devices

<table>
<thead>
<tr>
<th>Rectifier</th>
<th>Dickson</th>
<th>Conv. FX</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>D-connected</td>
<td>X-coupled</td>
<td>Self-biased</td>
</tr>
<tr>
<td>Turn-on (^1) ((V_{RF\text{min}}))</td>
<td>High ((=V_{DD}/2+V_{th}))</td>
<td>Low ((=V_{th}))</td>
<td>High ((=V_{DD}/2+V_{th}))</td>
</tr>
<tr>
<td>Dropout (^2) ((V_{\text{drop}}))</td>
<td>High (Sat.) ((=V_{th}+V_{\text{eff}}))</td>
<td>Low (Linear) ((=V_{\text{eff}}))</td>
<td>Low (Linear) ((=V_{\text{eff}}))</td>
</tr>
<tr>
<td>Sensitivity (^3)</td>
<td>Negligible</td>
<td>High, (I_d) (\text{MOS})</td>
<td>Low</td>
</tr>
<tr>
<td>RVS leak</td>
<td>Negligible leak (V_{RF}&gt;V_{\text{breakdown}})</td>
<td>Wide leak (2V_{th}&gt;V_{DD}&lt;V_{RF})</td>
<td>Low leak (2V_{th}&lt;V_{RF})</td>
</tr>
<tr>
<td>RVS Leakage Range (^4)</td>
<td>(V_{RF}&gt;V_{\text{breakdown}})</td>
<td>(&lt;V_{RF}&lt;V_{DD})</td>
<td>(V_{RF}&lt;V_{DD})</td>
</tr>
<tr>
<td>Efficiency (PCE)</td>
<td>Low peak</td>
<td>High peak</td>
<td>Good peak</td>
</tr>
<tr>
<td></td>
<td>Moderate-range</td>
<td>Narrow-range</td>
<td>Wide-range</td>
</tr>
</tbody>
</table>

\(^1\) Turn-on at \(V_{SG}>V_{th}\).

\(^2\) Dropout affects sensitivity, output voltage and efficiency.

\(^3\) Sensitivity: turn on at low \(V_{RF}\) & with low dropout voltage.

\(^4\) Reverse leakage if \((V_{SG,RVS}>V_{th})\) \& \((V_{SD,RVS}>0)\).
4.4 Prototyping and Measurements

The proposed rectifier is implemented in 0.18\(\mu\)m CMOS process technology and occupies 130\(\mu\)m \(\times\) 130\(\mu\)m active area (the die microphotograph is shown in Fig.4.10). A conventional FX rectifier is implemented on the same die for a fair comparison to the proposed rectifier using identical test setup and conditions. The RF measurement setup includes Agilent’s vector network analyzer (N5225A) and a digital multimeter (34420A). The rectifier’s power conversion efficiency (PCE) is measured with a single tone, a 433MHz signal at different input power levels, and the output DC voltage is recorded.
4.4.1 Measurement methodology

The rectifier chips are directly probed using differential microwave probes (GSGSG) and characterized using the RF test setup shown in Fig. 4.11. An Agilent’s 2-port vector network analyzer (VNA - N5225A) is used to measure the input reflection coefficient \((S_{11})\) of the rectifier under test at different input RF-power levels \((P_{RF})\) and at multiple-frequency \((f_{RF})\) sweeps. For each operating point, a single tone of specified frequency \((f_{RF})\) and RF power level \((P_{RF})\) is fed into the rectifier differential input, while the output DC voltage is recorded using an Agilent’s 7½-digits voltmeter (34420A). In order to convert the VNA single-source output into a differential signal, a Mini-Circuits’ coaxial RF-power splitter/combiner (2-Way, 180° BALUN) is utilized with the appropriate frequency band. Moreover, a programmable resistance substituter (IET PRS-202W) is used as a predefined load \((R_L)\) for the rectifier under test as a third parametric sweep.

4.4.2 Measurement Steps

Probe calibration:

First, the GSGSG differential probe is planarized to maintain all tips lying in the same horizontal plane (i.e. they are capable of landing together on the corresponding five pads). This is done by landing (and lifting) the probe, carefully, on a standard, gold-plated contact substrate, and adjusting the probe vertical rotation with the aid of the marks of the probe tips, as shown in Fig. 4.12b. Second, a short-open-load (SOLT without “through” for single-port measurement) calibration is performed at the probe tips using impedance standard substrates \((ISS)\) to define the RF reference plane for S-parameters measurements. After calibrating the probe, it is very important to re-

\[1\] The linear mode equation is used for the forward conduction (the charging interval in every RF cycle).
measure the *ISS* standard 'short', 'load’, and 'open' (or open air) to guarantee a minimum error and so the best measurement resolution.

**Measuring the input S-parameter and output DC voltage**

After landing the RF- and DC-probes over the device under test (DUT), the resistive load \( R_L \), the VNA RF frequency \( f_{RF} \) and power level \( P_{RF} \) are set and switched on. Then, the input S-parameter \( S_{11} \) and output DC voltage \( V_o \) are recorded for the DUT. In order to fully characterize all rectifiers under test, both \( S_{11} \) and \( V_o \) are recorded for each rectifier architecture at different RF-power levels and at multiple frequencies for different loads.

Hence, the RF-testing setup (shown in Fig. 4.11) is automated to accelerate the measurement data acquisition for each DUT over three parametric sweeps (input RF power, frequency, and load), as shown in the following algorithm and the flowchart in Fig. 4.13.
Figure 4.13 – Simplified program flowchart of the automated RF testing
Algorithm 4.1 Automation code to control the test equipment

Set \( R_L \)

Preset \( VNA \)

Load \( calset \); calibration setting

Set \( P_{RF}, f_{RF} \)

Get \( V_o \)

Get \( S_{11} \)

Save on disk

Deducing the power conversion efficiency

In order to calculate the RF-to-DC power conversion efficiency (PCE) of the rectifier under test, the actual input power to the rectifier \( (P_{in}) \) is calculated using the following equation 4.6:

\[
P_{in}(dBm) = P_{source}(dBm) - L_{cable}(dB) - 10 \log |S_{ds}|^2 - 10 \log |S_{11_{rec}}|^2 \tag{4.6}
\]

Where \( P_{source} \) is the output RF-power of the VNA port, \( L_{cable} \) is the single-ended cable loss, and \( S_{ds} \) is the characterized mixed-mode (single-to-differential) S-parameter of the BALUN (plus its attached differential cables). \( S_{11_{rec}} \) is the measured S-parameter (voltage reflection coefficient) of the rectifier input at the probe tips (i.e. the calibrated reference plane). \( S_{ds} \) represents the transmission losses (including single-to-differential gain/phase imbalance) through the BALUN (plus its output differential cables) and is calculated with equation:

\[
S_{ds} = \frac{1}{\sqrt{2}} (S_{21} - S_{31}) \tag{4.7}
\]

Where \( S_{21} \) and \( S_{31} \) are the characterized insertion losses of the (differential) output ports of the BALUN (port 2 and 3, respectively).

The output power is directly calculated by utilizing the measured output DC-
Figure 4.14 – Measured PCE of the proposed (solid) and conventional FX (dash) rectifiers versus input power for three loads.

After de-embedding the reflection and transmission losses, the net input power \( P_{in} \) is calculated using equation 4.6 and the power conversion efficiency for the proposed and conventional rectifiers is plotted in Fig.4.14 versus the input power at different

\[
P_o = \frac{V_o^2}{R_L}
\]  

(4.8)

\[
PCE = \frac{P_o}{P_{in}}
\]  

(4.9)

4.5 Results and Discussion (Data analysis)

After de-embedding the reflection and transmission losses, the net input power \( P_{in} \) is calculated using equation 4.6 and the power conversion efficiency for the proposed and conventional rectifiers is plotted in Fig.4.14 versus the input power at different
loads. Although the proposed rectifier has a lower peak PCE ($\approx 65\%$) than the conventional rectifier, whose peak PCE $\approx 75\%$, the proposed architecture maintains its power conversion efficiency over a broader dynamic range of input power. Thus, the proposed rectifier can operate efficiently at different RF power levels, enabling robust wireless powering from varying transmission distances or within unstable environments. Fig.4.15 depicts the measured output DC voltage versus input power level for the proposed and conventional FX rectifiers equally loaded by 50k, 100k, and 200k $\Omega$ resistors. With the same input power, the proposed self-biased rectifier delivers a higher DC output voltage than the conventional FX rectifier by 20% to 30%.

To elucidate the relative PCE enhancement of the proposed rectifier, the ratio of the proposed rectifier PCE over the conventional FX rectifier PCE is plotted in Fig.4.16a for variable loads $R_L = 50k$, 100k, and 200k $\Omega$. Approximately 40% to 70%
Figure 4.16 – (a) Measured ratio of the proposed rectifier PCE relative to the conventional FX rectifier PCE for three different loads, and (b) measured dynamic range of the proposed and conventional rectifiers.
efficiency improvement is achieved in the proposed rectifier at mid-high input power relative to the conventional FX rectifier, as shown in Fig. 4.16a. Moreover, the proposed rectifier maintains the achieved improvement of PCE over a wide input range at different loading conditions, as depicted in Figs. 4.14 and 4.16a. To further illustrate this point, the dynamic range of input power $[P_{\text{min}} \text{ to } P_{\text{max}}]$ at which the rectifier maintains 80% of its peak efficiency is represented as the ratio of $P_{\text{max}}$ over $P_{\text{min}}$ and is compared in Fig. 4.16b for the proposed and conventional FX rectifiers versus different loading conditions. Evidently, the proposed rectifier achieves a higher dynamic range across a wide range of loading conditions (from 30$k$ to 300$k$ $\Omega$).

Unlike conventional rectifier impedance which varies significantly versus different RF power levels, the input impedance of the proposed rectifier is more stable than the conventional rectifier versus RF power variations, as shown in Figs. 4.17 and 4.18. Therefore, a wide-range matching network can be easily achieved for the proposed rectifier impedance. Consequently, the mismatch loss due to impedance nonlinearity is suppressed in the proposed rectifier relative to the conventional rectifier.

A performance comparison of the proposed rectifier versus recent ISM 433MHz rectifiers is summarized in Table 4.2. The proposed rectifier shows $2 \times$ improvement in dynamic range and $5 \times$ enhancement in efficiency relative to [105]. More than a 50% wider dynamic range and doubled efficiency is achieved compared to [104] with a $9 \times$ chip area saving.

### 4.6 Conclusion

In this chapter, we propose a self-biased, cross-coupled, differential rectifier with 50% enhanced power conversion efficiency over a wide range of input power levels and
Figure 4.17 – Measured input (series) resistance of the proposed and conventional FX rectifiers at 433MHz versus RF input power for various loads.

Figure 4.18 – Measured input (series) capacitance of the proposed and conventional FX rectifiers at 433MHz versus RF input power for various loads.
Table 4.2 – Self-biased rectifier performance summary and comparison.

<table>
<thead>
<tr>
<th>Ref</th>
<th>CMOS Process</th>
<th>Architecture</th>
<th>stages</th>
<th>Area (mm²)</th>
<th>Freq. (Hz)</th>
<th>Sensitivity&lt;sup&gt;a&lt;/sup&gt;</th>
<th>Load R&lt;sub&gt;L&lt;/sub&gt;(Ω)</th>
<th>Peak PCE</th>
<th>Dyn.Range&lt;sup&gt;c&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work</td>
<td>0.18µm</td>
<td>Self-biased cross-coupled rectifier (Proposed)</td>
<td>1-stage</td>
<td>0.017</td>
<td>433M</td>
<td>-15.2</td>
<td>50 k</td>
<td>65.3 %</td>
<td>6.5</td>
</tr>
<tr>
<td>This Work</td>
<td>0.18µm</td>
<td>Fully cross-coupled (FX) rectifier (Conventional)</td>
<td>1-stage</td>
<td>0.005</td>
<td>433M</td>
<td>-13.6</td>
<td>50 k</td>
<td>77 %</td>
<td>4.5</td>
</tr>
<tr>
<td>[105]</td>
<td>0.18µm</td>
<td>Fully cross-coupled with inter-stage RF injection</td>
<td>3-stage</td>
<td>0.088</td>
<td>433M</td>
<td>-7.8</td>
<td>30 k</td>
<td>13.2 %</td>
<td>3.2</td>
</tr>
<tr>
<td>[104]</td>
<td>0.18µm</td>
<td>Dickson rectifier with multiple-V&lt;sub&gt;th&lt;/sub&gt; offset cancellation.</td>
<td>4-stage</td>
<td>0.15</td>
<td>433M</td>
<td>-11.2</td>
<td>50 k</td>
<td>32 %</td>
<td>4.2</td>
</tr>
<tr>
<td>[106]</td>
<td>0.18µm</td>
<td>Hybrid V&lt;sub&gt;th&lt;/sub&gt; cancellation using RF input &amp; DC output voltage</td>
<td>1-stage</td>
<td>NA</td>
<td>433M</td>
<td>&gt; 0&lt;sup&gt;b&lt;/sup&gt;</td>
<td>30 k</td>
<td>12.5 %</td>
<td>3.3</td>
</tr>
</tbody>
</table>

<sup>a</sup> P<sub>RF</sub> @ V<sub>o</sub> = 1V  
<sup>b</sup> 0 dBm for V<sub>o</sub> = 0.78V.  
<sup>c</sup> Input power range of PCE≥0.8 Peak PCE.
under different loading conditions. A sensitivity of (Pin=30µW at Vo=1V) and peak power conversion efficiency (peak PCE=65.3%) are achieved for a 50kΩ load. The architecture of the proposed rectifier is presented, and its performance is compared to the conventional, cross-coupled rectifier.
Chapter 5

Wide-Range Adaptive RF-to-DC Power Converter for UHF RFIDs

5.1 Introduction

The self-biased rectifier proposed in Chapter 4 achieves a dynamic range wider than conventional rectifiers by more than 50%; however, it suffers from two limitations. First, the PCE peak is lower than that of the conventional FX rectifier, as presented in the results in Chapter 4. This is due to self-biasing, used to limit the reverse leakage, which is always applied to the rectifying devices even at low RF power levels. Hence, the minimum turn-on voltage required to operate the rectifier increases, degrading its sensitivity to low RF power levels. Second, the parasitic capacitances attached to the on-chip feedback resistors reduce the rectifier efficiency in the sub-GHz range and beyond.

In this chapter, we propose a wide-range, differential RF-to-DC power converter using an adaptive, self-biasing technique. The proposed architecture extends the optimal input range at which the rectifier maintains 80% of its peak power conversion efficiency over a wider input range compared to conventional rectifiers. Unlike the continuously self-biased rectifier proposed in Chapter 4, this adaptive self-biased rectifier extends the dynamic range while maintaining both the high PCE peak and the sensitivity advantage of the conventional cross-coupled scheme (shown in Fig. 5.1a). In this chapter, Section II describes the proposed adaptive rectifier design, the exper-
Figure 5.1 – (a) Schematic of a single-stage, conventional cross-coupled rectifier and (b) its power conversion efficiency versus RF input power.

Experimental results are presented in Section III, and the conclusion is drawn in Section IV.

5.2 Self-Adaptive Rectifier

A schematic of the proposed adaptive rectifier is shown in Fig. 5.2. Its operation principle is based on limiting the conduction of the rectifying devices at a high input power range at which the reverse leakage becomes severe. This is achieved by raising the DC bias of the rectifying transistors (MP1,2) gates as the input RF power increases. The proposed rectifier is comprised of four driving MOSFETs (MP1,2 and MN1,2), as rectifying devices, that are connected in a fully, cross-coupled manner to enhance the rectifier sensitivity. However, unlike the conventional cross-coupled rectifier shown in Fig. 5.1, the DC voltage of the gates of the MP1,2 are decoupled from their corresponding NMOS gates, while the AC voltages of the PMOS gates are coupled to the corresponding AC voltage of NMOS gates via two pumping capacitors CP3,4.

To control the conduction of the rectifying devices, a self DC biasing is dynamically
applied to the PMOS gates only in the presence of high input RF power. The output charging current \( I_{Dp} \) and output resistance \( R_{out} \) of the rectifying device can be expressed by equations 5.1 and 5.2, respectively.

\[
I_{Dp} = \begin{cases} 
K_p \frac{W}{L} (V_{RF} - V_{\text{th}}) V_{sd} & ; \text{at low RF power.} \\
K_p \frac{W}{L} (V_{RF} - V_{DD}/2 - V_{\text{th}}) V_{sd} & ; \text{at high RF power.}
\end{cases}
\]

\[
R_{out\, pmos} = \begin{cases} 
\frac{1}{K_p \frac{W}{L} (V_{RF} - V_{\text{th}})} & ; \text{at low RF power.} \\
\frac{1}{K_p \frac{W}{L} (V_{RF} - V_{DD}/2 - V_{\text{th}})} & ; \text{at high RF power.}
\end{cases}
\]

As the output voltage VDD grows, the conductance \( G_p \) of the rectifying device decreases (intentionally to limit the reverse leakage) and the output resistance \( R_{out} \) increases, as expressed by equation 5.2, only at high RF power levels. On the other

\[1\text{The rectifying device operates in linear mode during the charging interval of every RF cycle at mid-high RF power levels.}\]
hand, at low RF power levels, the rectifier maintains just as high a conduction current as the conventional rectifier.

While this dynamic self-biasing can be implemented in various ways, a simple yet dynamic approach is adopted by using two feedback transistors (MN5,6), as shown in Fig. 5.2. Here, the MN5,6 are controlled by a 'Sense' signal which is derived from the output DC voltage (VDD) using a potential divider of a diode-connected transistor (MN3) and a linear transistor (MN4).

In the presence of high input RF power, the output DC voltage and the corresponding 'Sense' signal will have high voltage levels. This high 'Sense' signal switches on the biasing transistors (MN5,6), hence, applying dynamic biasing to the gates of the PMOS rectifying devices to limit their reverse leakage current, as shown in Figs.5.3a and 5.3b.

Although the DC bias applied to the PMOS gate limits both its forward and reverse conductivity, it does not increase its conduction loss; as it holds a low voltage drop ($V_{SDp}$), as shown in Fig.5.3c by operating in the linear region while passing a lower current, ($I_{Dp}$), than the conventional rectifier, as shown in Fig.5.3a. The rectifying PMOS and NMOS currents ($I_{Dp}$, $I_{Dn}$) and the alternating charges per RF cycle ($Q_p$, $Q_n$) required to produce 1.6V output DC voltage from the proposed and conventional rectifiers are plotted in Figs.5.3a,b,and c, respectively. As expected, both rectifiers supply the same net charges, $\Delta Q_f$, to produce the same output voltage for equal loading, ($100k\Omega$), as calculated by:

$$\Delta Q_f = \frac{V_o}{R_L} \times \frac{T_{RF\ cycle}}{2} = \frac{1.6V}{100k\Omega} \times \frac{0.5}{1GHz} \approx 8 fC. \quad (5.3)$$

However, the magnitude of alternating charges flowing back and forth is much larger ($5 \times$) in the case of the conventional rectifier compared to the proposed rectifier,
Figure 5.3 – (a) Simulated currents, and (c) voltage drops of the rectifying PMOS in the conventional and proposed rectifiers.
Figure 5.4 – Charges per RF cycle in conventional and proposed rectifiers for 1.6V output DC voltage.
demanding higher RF power for the same output voltage. Although the adaptive bias circuit is applied only to the PMOS transistors, reverse leakage for NMOS is also reduced due to the reduced effective bias leading to a $3 \times$ charge saving, as shown in Fig. 5.3b.

On the other hand, at low RF power, the sampled 'Sense' signal is low and MN5,6 are off. At the same time, the RF voltage is still applied differentially to the gate-source terminals of the four rectifying devices as in the conventional, cross-coupled rectifier [38]. This preserves the main sensitivity advantage of the cross-coupled scheme to the low input RF power levels.

Moreover, the proposed implementation has minimal loading effects. The sensing branch (MN3,4) is designed such that it has a low quiescent current ($\sim 1.3 \mu A$ at $V_o = 1.2 V$, $R_L = 100 k\Omega$) by increasing the length of the diode-connected MN3 and the linear-resistive MN4, whereas it is OFF at $V_o < V_{th}$, as shown in Fig. 5.5. Also, the biasing branches (MN5,6) have no static power consumption as they are connected to gates of MOS devices (MP1,2) and to the decoupling capacitors.

5.3 Experimental Results

The proposed rectifier is implemented in 0.18$\mu m$ CMOS process technology and occupies a 65 x 130 $\mu m$ active area, including the two additional capacitors and transistors. A microphotograph of the module including the testing pads is shown in Fig. 5.6. First, the input reflection coefficient is measured using Agilent’s vector network analyzer (N5225A) at different input RF power levels. Then, the input RF power ($P_{in}$) is deduced from the RF source power level after the reflection and transmission losses are de-embedded. The RF measurements are carried out using a 1GHz sinusoidal signal fed to a single-stage adaptive rectifier loaded by a 100$k\Omega$ resistor. All tests are
Figure 5.5 – Simulated standby (a) current and (b) power of the sensing branch MN3,4 in the proposed rectifier versus the output voltage.
Figure 5.6 – (a) Microphotograph of the realized adaptive rectifier on CMOS 0.18µm with test pads and (b) an enlarged view of the active area.

repeated for a single-stage, conventional, FX rectifier fabricated on the same die using the same test setup for comparison purposes.

The measured RF-to-DC power conversion efficiency is in well agreement with the simulation results for the proposed adaptive rectifier and the conventional FX rectifier, as shown in Fig. 5.7. The adaptive rectifier is verified to maintain a high PCE over an extended input range of RF power (more than twice the range of the conventional FX rectifier), as shown in Fig. 5.7. This enables the proposed adaptive rectifier to operate at both a low RF power level (i.e. long wireless power range) with superior sensitivity and also at a high RF power level with extended efficiency. The measured output DC voltage of the proposed adaptive rectifier and the conventional FX rectifier are shown in Fig.5.8. At the same input RF power level, the adaptive rectifier achieves a boosted output DC voltage, which is 25% higher than that of the conventional rectifier under the same loading conditions. While the proposed rectifier achieves extended optimal range, it still maintains a high peak efficiency of 65% and a sensitivity of -18dBm for 1V output over 100kΩ.

The proposed rectifier is fully characterized, for different input power levels and
Figure 5.7 – Simulated (dashed) and measured (solid) power conversion efficiency versus RF input power for the proposed and conventional rectifiers.

Figure 5.8 – Simulated (dashed) and measured (solid) output DC voltage of the proposed and conventional rectifiers versus RF input power.
Figure 5.9 – (a) Measured output DC voltage of the proposed (solid) and conventional (dashed) rectifiers versus RF input power for different loading conditions, and (b) the relative improvement percentage ($\Delta V_o$) for three different power levels.
various loads, using the automated test setup presented in Chapter 4. The measured output voltage of the proposed rectifier is higher than that of conventional rectifier for a large set of loads, varying from 20\(k\) to 200\(k\Omega\), as shown in Fig. 5.9a. In order to highlight the realized boosting in the output voltage, the percentage of the voltage improvement (\(\Delta V_o\)) is calculated relative to the conventional rectifier, at three different RF power levels (\(P_{in} = 60\mu W, 120\mu W, \text{ and } 180\mu W\)), and plotted in Fig. 5.9b. Obviously, the relative voltage boosting ranges from 24.5% to 30% over varying loads from 50\(k\) to 1\(M\Omega\).

Similarly, the measured power conversion efficiency shows a persistent improvement in the input-power dynamic-range for a large set of different loads varying from 30\(k\Omega\) to 1\(M\Omega\), as shown in Fig. 5.10. The results are separated in four subplots to highlight the relative improvement in the dynamic range of the proposed rectifier for each group of loads using the appropriate axes scale. It should be noted that, as the load resistance decreases, the output current (and thus the power) increases at lower output voltage (and thus at lower reverse leakage). This allows the PCE to grow to larger peaks for small load resistances, as shown in Figs. 5.10c and 5.10d. In other words, there is a critical output voltage after which the reverse-leakage loss becomes more severe than the dissipation power loss. Therefore, operating at output voltage less than this critical point (using smaller loads) increases the output DC power relative to the dissipation loss (while the reverse leakage is negligible at low output voltage). Consequently, high PCE peaks are achieved for low load resistances, as shown in Figs. 5.10c and 5.10d relative to high load resistances (shown in Figs. 5.10a and 5.10b) with the same power input.

Furthermore, this critical output voltage can be clarified by plotting the measured PCE curves versus output voltage. As shown in Fig. 5.11, the proposed rectifier has a higher optimal output voltage (\(V_{opt.} \approx 1V\)) than the conventional rectifier whose
Figure 5.10 – Measured power conversion efficiency versus RF input power for the proposed (solid) and conventional (dashed) rectifiers for different loading conditions.

Figure 5.11 – Measured power conversion efficiency of the proposed (solid) and conventional (dashed) rectifiers versus the output DC voltage.
PCE peak occurs at \( V_{\text{opt.}} \simeq 0.6V \). This enhanced headroom of the output voltage allows for wide dynamic range of input power levels, for a large set of different loads, as verified in Fig. 5.10 and Fig. 5.11.

Additionally, the measured PCE peaks are plotted versus the load resistances in Fig. 5.12. The PCE peak of both the proposed and conventional rectifiers follow the same behavior with regard to the load change. It worth mentioning that the PCE peaks of the two architectures are equal; however, they are located at different input power levels and output voltages, as illustrated previously in Figs. 5.10 and 5.11.

Similarly, the input dynamic range, at which the rectifier maintains 80% of its peak power conversion efficiency, is extracted from the measured data of Fig. 5.10 and is plotted in Fig. 5.13. The proposed rectifier shows a wider dynamic range than the conventional rectifier for a large set of different loads.

In terms of the operating frequency, the adaptive rectifier proposed in this chapter shows higher power conversion efficiency at 1 GHz in UHF band compared to the self-
biased rectifier proposed in chapter 4, as shown in Fig. 5.14. The PCE peak of the self-biased rectifier is 40% at 850MHz (the minimum frequency in the RFID UHF band), while the PCE peak of the adaptive rectifier approaches 90% at 1GHz for the same loading condition (50 kΩ).

In addition to the extension achieved in the dynamic range of the proposed rectifier, the input impedance is also stabilized versus different RF input power levels, as shown in Figs. 5.15 and 5.16. As a result, a wide-range matching network can be simply implemented for the stable impedance of the proposed rectifier. The measured input (series) resistance of the proposed rectifier is less than that of the conventional rectifier, as shown in Fig. 5.15, due to the adaptive negative feedback controlling its conductivity (and thus its parallel resistance). As shown in Fig. 5.16, the measured input (series) capacitance of the proposed rectifier is higher than the conventional rectifier due to the added coupling capacitors (CP3,4) at the rectifier inputs.

A performance comparison of the adaptive rectifier with prior art is presented in
Figure 5.14 – Measured power conversion efficiency (PCE) of both the proposed adaptive and self-biased rectifiers, and the conventional rectifier versus RF input power levels at UHF band.

Table 5.1. The optimal range is defined as the input power range over which the rectifier maintains power conversion efficiency higher than 80% of its peak efficiency. The proposed architecture achieves a much wider optimal range compared to previously reported architectures, including the most common, fully cross-coupled rectifier [38] with 5dB better sensitivity. More than 2× improvement is achieved compared to the enhanced, 36-stage voltage doubler with floating gate devices [83]. Also, the proposed architecture provides a wide optimal range without sacrificing either the PCE as [107] or sensitivity as [38,83]. Although the reconfigurable 4-stage rectifier [103] shows wide dynamic range, it requires a multi-stage re-configuration and is measured over a tracking load (regulator with external reference). It is important to note that the proposed single-stage architecture can be combined with this tracking load and multi-stage techniques in [101,103] to build a wider range, multi-stage rectifier.
Figure 5.15 – Measured input (series) resistance of the proposed (solid) and conventional (dashed) rectifiers versus RF input power for different loads.

Figure 5.16 – Measured input (series) capacitance of the proposed (solid) and conventional (dashed) rectifiers versus RF input power for different loads.
Table 5.1 – The performance of the adaptive rectifier versus the self-biased rectifier and state of the art UHF rectifiers.

<table>
<thead>
<tr>
<th>Ref</th>
<th>Process</th>
<th>Configuration</th>
<th>Stages</th>
<th>Load ( (R_L) )</th>
<th>Freq. ( (f_{RF}) )</th>
<th>Sensitivity @( Vo = 1V )</th>
<th>Peak PCE</th>
<th>Dynamic Range(^a)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work</td>
<td>0.18( \mu m )</td>
<td>Proposed Adaptive(^b)</td>
<td>1-stage</td>
<td>100 kΩ</td>
<td>1 GHz</td>
<td>−18 dBm</td>
<td>65%</td>
<td>8.7</td>
</tr>
<tr>
<td>This Work</td>
<td>0.18( \mu m )</td>
<td>Proposed Self-biased rectifier</td>
<td>1-stage</td>
<td>100 kΩ</td>
<td>950 MHz</td>
<td>−14.6 dBm</td>
<td>28.4%</td>
<td>4.8</td>
</tr>
<tr>
<td>This Work</td>
<td>0.18( \mu m )</td>
<td>Conventional cross-coupled</td>
<td>1-stage</td>
<td>100 kΩ</td>
<td>1 GHz</td>
<td>−14.8 dBm</td>
<td>63%</td>
<td>5.4</td>
</tr>
<tr>
<td>[38]</td>
<td>0.18( \mu m )</td>
<td>Conventional cross-coupled</td>
<td>1-stage</td>
<td>100 kΩ</td>
<td>953 MHz</td>
<td>−12.8 dBm</td>
<td>82.6%</td>
<td>3.2</td>
</tr>
<tr>
<td>[83]</td>
<td>0.25( \mu m )</td>
<td>Floating gate voltage doubler</td>
<td>36-stage</td>
<td>330 kΩ</td>
<td>906 MHz</td>
<td>−14.6 dBm</td>
<td>60.7%</td>
<td>3</td>
</tr>
<tr>
<td>[107]</td>
<td>90 nm</td>
<td>Conventional cross-coupled</td>
<td>5-stage</td>
<td>330 kΩ</td>
<td>868 MHz</td>
<td>−20 dBm</td>
<td>40%</td>
<td>3.8</td>
</tr>
<tr>
<td>[108]</td>
<td>0.13( \mu m )</td>
<td>Adaptive ( V_{th} ) compensated</td>
<td>12-stage</td>
<td>500 kΩ</td>
<td>915 MHz</td>
<td>−17 dBm</td>
<td>32%</td>
<td>5.2</td>
</tr>
<tr>
<td>[103]</td>
<td>0.13( \mu m )</td>
<td>Reconfigurable stages wiring</td>
<td>4-stage</td>
<td>Tracking Load(^c)</td>
<td>868 MHz</td>
<td>−21 dBm(^d)</td>
<td>60%</td>
<td>19.5</td>
</tr>
</tbody>
</table>

\(^a\)Input power dynamic range = \( (P_{max}/P_{min}) \) for PCE ≥ 0.8 Peak PCE,
\(^b\)Intra-stage,
\(^c\)Tracking load (regulator with external ref. [103])
\(^d\)for \( Vo = 2V \)
5.4 Conclusion

In this chapter, we propose an adaptive, differential, cross-coupled rectifier with an extended input RF power range without trading off the sensitivity (Pin=-18dBm at Vo=1V) or the peak power conversion efficiency (peak PCE=65%). The architecture of the proposed rectifier was presented and its performance was verified and compared with the conventional, fully cross-coupled rectifier.
Chapter 6

Conclusion & Future Work

The wireless power receiver (WPRx) is the linchpin for the current and next generation battery-less devices, including biomedical implantable sensors. In this work, we propose a wirelessly powered biomedical implantable sensor as a single chip solution. The proposed chip can serve as a generic platform for sustainable battery-less devices. At the time of publishing this work [3], the proposed wirelessly powered sensor has the first fully integrated WPRx front end that uses an on-chip antenna for both the RF power and data. The design has been optimized for the eye environment to account for signal deterioration at the designed frequency. A custom test setup has been presented imitating a real eye environment. The size of the chip is only 1.5 mm × 3.0 mm, and when measured in the eye-like environment, it successfully harvested 1 V from an incoming 5.2-GHz 5-W EIRP RF signal from a distance of 3 cm. The power receiver module stores sufficient energy (2.5 nJ) on the integrated 5-nF MOSCAPs to power the circuits for reliable IOPM operation.

From the lessons gained during the design and test of the first chip, we propose two novel architectures for adaptive WPRx front end that operate at wider dynamic ranges of input RF power than other conventional ones. The first is a self-biased, cross-coupled, differential rectifier with a 50% enhanced power conversion efficiency over a wide range of input power levels and under different loading conditions. A sensitivity of $P_{in} = 30\mu W$ at $V_o = 1V$ and peak power conversion efficiency (peak
Figure 6.1 – Power conversion efficiency versus RF input power for state-of-the-art UHF rectifier [4]

PCE = 65.3) is achieved for a 50kΩ load. The architecture of the proposed rectifier is presented, and its performance is compared with the conventional, cross-coupled rectifier.

In order to enhance the proposed self-biased rectifier, and to alleviate the emerging drawbacks, we propose an adaptive self-biased rectifier that achieves a wider dynamic range than conventional rectifiers while maintaining high PCE peak (65%) and without trading off the sensitivity (Pin = −18 dBm at Vo = 1 V). Unlike the self-biased rectifier that is proposed earlier in this thesis, the second proposed adaptive rectifier pushes the upper limits of the operating frequency to the GHz range. The architecture of the proposed rectifier was presented, and its performance was verified and compared with the conventional, fully cross-coupled rectifier.

The PCE of the proposed adaptive rectifier is compared with state-of-the-art UHF rectifiers versus RF input power in Fig. 6.1. CMOS rectifiers achieve high PCE at high
Future Work

- Using the proposed sensing platform for other implantable/wearable devices or other WSN applications.

- Adaptive (tunable) matching network to account for $Z_{\text{rec}} = f(P_{\text{RF}})$ variations.

- Adaptive (smart) loading to maximize PCE efficiency and to account for the loading variations.

- Smart antenna and beamforming for MIMO wireless information/power transfer (WIPT).

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**Figure 6.2** – Potential blocks and techniques for further enhancement in the wireless power receiver front end

RF power levels, however they have poor sensitivity and efficiency at low RF power levels. Although Schottky rectifiers show good sensitivity at low power levels (around -20 dBm) and operate in the high GHz range, they suffer from a poor efficiency at these low power levels, as shown in Fig. 6.1. Moreover, Schottky diodes require additional mask layer and processing steps, therefore they are not commonly available in commercial CMOS processes. As shown in Fig. 6.1, the proposed adaptive rectifier shows higher PCE peak than Schottky rectifier and better sensitivity (low RF power level) than CMOS rectifiers.

### 6.1 Future Directions

The work of this thesis can lead to further advances on both the system level and on the WPT components level. The proposed wirelessly powered implantable sensing platform can be utilized for various types of sensors, such as temperature sensors, pressure sensors, or chemical and biological sensors, attached on-chip or off-chip. Also, designing a second prototype utilizing the adaptive WPRx front-end will lead to a wider operating range of wireless powering.
The proposed concept of adaptive biasing is applied for the half of the rectifier circuit (PMOS devices only) to avoid degradation of the PCE peak, however, the proposed technique can be adjusted to control all rectifying devices (NMOS and PMOS devices). As a result, the dynamic range is expected to be wider with slight degradation of the rectifier sensitivity.

Furthermore, the big picture of having an agile WPRx front end can be extended by integrating a smart, tunable matching network to counteract the variations of the rectifier input impedance with the change of the RF power levels. In the same token, an adaptive smart loading mechanism can absorb the maximum efficiency out of the WPRx front end at the presence of high RF power levels, while reducing the loading current at low power to maintain the rectifier sensitivity. Better hybrid RF-to-DC power converter architectures can also be built by mixing different architectures in both the intra-stage or inter-stage levels. Smart antennas can be used in a MIMO system to optimize the wireless information and power transfer (WIPT) process. Even the RF signal can be replaced with an optimized waveform, which has high peak-to-average ration, to maximize the overall efficiency of the wireless power transfer process.
REFERENCES


tification CMOS Tag IC Using Ferroelectric RAM in 0.35-µm Technology,”


[85] M. Mark, “Powering mm-size wireless implants for brain-machine interfaces,” p. 150, 2011, 2614388481; Integrated circuits; Applied sciences; Brain-machine interfaces; 66569; n/a; English; Mark, Michael; Copyright ProQuest, UMI Dissertations Publishing 2011; 0544: Electrical engineering; 2011; 9781267228673; 929198804; 64402471; Wireless implants; 3499020; Wireless power transfer; 2012-03-30; M3: 3499020; M1: Ph.D. [Online]. Available: http://search.proquest.com/docview/929198804?accountid=78788


[98] M. Mark, T. Björninen, L. Ukkonen, L. L. Sydänheimo, L.nheimo, and J. Rabaey, “SAR reduction and link optimization for mm-size remotely powered wireless implants using segmented loop antennas,” in *Biomedical Wireless*


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