Channel Equalization Techniques for Non-Volatile Memristor Memories

Rawan Naous*, Mohammed Affan Zidan†, Ahmed Sultan*, and Khaled Nabil Salama*
*King Abdullah University of Science and Technology, Saudi Arabia, {rawan.naous, ahmed.salem, khaled.salama}@kaust.edu.sa
†University of Michigan, USA, {mzidan@umich.edu}

Abstract—Channel coding and information theoretic approaches have been utilized in conventional non-volatile memories to overcome their inherent design limitations of leakage, coupling and refresh rates. However, the continuous scaling and integration constraints set on the current devices directed the attention towards emerging memory technologies as suitable alternatives. Memristive devices are prominent candidates to replace the conventional electronics due to its non-volatility and small feature size. Nonetheless, memristor-based memories still encounter an accuracy limitation throughout the read operation addressed as the sneak path phenomenon. The readout data is corrupted with added distortion that increases significantly the bit error rate and jeopardizes the reliability of the read operation. A novel technique is applied to alleviate this distorting effect where the communication channel model is proposed for the memory array. Noise cancellation principles are applied with the aid of preset pilots to extract channel information and adjust the readout values accordingly. The proposed technique has the virtue of high speed, energy efficiency, and low complexity design while achieving high reliability and error-free decoding.

I. INTRODUCTION

Non-volatile memory systems are storage mediums that retain the data without the need of having an input bias. The physical properties of these systems make retrieving the saved data a distorting process and prone to errors. Particularly due to mechanisms such voltage drift, overwriting, or inter-cell coupling, the threshold between the high and low bit is not clear and affects the decoding operation. Communication and information theoretic principles have been employed into the non-volatile memory domain to enhance the reliability of the memory array. Error correcting schemes try to combat the charge drifting and enhance the error rate [1]–[3]. Alternatives such as low-density parity check (LDPC) decoding is applied with the aid of soft information to maximize the mutual information between the input and the output and enhance by that the accuracy of the read operation [4]. Rank modulation schemes address the writing asymmetry within memory where the relative charge among several cells is used to represent the information [5]. Moreover, dynamic threshold setting is employed in flash memories, where the threshold is not fixed, but rather recalculated at every read operation [6], [7]. These problems have become increasingly apparent in conventional designs due to the technology scaling [8] and integration requirements. It has mandated a shift towards emerging non-volatile memory technologies, such as memristors. However, information theoretic [9] and analytical [10] techniques are also applied as data distortion remains a reliability affecting parameter in the memory design.

The memristor is a two-terminal non-volatile memory device that undergoes a resistance change under an input excitation. It varies between a high conductive state $R_{\text{ON}}$ and high resistive state $R_{\text{OFF}}$ [11], [12]. The two boundary resistance values can be considered as digital high ‘1’ and low ‘0’ bits respectively [13]. Memristor-based memories are comprised of crossbar structures where the memristor lies at the intersection of two connecting nanowires [14]. Data is saved as resistance values across the memristor [15]. The most energy efficient approach to reading out from the memory is conducted through activating the corresponding word line and bit line of a particular cell while keeping the remaining lanes within the array floating. The voltage applied at the terminal of the memristor induces a current that is sensed to indicate the value of the saved data. Despite the appealing features of the crossbar, particularly concerning the activation, scaling, and density attainment, a limiting factor is faced throughout the read operation. Due to the nature of passive arrays, where no switching control is available at the terminals of the memory cell, once the reading voltage is applied, the
builds on estimation principles that are well-established in read out operation accuracy. However, the proposed method density compromising techniques [25]–[27] to enhance the former handles the array from a probabilistic perspective and be split into analytical and circuit-based techniques. The gateless approaches that target the sneak path problem could accuracy versus the density of the memory array. Alternative a selector device per cell [20]. Hence prioritizing the ac-

data detection.

estimated and subtracted from the received values for proper

paths are thus the channel imposed distortion that needs to be

data. The sneak memory are the actual transmitted bits, and the data attained

distortion within the row allows for the dynamic estimation noise is two-dimensional and shows a high correlation [29]. The sneak path effect, is modeled as a Gaussian noise added to the original signal [29]. The read values become dominated by the noise and the margins between the high and low bits almost diminish. This overlap increases the bit error rate drastically as the spectra are almost completely overlapping as shown in Figure 2a. The inset of Figure 2a represents the ideal case for the read out data where no sneak path effect is apparent. This overlap is due to the physical property of the crossbar structure and the reading techniques. Figure 2b shows the equivalent resistance $R_{eq}$ seen upon reading from a target cell. The sneak path is seen as a resistance in parallel with the target cell to be read and the total resistance seen at the reading terminals $n_1$ and $n_2$ is

$$R_{eq} = R_m/ \left( R_1 + R_2 + R_3 \right)/ \left( R_4 + R_5 + \ldots \right)/ \ldots$$

$$R_{eq} = R_m/ \left( R_{sp} \right), R_{sp} = f(\text{data})$$

where $R_m$ is the actual cell value that needs to be retrieved, and $R_{sp}$ is the sneak path resistance that is mainly data dependent. It is a function of the data patterns saved, as the high and low bit values, and consequently the resistances whether $R_{ON}$ or $R_{OFF}$ affect the sensed current with a different weight and intensity.

During the read operation, the activated row and column of interest are the main factors affecting the sneak path. The noise is two-dimensional and shows a high correlation [29] across these dimensions along with the target cell. The number of high bits along the vertical and horizontal dimensions is the principle contributor to the distortion undergone at the target cell read. The higher the number of high bits, the larger is the distortion imposed. The memory is then modeled as a channel with the saved data corresponding to the actual signal $S_i$, the sneak path as the added distortion $D_i$, and an estimated signal $\hat{S}_i$ as depicted in Figure 3. For the distortion adjustment, having these parameters $N_{c,j}$, corresponding to the number of high bits per column, and $D_{max,i}$ as the maximum distortion within the row allows for the dynamic estimation of the distortion per cell $D_{i,j}$. Thereby, we can formulate an equation for the distortion at target cell $(i,j)$ as follows

$$D_{i,j} = D_{max,i} \frac{N_{c,j}}{N_A}$$

II. Estimation Principles

The read operation conducted within the array results in a distribution of values for the high and low bit respectively. Ideally, the two spectra would have sufficient separation to allow for accurate detection of the read bit. However, the added distortion within the array, which is primarily dependent on the sneak path effect, is modeled as a Gaussian noise added to the communication field. Pilots are inserted into the array to extract the noise information and adjust the read out values accordingly [28]. The estimation principles and the readout technique are further illustrated in the following sections. Circuit simulations for the memristor-based memory array show the efficiency of the applied technique with the improved read margins and the diminished bit error rates.

A direct solution to the sneak path effect is by adding a selector device per cell [20]. Hence prioritizing the accuracy versus the density of the memory array. Alternative gateless approaches that target the sneak path problem could be split into analytical and circuit-based techniques. The former handles the array from a probabilistic perspective and imposes limitations on the distributions [9], [10], [21] and data to be saved within the array. On the other hand, the later adopts delay imposing [22], architectural [23], [24], and density compromising techniques [25]–[27] to enhance the read out operation accuracy. However, the proposed method builds on estimation principles that are well-established in

Fig. 2: Bits Distribution Illustration (a) The overlapping distributions for the high and low bits as a result of the sneak path distortion added. The inset of the figure represents the ideal read case where there is not added distortion. (b) The cell resistance seen at the read out operation. The actual cell resistance is put in parallel with the sneak path resistance affecting significantly the read out current

Fig. 3: Signal Detection Model The sensed signal is composed of the original saved data with the sneak path current modeled as an added distortion parameter.
where $D_{\text{max},i}$ corresponds to the maximum distortion that could be encountered within the row. This maximum value is seen in a cell that lies in an all-ones column. Thus, preset cells are used to extract the required information for the estimation process. The first row and column of the memory array are allocated for pilots with high bit value. For estimating the maximum distortion $D_{\text{max},i}$, the row pilot lying on the same row of the target cell is used. The corresponding distortion is the difference between the read out value for the pilot $P_1$ and the saved data $I_{\text{high}}$. The second parameter required for the estimation is the number of high bits per column $N_{c,j}$. For that, a hypothesized relation is formulation between the readout value of the pilot on top of each column and the number of high bits. A linear relationship is found as

$$P_{c,j} = \alpha N_{c,j} + \beta$$  \hspace{1cm} (3)

where the parameters $\alpha$ and $\beta$ are obtained from an offline fitting performed prior to the start of the reading operation. The fitting process remains valid for different distributions and patterns saved within the array. Thus, the offline formulation is required only once for a particular array size. Figure 4 represents the simulation results for a 256kb array and shows the linear dependence of the readout values of the pilots and the number of high bits per column.

The estimation scheme was applied on a 512x512 array with pilots induced at the first row and column. The pilots were set to a high bit value and used for the estimation processes described earlier. Reading out 100 samples from random locations within the array shows the predominance of the distortion on the read out values. The margin between the high and low bits is completely collapsed with no clear separation to ensure accurate bit decoding. Figure 5a depicts the readout values along with the actual input values saved in the array. The data shown is normalized with respect to the ideal high bit. The sneak path effect is apparent making the levels of readout data almost double that of the input data. Nonetheless, applying the estimation scheme proposed and provides an estimate of the noise parameter per cell as shown in Figure 5b. The adjusted values after the removal of the estimated distortion are shown in Figure 5c. The adjustment allowed for the readout values to be shifted back to the range of the input values and a clear distinction between the high and low bits is possible leading to an error-free detection process.

### III. Pilot-assisted Readout Scheme

Pilots in communication terms are preset channel slots used to get information about the channel [19]. In a similar sense, pilots are inserted in the array at preset locations to provide an estimate of the distortion imposed by the channel throughout the read operation. We suggested this technique earlier in [29] as a possible solution to the sneak path problem but without analyzing or providing the optimum setting for the allocation.
Fig. 6: **Pilots in Memory** An example of the allocation of pilot cells at the primary row and column of the memory array. The actual data is saved as binary values of ‘1’ or ‘0’ at the remaining cells within the array.

of the pilot cells nor the estimation principles to be applied. In the following subsections, the pilot-assisted read operation is further elaborated along with the simulation results for the memory array. Moreover, in [30] we introduced the notion of dummy bits to provide an adaptive threshold technique for connected terminals reading mode.

A. **Read Operation**

Incorporating the estimation scheme into the read operation within the array is a multi-step process. As dynamic signal adjustment is required prior to decoding the target cell value to a ‘1’ or ‘0’ respectively. To that end, a three steps process is required

1) **Read the row pilot** \( P_{R,i} \) and extract the row distortion.
2) **Read the column pilot** \( P_{C,j} \) and extract the number of high bits.
3) **Read the Target cell** \( S_{i,j} \) and adjust it according to the estimated distortion.

We apply a threshold to \( \hat{S}_{i,j} \). This is equal to \( S_{i,j} \) minus \( \hat{D}_{i,j} \), which is the estimated sneak path distortion.

\[
\hat{D}_{i,j} = (P_{r,i} - I_{\text{high}}) \frac{P_{c,j} - \beta}{\alpha N_A} 
\]

(4)

In comparison to the state of the art architectural techniques, the number of needed reading steps per cell is equivalent to the minimum required. However, this is valid while adopting an entirely random reading approach in the memory. However, once fetching data out of memory, entire blocks are taken at a time, and complete words or lines are read sequentially. A concept referred to as locality of reference is employed and reduces the number of required readings. As an entire row is read in sequence, the row pilot reading is then shared with all the data cells within the same row. This continuous read eliminates the need to extract the maximum distortion \( D_{\text{max},i} \) for the every target cell along the same horizontal dimension. However, this distortion still needs to be scaled down with the number of high bits along the vertical dimension. Thus, the column pilots \( P_{c,j} \) are required per target cell. Consequently, an average of two reads per cell is needed to get an estimate of the data stored. A faster read operation is thus attained with the applied scheme at a higher energy efficiency.

B. **Simulation and Results**

The testing and simulations were performed using a circuit-based simulator (HSPICE) to get a more realistic insight into the behavior of the system. However, in order to cater for the large memory sizes and the different patterns and data types to be saved within the array, a python script was used in order to generate the spice netlists and simulate the complete array iteratively [24]. The script offered a lot of flexibility in terms of the testing sizes, patterns, interconnections and modeling parameters, whether for the non-idealities of the circuit or the memristor characteristics. The model for the memristor used corresponds to real devices reported by HP for memory application [22], [31].

\[
I = k_{\text{on/off}} \sinh(\alpha V) 
\]

(5)

where \( k_{\text{on/off}} \) and \( \alpha \) stand for the ON/OFF state constants for the memristor device and \( V \) corresponds to the input voltage. The circuit structure was completely simulated including the interconnect wires. A value of 10Ω was used as wire resis-
Fig. 8: **Bits Margins.** Simulation for a 256kb array filled with NIST data images. The parameters for the non-linear memristor device used are: $\alpha=3V^{-1}$, $k_{on}=10N$, $K_{eff}=10P$, $R_{ch}=10\Omega$. (a) Data distributions prior to estimation show an overlap between the high and low bits. (b) Split margins for the high and low bit after the estimation process. It allows for the accurate detection and distinction of the bits '0' and '1' respectively.

Fig. 9: **Array Density**. The density loss with the added pilots with respect to the array size. The loss is almost negligible (less than 1%) for practical array sizes of 256kb and higher.

array were used to validate the proposed scheme. Figure 7 shows a snapshot of 4 samples used for the simulation of a 256kb array. The read values prior to any estimation are shown in Figure 8a. As depicted, the margins for the high and low bits are completely overlapped resulting in significant bit error rates. Alternatively, once distortion estimation is applied, the ones and zeros values are completely separated as depicted in Figure 8b. This channel equalization approach leads to error-free decoding for the read out data. An enhancement of 110% in the read margin is attained at the mere expense of two reserved lines in the memory array. A negligible density loss of less than 1% for practical sized array aids in establishing the accuracy, speed, and simple design.

Overall, a comprehensive technique is proposed that offers the flexibility of circuit-based approaches in allowing any data distribution and memory structure while originating from an analytical perspective. It doesn’t impose any restrictions on the size of the array, where restrictions up to 16kb were reported [10], nor limits the amount of information that could be saved, up to $2n\log n$ for a square array of $(n, n)$ as compared to alternative information theoretic approaches. Figure 9 shows the density loss attained with the allocation of the pilot cells. As only two lines of data are reserved for the pilots, a negligible loss of less than 1% is encountered with practical array sizes.

**IV. Conclusion**

A communication-inspired approach is adopted in the read operation of emerging non-volatile memristor-based memory. It builds upon the use of preset pilots at the primary horizontal and vertical dimensions of the array to accommodate the two-dimensional nature of the noise imposed. The a priori information aided in extracting the distortion parameters per cell and consequently alleviating the sneak path effect. A novel solution addressing the different design challenges is proposed offering enhancements on several aspects of speed, accuracy, design simplicity, and power efficiency.

### Table 1: Array Density

<table>
<thead>
<tr>
<th>Array Size (Kb)</th>
<th>Density Loss (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>12</td>
</tr>
<tr>
<td>1</td>
<td>11</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
</tr>
<tr>
<td>16</td>
<td>9</td>
</tr>
<tr>
<td>64</td>
<td>8</td>
</tr>
<tr>
<td>256</td>
<td>7</td>
</tr>
<tr>
<td>1,024</td>
<td>6</td>
</tr>
</tbody>
</table>

**Fig. 9:** The density loss with the added pilots with respect to the array size.
REFERENCES


