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In-situ CdS/CdTe Heterojuntions Deposited by Pulsed Laser Deposition

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Abstract

In this paper pulsed laser deposition (PLD) methods are used to study p-n CdTe/CdS heterojunctions fabricated *in-situ*. *In-situ* film deposition allows higher quality p-n interfaces by minimizing spurious contamination from the atmosphere. Morphologic and structural analyses were carried for CdTe films deposited on various substrates and different deposition conditions. The electrical characteristics and performance of the resulting p-n heterojunctions were studied as function of substrate and post-deposition anneal temperature. *In-situ* growth results on diodes with a rectification factor of ~ 10^5, an ideality factor < 2, and a reverse saturation current ~10^{-8} A. The carrier concentration in the CdTe film was in the range of ~10^{15} cm^{-3}, as measured by C-V methods. The possible impact of sulfur diffusion from the CdS into the CdTe film is also investigated using High Resolution Rutherford Back-Scattering.

Keywords: Cadmium telluride, pulsed laser deposition, heterojunctions

1. Introduction

Over the past decades cadmium telluride (CdTe) has been widely studied as a p-type absorption layer in photovoltaics given its adequate band gap (~1.45 eV) and high absorption coefficient (10^5 cm^{-1}) [1-3]. In fact, CdTe-based solar cells have shown efficiency > 21%, although most reports range from 10% to 20%. These solar cells have also been demonstrated in large area substrates [4]. Furthermore, exciting photonics properties reported for CdTe quantum dots have positioned this material as a candidate for novel optoelectronics devices and detectors [5-7]. For example, recently Barber et al. and Koenig et al. reported single crystal CdTe X-ray detectors for clinical applications [8, 9]. Ma et al. reported multilayers of CdTe quantum dots as formaldehyde gases sensors.[10] Filipenko et al. and Murphy et al. also reported the use of single crystal and thin films CdTe as particle detectors for α–particles, single electrons, and thermal neutrons [11, 12]. An additional advantage of thin film CdTe is that it can be deposited using a wide variety of methods including sputtering, close-spaced sublimation, pulsed laser deposition, physical vapor deposition, among others [2, 13, 14].

Most thin film CdTe heterojunctions (< 5 μm) are formed with CdS as the window layer in solar cells [1, 3, 4, 13-21]. So far, most CdTe/CdS reports are focused on evaluating the impact of this material on solar cells performance as function of CdTe deposition parameters such as substrate temperature, deposition pressure, post deposition treatments as well as metal contacts. In particular, when physical vapor deposition methods are used, the deposition pressure is one of the most important parameters to control since a change in deposition pressure results in substantial changes on the species mean free path and directly impacts film stoichiometricity

with the concomitant change in carrier concentration. This was also demonstrated for CdS in a previous report from our group [22]. The substrate temperature is also important. Substrate temperature directly impacts crystallinity and grain size in the CdTe films; however, if the substrate temperature is too high some re-evaporation might occur and affect film composition and carrier concentration [19]. CdTe post deposition annealing is normally required for a recrystallization process and grain growth. This annealing improves the crystalline quality and the electrical performance of the resulting CdTe films. The impact of this annealing treatment has been widely reported and it is normally carried out at temperatures from 360 °C to 440 °C [1, 3, 4, 13, 14, 23]. However, none of these reports consider the effect of exposing the interfaces to ambient when switching from one deposition system (or film) to another. Such exposure to atmospheric conditions might impact the quality of the CdTe/CdS junction.

In this work, pulsed laser deposition (PLD) methods are used to study CdTe/CdS heterojunctions fabricated *in-situ*. *In-situ* deposition allows higher quality p-n interfaces by minimizing exposure to potential contamination from air. PLD deposition methods use a high-power laser that ablates the target materials to deposit thin films on a substrate. A key advantage of PLD is that the target composition is directly transferred to the substrate with a very well controlled deposition rate. Furthermore, the film growth can be carried out in several reactive atmospheres. Other variables include laser power and frequency, substrate temperature, etc. There are some reports for CdTe/CdS layers deposited by PLD. However, the reports are mainly focused on physical properties of the films as evaluated by scanning electron microscopy, atomic force microscopy, UV-Vis and X-ray diffraction [24, 25]. PLD-based solar cells with efficiencies from 3% to 10.5% have also been reported [16-21]. In this paper, *in-situ* deposited CdTe/CdS films are analyzed with a special emphasis on their electrical properties using current-voltage

and capacitance-voltage measurements of the resulting diodes. Diode parameters evaluated include the ideality factor, rectification factor, reverse saturation current, and film carrier concentration [26-28]. High Resolution Rutherford Back Scattering is used to analyze the heterojunction composition and identify possible sulfur diffusion from the CdS film into the CdTe films.

2. Experimental details

The CdS and CdTe films were deposited by PLD methods. 500 nm thick of thermally grown SiO_2 on silicon wafers or on 150 nm thick commercial ITO/glass were used as a substrates; before deposition, all substrates were cleaned using acetone, IPA and water for 5 minutes in an ultrasonic bath followed by drying in nitrogen. The films were deposited using a commercially available Pioneer 180 from Neocera Inc. with a 248nm KrF excimer laser. During deposition, the energy density and frequency were maintained at 0.75 J/cm^2 and 10 Hz, respectively. The background pressure was at $1x10^{-6}$ Torr and a mass flow controller (MFC) was used to control the gas flow during the film deposition. After deposition, Scanning Electron Microscope (SEM, Zeiss supra-40) was used to study the resulting film morphology. A Rigaku Ultima III X-ray Diffractometer (XRD) equipped with a Cu Kα radiation (λ= 0.15406 nm) was used to study the crystalline structure and grain size for the films. A Keithley 4200-SCS tool and a HP 4284A precision LCR meter were used for the electrical characterization of the heterojunctions. The electrical characterization included I-V curves to extract the ideality factor and reverse saturation current. C-V curves were measured to extract carrier concentration. Finally, the CdTe/CdS interface was analyzed by RBS. A Kobelco RBS with 45° as a solid angle and 107.5° as scattering angle was used.

3. Results and discussion

The effect of the deposition pressure on the characteristics of the CdTe films was first evaluated. The CdTe films were first deposited on thermally grown SiO_2 using silicon wafers. For the CdTe deposition a mass flow controller (MFC) was used to control the Argon pressure in the PLD chamber ranging from 1 to 100 mTorr. All the CdTe films were deposited at room temperature and 20,000 laser shots were used to deposit these samples. This results in film thickness ranging from 190 to 230 nm. The thicker films correspond to films deposited at lower pressure. After film deposition, morphology and crystallinity of the CdTe films were studied using SEM and XRD respectively. Figure 1 shows the SEM results for CdTe films deposited at different deposition pressures. The CdTe films deposited at low pressure seem to be mostly composed by small CdTe grains. This is especially clear for the films deposited at 1 mTorr (a). This effect is likely due to the fact that for lower pressure the mean free path of the ablated species is very large and this results in species reaching the substrate surface at higher energy, which hiders further growth of larger CdTe crystals. As the pressure increases, larger CdTe grains are evident and the number of grains and size monotonically increase with deposition pressure. Uniform CdTe films are achieved for films deposited at pressures >20 mTorr (c). Some cracks are evident for films deposited at 50 mTorr and 100 mTorr. This is due to residual stress in the CdTe film. These cracks can produce short circuit in diodes, as we will show later in the paper.

XRD analyses were carried out to evaluate the impact of deposition pressure in the CdTe microstructure. Figure 2 (a) shows the XRD results for the CdTe as function of deposition pressure. All the films show a preferential (111) CdTe cubic phase. The main diffraction peak intensity reduces and broadens as the pressure reduces and is due the smaller grain size of the

CdTe films, as discussed above in the SEM results. Also, the shift in the (111) peak for films deposited at pressures >20mT further indicates residual stress in the films, which produces the cracks observed in Figure 1. Figure 2 (b) shows additional smaller peaks in the region from 25 to 50^{o}. Such peaks are for both cubic and hexagonal CdTe phases. CdTe films deposited at pressures >50 mTorr show stronger hexagonal (101) and (200) peaks. In summary, low deposition pressure results in CdTe films with very low concentration of hexagonal CdTe whereas higher pressure results in a CdTe with both hexagonal and cubic phases. It is important to notice that the hexagonal phase for CdTe is metastable [18] [24] and for the next set of experiments a deposition pressure of 20 mTorr was selected. This pressure achieves CdTe films that are stress-free and mostly cubic. Next, the effect of the substrate is discussed.

To investigate the effect of the substrate CdTe films were deposited on top of a CdS film that had been previously deposited on either amorphous (SiO_2) or polycrystalline (ITO) substrates. The CdS layers were deposited by PLD and with a thickness of 100 nm. The deposition pressure was 80 mTorr and at room temperature. The CdTe film was deposited *in situ* after the CdS deposition at a deposition pressure of 20 mTorr, as discussed before. SEM and XRD were used to study the morphology and the crystalline structure of the CdTe films. Figure 3a and 3b show the top view SEM results for the CdTe/CdS/ITO and CdTe/CdS/SiO_2, respectively. No effect on the CdTe grain morphology for films deposited on different substrates is observed. In both cases the XRD results (Figures 3c and 3d) show that the CdTe films have a cubic phase with a preferential orientation in the (111) direction. These results indicate that regardless of the substrate used to deposited the CdS (amorphous or polycrystalline) the CdS growth has little effect on the resulting crystalline phases for the CdTe films.

The substrate temperature during PLD deposition was also investigated. For this study, the CdS films were deposited on 100 nm ITO films and to complete the p-n junction a CdTe film was deposited *in-situ* using 200,000 laser shots for 800 nm thick. Both films (CdS and CdTe) were deposited at 150°C, 220°C, 300°C and 400°C. After deposition, the p-n junction was annealed at 400°C in a N_2 atmosphere for 30 minutes. This annealing process results not only in passivation of grain boundaries, but also increases grain size in CdTe films which in consequence improves reverse leakage current and improve the diode behavior of the CdS/CdTe devices. [3, 14, 18, 21]. To complete the devices, 200 nm of gold on 3 nm of copper contacts [16] were deposited by e-beam deposition and an annealing process at 150°C in a N_2 atmosphere for 30 minutes was carried out after contact deposition. The resulting devices were analyzed electrically studied using I-V and C-V measurements. Figure 4 shows the SEM results for CdTe/CdS films deposited at substrate temperatures ranging from 150°C to 400°C. Annealed films are also shown in Figure 4. The as-deposited films (Figures 4a to 4d) show that higher substrate temperature results in larger CdTe grains, as expected. Figures 4e to 4h show the same samples after annealing at 400°C in N_2 for 30 minutes. Larger crystal growth after annealing is observed for films deposited at lower substrate temperature with negligible impact on the grain size for films deposited at higher substrate temperature. In fact, no effect on grain size is observed for films deposited at 400°C and subsequently annealed at 400°C. Annealing films deposited at low temperature results in CdTe films with cracks that will likely compromise the electrical performance of the CdTe films. Films deposited at 300°C and 400°C have the largest grains while the films deposited at 220°C show the highest impact on the grain size after annealing. The XRD results for the same set of samples are shown in Figure 5. Figure 5a and 5b show the XRD results for films without annealing and Figure 5c and 5d show the XRD results

for annealed films. The CdTe films deposited at 300°C and 400°C do not show substantial changes in the crystal structure and remain cubic and preferentially oriented in the (111) plane. This behavior is also observed in the SEM images. However, for films deposited at 150°C and 220°C an increase in the (111) plane is observed. Before annealing samples deposited at 150°C and 220°C have a cubic structure with preferential growth in the (111) plane and very low (220) orientation. After annealing, there is a substantial increase in the (220) orientation. This change in preferential orientation is likely due to the lateral grain growth of the CdTe during annealing. However, substantial cubic (111) orientation is still observed. For some devices, such as solar cells and sensors, larger grains are preferred since this improves efficiency by reducing grain boundaries which in consequence increased the carrier mean free path and charge collection at the electrodes. From these arguments, the best characteristics are observed for film deposited at 220°C since these films show larger grains and no visible cracks.

Figure 6 shows the electrical characterization for *in-situ* CdTe/CdS diodes fabricated with CdTe grown at 150, 220 and 300 °C and annealed at 400°C in N_2 for 30 minutes. Only one I – V curve for un-annealed samples is shown since un-annealed structures showed poor diode rectification. The poor diode behavior observed for un-annealed films is related to the small grain size, as discussed in the SEM results of Figure 4. The improved in electrical performance after annealing is attributed to grain size increase and grain boundary passivation. Samples deposited at 400°C and annealed at 400°C showed short circuit likely due to the cracks discussed before. P-n devices deposited at 150°C showed higher reverse leakage current, probably due to the cracks originated after annealing, as observed by SEM (Figure 4e). Figure 6b shows the ideality factor and the reverse saturation current for the same set of diodes. For a device with pure thermionic emission mechanism, the ideality factor should be equal to unity, however,

additional mechanism transport, non-ideal contacts behavior, defects on the interfaces or in the bulk increase the ideality factor value [26, 27, 29]. Therefore, the ideality factor for optimized diodes has to be as close as possible to 1. CdTe/CdS p-n diodes deposited at temperatures >220°C showed lower ideality factors. This behavior can be explained by the SEM results discussed in Figures 4f and 4g. The CdTe films deposited at 220°C have a compact structure and lower defect density, resulting in well-behaved diodes. In all cases, the CdTe carrier concentration, as calculated from C-V measurements, was in the order of ~10^{15} cm^{-3}. The C-V measurements were performed at several frequencies and the results are shown in Figure 6c. Given these results, the CdTe films deposited with a substrate temperature of 220°C were selected for the next set of experiments.

In the last part of this study the effect of the annealing temperature after CdTe deposition on CdTe/CdS devices is evaluated. Figure 7 shows CdTe films deposited at 220°C and annealed from 360°C to 440°C for 30 min in N_2. Higher annealing temperature results in larger CdTe grains. This is also evident in Figure 8 (XRD). Samples without annealing have a cubic phase with a preferential (111) orientation. After annealing, the samples have an increase in the cubic (220) phase. Figure 9 shows the electrical characterization results for the various annealing temperatures. As seen in the previous results, samples that did not undergo an annealing process showed a poor rectification behavior and are not reported here. The I-V behavior is very similar for all the annealing temperatures evaluated. Nevertheless, the ideality factor and reverse saturation current seem to be better for devices annealed at T>400°C. When analyzing the carrier concentration data, it appears that the CdTe carrier concentration is independent of the annealing temperature and the frequency during the measurement (Figure 9c).

The RBS results for a CdS/CdTe/CdS structure deposited *in-situ* are shown in Figure 10. Figure 10a shows the experimental and the simulated curves. The dashed line corresponds to the simulation and the open symbols to the experimental data. Very good fitting is reported. Figure 10b shows the depth profile for cadmium, telluride and sulfur along the CdS/CdTe/CdS structure. A Cd/Te atomic ratio close to 1:1 in the CdTe layer is observed, consistent with the stoichiometry character of the CdTe target. However, sulfur concentration > 15% is observed in the CdTe films. Interestedly, the lower S concentration in the CdS under the CdTe is lower and seems to indicate that the S diffusion is coming from the CdS underneath the CdTe film and not form the CdS on top of the CdS. For thick devices, like solar cells and detectors, this inter-diffusion could cause a mismatch in the lattice and increase the CdS/CdTe interface defect density, which can be detrimental for these devices. From an electrical performance perspective, CdTe is a p-type material due to Cd vacancies and excess of Te. Since, S and Te have the same valence any S diffusion into CdTe should act as an isoelectric doping and might not affect carrier concentration. Typically, CdTe carrier concentration is usually $<10^{14}$ cm^{-3} when CdTe is deposited by the Closed-Space Sublimation (CSS) methods. However, it was noted that the carrier concentration in CdTe measured in this work was ~10^{15} cm^{-3} and the increase in carrier concentration might be related to the diffusion of S into the CdTe film that might impact the stochimetricity of the CdTe film. The inset in Figure 10b shows the carrier concentration in thinner CdTe layer (200nm) and compares it with the carrier concentration calculated for the CdTe/CdS devices reported in this paper, where the thickness for CdTe is ~ 800 nm. Sulfur diffusion into the thinner CdTe films results in more than one order of magnitude (~$1x10^{16}$ cm^{-3}) increase in carrier concentration, when compared with the thicker films (~ 4 - $7x10^{16}$ cm^{-3}). Such increase will likely result in a substantial decrease of the p-n depletion layer

Conclusions

This paper reports the impact of processing conditions for CdTe/CdS junctions prepared in-situ. The optimum pressure for CdTe (20 mTorr) results in CdTe films with optimum morphology and no stress in the films. The CdTe films have a preferential orientation in the (111) plane and it is substrate independent. Optimum deposition and annealing temperature are 220°C and 400°C, respectively. These conditions result in CdTe films with carrier concentration ~10^{15} cm^{-3}. This carrier concentration value is higher than CdTe deposited by CSS and might be related to lower efficiencies reported for solar cells fabricated with CdTe deposited PLD compared with those deposited by CSS. RBS analyses show high sulfur diffusion from CdS into the CdTe films that might be responsible for the higher carrier concentration of the CdTe films. *In-situ* growth results on diodes with a rectification factor of ~ 10^5, an ideality factor < 2, and a reverse saturation current ~10^{-8} A. This low reverse current can enable the CdS/CdTe junction as a good photo detector.

4. Acknowledgements

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5. References

[1] Z. Bai, L. Wan, Z. Hou, D. Wang, Effect of CdCl2 annealing treatment on CdS thin films and CdTe/CdS thin film solar cells, Physica Status Solidi C: Current Topics in Solid State Physics, Vol 8, No 2, 8 (2011).
[2] F. de Moure-Flores, J.G. Quinones-Galvan, A. Guillen-Cervantes, J.S. Arias-Ceron, A. Hernandez-Hernandez, J. Santoyo-Salazar, J. Santos-Cruz, S.A. Mayen-Hernandez, M.d.l.L. Olvera, J.G. Mendoza-Alvarez, M. Melendez-Lira, G. Contreras-Puente, CdTe thin films grown by pulsed laser deposition using powder as target: Effect of substrate temperature, Journal of Crystal Growth, 386 (2014) 27-31.
[3] I. Irfan, H. Lin, W. Xia, H.N. Wu, C.W. Tang, Y. Gao, The effect of MoOx inter-layer on thin film CdTe/CdS solar cell, Solar Energy Materials and Solar Cells, 105 (2012) 86-89.
[4] T. Aramoto, F. Adurodija, Y. Nishiyama, T. Arita, A. Hanafusa, K. Omura, A. Morita, A new technique for large-area thin film CdS/CdTe solar cells, Solar Energy Materials and Solar Cells, 75 (2003) 211-217.

[5] S. Neretina, R.A. Hughes, N.V. Sochinskii, M. Weber, K.G. Lynn, J. Wojcik, G.N. Pearson, J.S. Preston, P. Mascher, Growth of CdTe/Si(100) thin films by pulsed laser deposition for photonic applications, Journal of Vacuum Science & Technology A, 24 (2006) 606-611.
[6] A. Guillen-Cervantes, H. Silva-Lopez, M. Becerril-Silva, J.S. Arias-Ceron, E. Campos-Gonzalez, A.C. Medina-Torres, O. Zelaya-Angel, Photoluminescence of CdTe nanocrystals grown by pulsed laser ablation on a template of Si nanoparticles, Applied Physics a-Materials Science & Processing, 118 (2015) 1039-1042.
[7] A. Yeremyan, H. Avetisyan, K. Aviyan, G. Vardanyan, A. Khachatryan, Pulsed laser deposition of layers and nanostructures based on cadmium telluride and bismuth, in: K.A. Valiev, A.A. Orlikovsky (Eds.) Micro- and Nanoelectronics 2007, 2008.
[8] W.C. Barber, J.C. Wessel, E. Nygard, J.S. Iwanczyk, Energy dispersive CdTe and CdZnTe detectors for spectral clinical T and NDT applications, Nuclear Instruments & Methods in Physics Research Section a-Accelerators Spectrometers Detectors and Associated Equipment, 784 (2015) 531-537.
[9] T. Koenig, J. Schulze, M. Zuber, K. Rink, J. Butzer, E. Hamann, A. Cecilia, A. Zwerger, A. Fauler, M. Fiederle, U. Oelfke, Imaging properties of small-pixel spectroscopic x-ray detectors based on cadmium telluride sensors, Physics in Medicine and Biology, 57 (2012) 6743-6759.
[10] Q. Ma, H. Cui, X. Su, Highly sensitive gaseous formaldehyde sensor with CdTe quantum dots multilayer films, Biosensors & Bioelectronics, 25 (2009) 839-844.
[11] J.W. Murphy, L. Smith, J. Calkins, G.R. Kunnen, I. Mejia, K.D. Cantley, R.A. Chapman, J. Sastre-Hernandez, R. Mendoza-Perez, G. Contreras-Puente, D.R. Allee, M. Quevedo-Lopez, B. Gnade, Thin film cadmium telluride charged particle sensors for large area neutron detectors, Applied Physics Letters, 105 (2014).
[12] M. Filipenko, T. Gleixner, G. Anton, J. Durst, T. Michel, Characterization of the energy resolution and the tracking capabilities of a hybrid pixel detector with CdTe-sensor layer for a possible use in a neutrinoless double beta decay experiment, European Physical Journal C, 73 (2013).
[13] J.-f. Han, G.-h. Fu, V. Krishnakumar, C. Liao, W. Jaegermann, CdS annealing treatments in various atmospheres and effects on performances of CdTe/CdS solar cells, Journal of Materials Science-Materials in Electronics, 24 (2013) 2695-2700.
[14] N.R. Paudel, A.D. Compaan, Y. Yan, Sputtered CdS/CdTe solar cells with MoO3-x/Au back contacts, Solar Energy Materials and Solar Cells, 113 (2013) 26-30.
[15] A. Bylica, P. Sagan, I. Virt, A. Bester, I. Stefaniuk, M. Kuzma, Layers of CdTe and CdS obtained by PLD on ITO substrates, Thin Solid Films, 511 (2006) 439-442.
[16] A. Compaan, C.N. Tabory, M. Shao, Y. Li, A. Fischer, Z. Feng, R.G. Bohn, CADMIUM TELLURIDE THIN-FILM SOLAR-CELLS BY PULSED-LASER DEPOSITION, in: J.C. Miller, D.B. Geohegan (Eds.) Laser Ablation: Mechanisms and Applications-Ii, 1994, pp. 225-230.
[17] C. Ding, Z. Ming, B. Li, L. Feng, J. Wu, Preparation and characterization of pulsed laser deposited CdTe thin films at higher FTO substrate temperature and in Ar + O-2 atmosphere, Materials Science and Engineering B-Advanced Functional Solid-State Materials, 178 (2013) 801-806.
[18] P. Hu, B. Li, L. Feng, J. Wu, H. Jiang, H. Yang, X. Xiao, Effects of the substrate temperature on the properties of CdTe thin films deposited by pulsed laser deposition, Surface & Coatings Technology, 213 (2012) 84-89.
[19] S. Keitoku, H. Ezumi, PREPARATION OF CDS/CDTE SOLAR-CELL BY LASER-ABLATION, Solar Energy Materials and Solar Cells, 35 (1994) 299-303.
[20] B. Li, J. Liu, G. Xu, R. Lu, L. Feng, J. Wu, Development of pulsed laser deposition for CdS/CdTe thin film solar cells, Applied Physics Letters, 101 (2012).
[21] Z. Ming, C. Ding, B. Li, L. Feng, J. Wu, Study of Ar + O-2 deposition pressures on properties of pulsed laser deposited CdTe thin films at high substrate temperature, Journal of Materials Science-Materials in Electronics, 25 (2014) 1901-1907.

[22] N. Hernandez-Como, V. Martinez-Landeros, I. Mejia, F.S. Aguirre-Tostado, C.D. Nascimento, G.D. Azevedo, C. Krug, M.A. Quevedo-Lopez, Defect control in room temperature deposited cadmium sulfide thin films by pulsed laser deposition, Thin Solid Films, 550 (2014) 665-668.
[23] B. Maniscalco, A. Abbas, J.W. Bowers, P.M. Kaminski, K. Bass, G. West, J.M. Walls, The activation of thin film CdTe solar cells using alternative chlorine containing compounds, Thin Solid Films, 582 (2015) 115-119.
[24] S.K. Pandey, U. Tiwari, R. Raman, C. Prakash, V. Krishna, V. Dutta, K. Zimik, Growth of cubic and hexagonal CdTe thin films by pulsed laser deposition, Thin Solid Films, 473 (2005) 54-57.
[25] B. Ghosh, S. Hussain, D. Ghosh, R. Bhar, A.K. Pal, Studies on CdTe films deposited by pulsed laser deposition technique, Physica B-Condensed Matter, 407 (2012) 4214-4220.
[26] E. Coskun, H.H. Gullu, I. Candan, O. Bayrakli, M. Parlak, C. Ercelebi, Device behavior of an In/p-Ag(Ga,In)Te-2/n-Si/Ag heterojunction diode, Materials Science in Semiconductor Processing, 34 (2015) 138-145.
[27] A.S. Kavasoglu, O. Birgi, N. Kavasoglu, G. Oylumluoglu, A.O. Kodolbas, R. Kangi, O. Yilmaz, Electrical characterization of a-Si:H(n)/c-Si(p) structure, Journal of Alloys and Compounds, 509 (2011) 9394-9398.
[28] G.K. Rao, K.V. Bangera, G.K. Shivakumar, Studies on vacuum deposited p-ZnTe/n-CdTe heterojunction diodes, Solid-State Electronics, 56 (2011) 100-103.
[29] M. Caglar, F. Yakuphanoglu, Fabrication and electrical characterization of flower-like CdO/p-Si heterojunction diode, Journal of Physics D-Applied Physics, 42 (2009).

List of figure captions

Figure 1. Effect of PLD deposition pressure ((a) 1mT, (b) 10mT, (c) 20mT, (d) 50mT and (e) 100mT) on morphology of CdTe films deposited at room temperature.

Figure 2. (a) Effect of PLD deposition pressure on crystalline structures of CdTe films deposited at room temperature. (b) The XRD patterns for 2θ values show the mixture of phases. Lower pressure reduces the (101) hexagonal CdTe phase.

Figure 3. Amorphous (SiO_2) and polycrystalline substrates (ITO) with a 100 nm thick CdS films and CdTe deposited on top are shown. Figures 3a and 3b show SEM results. Figures 3c and 3d show XRD results. For reference the XRD for ITO is also shown.

Figure 4. Effect of deposition temperature on the morphology of CdTe/CdS films. Samples were deposited at (a) 150°C, (b) 220°C, (c) 300°C and (d) 400°C. Figure 4e, 4f, 4g and 4h shows the films after annealing at 400°C for 30 minutes in N_2 atmosphere.

Figure 5. Effect of deposition temperature on the crystalline structure of CdTe/CdS films. Films in Figure 5a and 5b were deposited at 150°C, 220°C, and 300°C and 400°C. In Figure 5c and 5d, the samples were annealed at 400°C for 30 minutes in N_2 atmosphere after deposition. Detailed analyses of the XRD patterns show the (200) phase increasing after annealing.

Figure 6. Effect of deposition temperature on the electrical properties of CdTe/CdS diodes. Un-annealed diodes showed poor rectifier behavior and samples deposited at 400°C were a short circuit. (a) I-V raw data (Inset shows the diode structure for the I-V and C-V measurement), (b) Ideality factor and reverse saturation current, and (c) carrier concentration extracted from C-V measurements.

Figure 7. Effect of deposition temperature on the morphology of CdTe/CdS films. Samples were deposited at 220°C. (a) as-deposited and annealed at (b) 360°C, (c) 400°C and (d) 440°C for 30 minutes in N_2.

Figure 8. (a) Effect of the deposition temperature on the crystalline structure of CdTe/CdS films. Samples were deposited at 220°C and then annealed at 360°C, 400°C and 440°C for 30 minutes in N2 after deposition. (b) XRD patterns for 2θ values show the increase of the phase (220) after the annealing process.

Figure 9. Effect of annealing temperature on the electrical behavior of CdTe/CdS diodes. Un-annealed films did not have rectification behavior. (a) I-V results, (b) ideality factor and reverse saturation current, and (c) carrier concentration extracted from the C-V measurements.

Figure 10. (a) Fitting between experimental and simulation from RBS raw data. The inset shows the device structure used for the RBS measurement). (b) Atomic concentration depth profile for the CdS/CdTe/CdS films extracted from the fitting of the RBS data. The inset shows the carrier concentration for CdTe/CdS devices using different CdTe thickness layer.

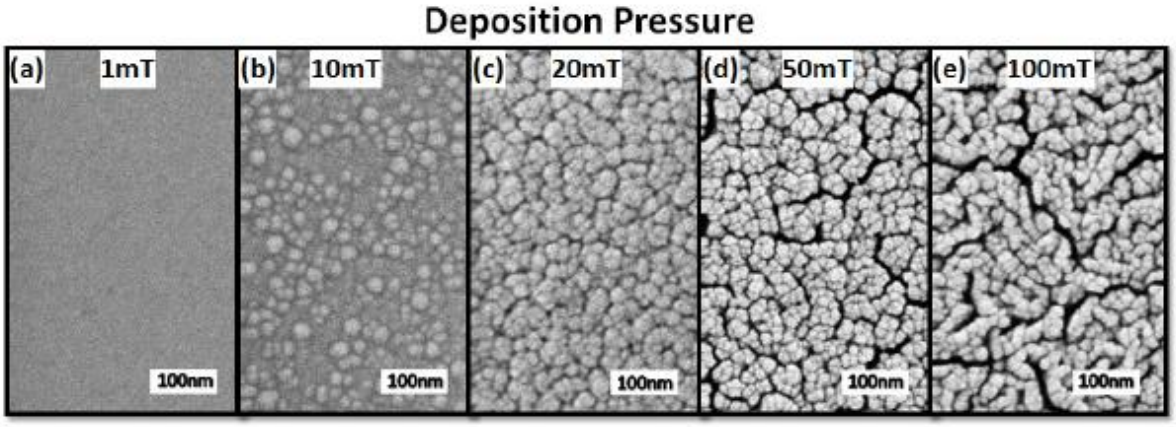

Figure 1. Effect of PLD deposition pressure ((a) 1mT, (b) 10mT, (c) 20mT, (d) 50mT and (e) 100mT) on morphology of CdTe films deposited at room temperature.

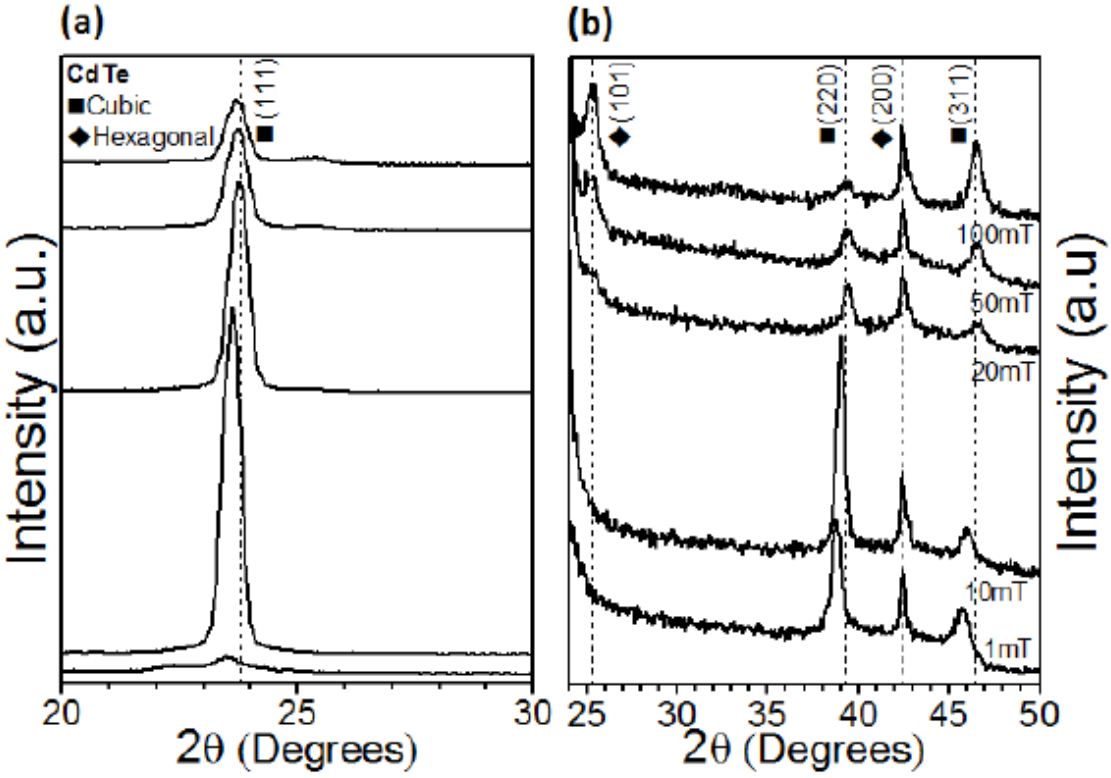

Figure 2. (a) Effect of PLD deposition pressure on crystalline structures of CdTe films deposited at room temperature. (b) The XRD patterns for 2θ values show the mixture of phases. Lower pressure reduces the (101) hexagonal CdTe phase.

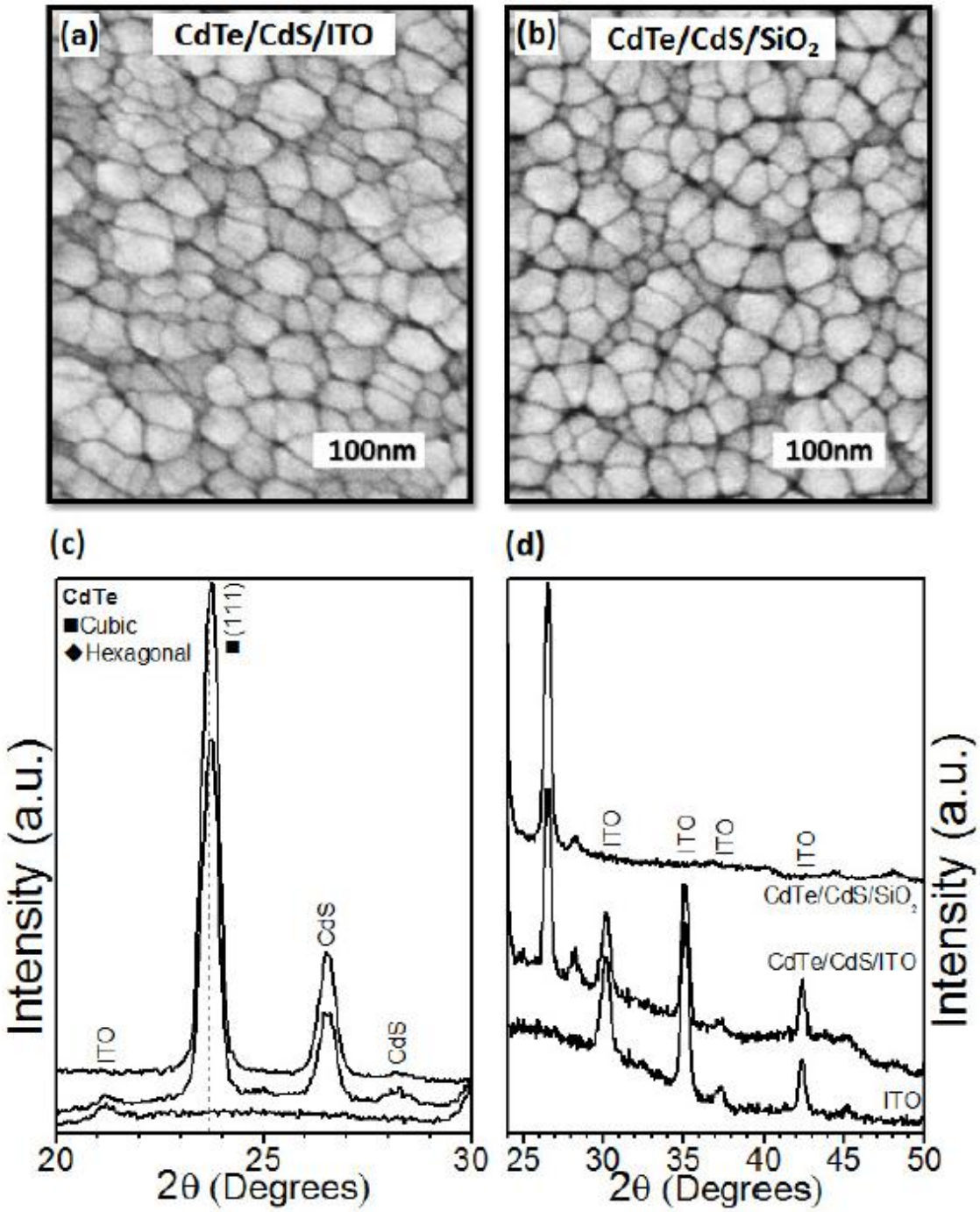

Figure 3. Amorphous (SiO_2) and polycrystalline substrates (ITO) with a 100 nm thick CdS films and CdTe deposited on top are shown. Figures 3a and 3b show SEM results. Figures 3c and 3d show XRD results. For reference the XRD for ITO is also shown.

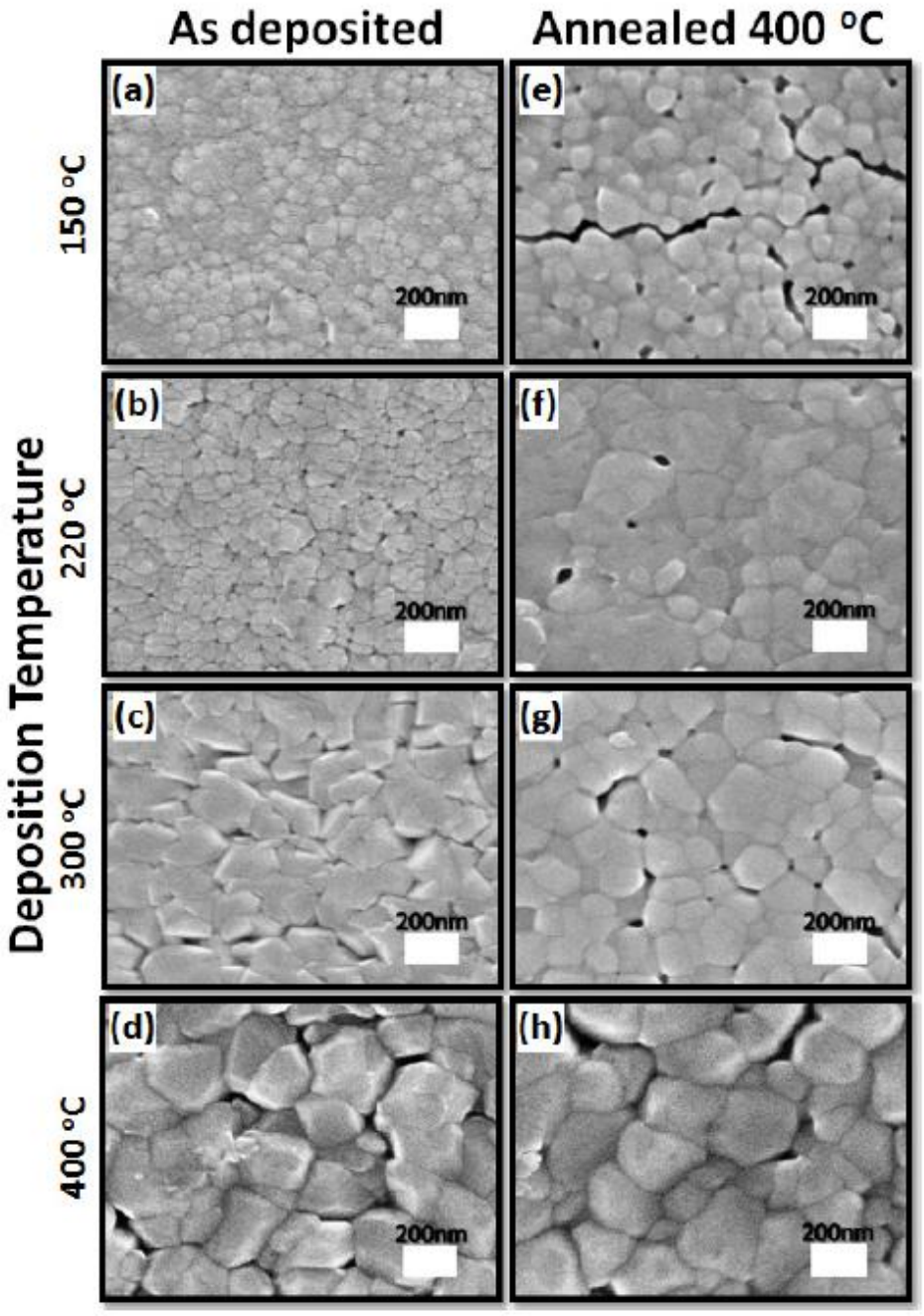

Figure 4. Effect of deposition temperature on the morphology of CdTe/CdS films. Samples were deposited at (a) 150°C, (b) 220°C, (c) 300°C and (d) 400°C. Figure 4e, 4f, 4g and 4h shows the films after annealing at 400°C for 30 minutes in N_2 atmosphere.

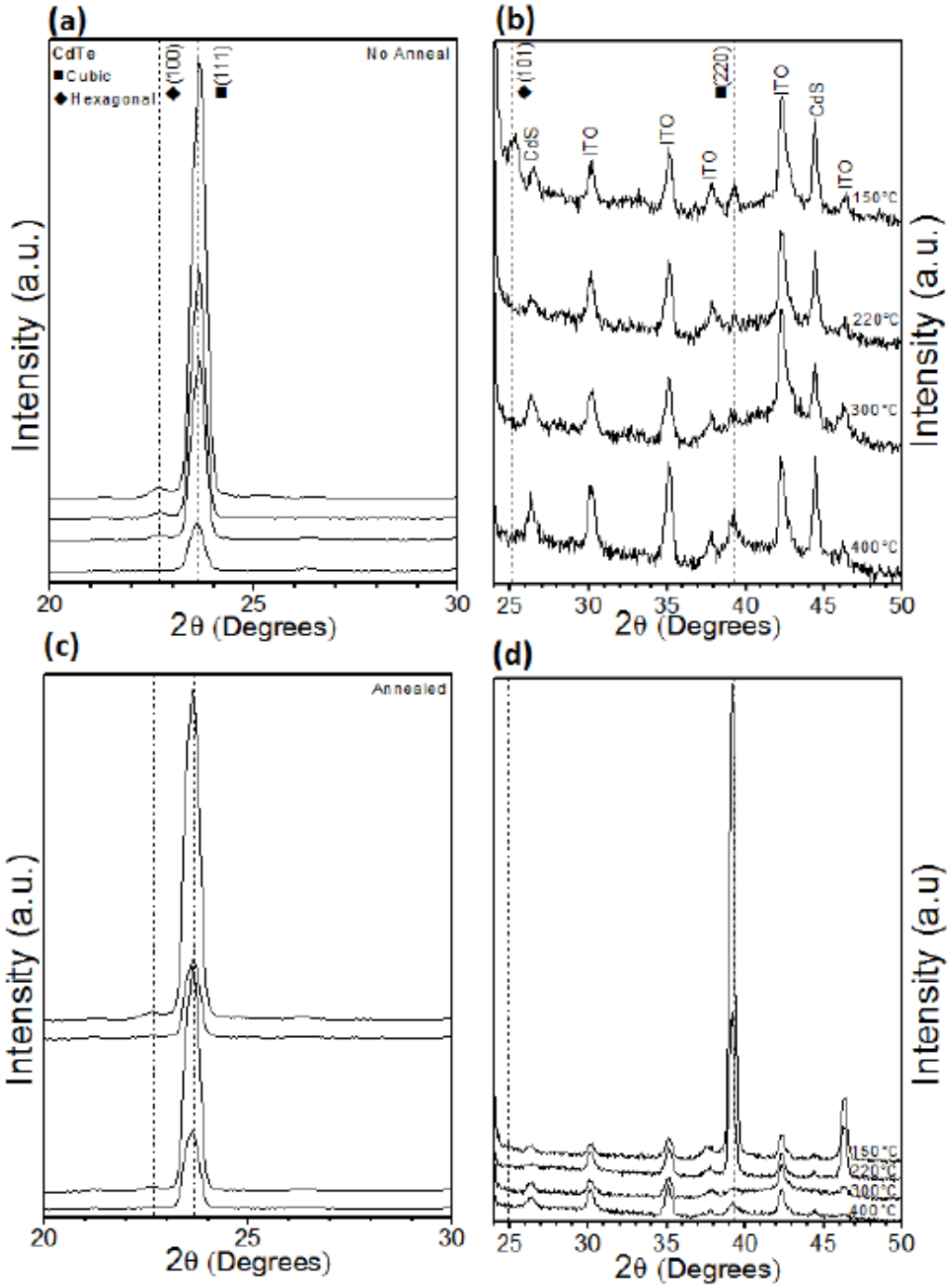

Figure 5. Effect of deposition temperature on the crystalline structure of CdTe/CdS films. Films in Figure 5a and 5b were deposited at 150°C, 220°C, and 300°C and 400°C. In Figure 5c and 5d, the samples were annealed at 400°C for 30 minutes in N_2 atmosphere after deposition. Detailed analyses of the XRD patterns show the (200) phase increasing after annealing.

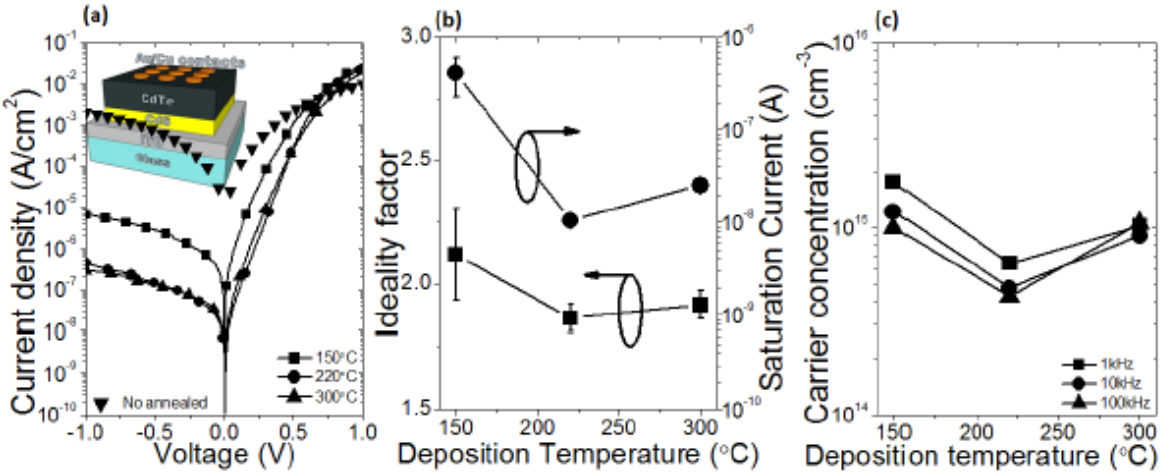

Figure 6. Effect of deposition temperature on the electrical properties of CdTe/CdS diodes. Un-annealed diodes showed poor rectifier behavior and samples deposited at 400°C were a short circuit. (a) I-V raw data (Inset shows the diode structure for the I-V and C-V measurement), (b) Ideality factor and reverse saturation current, and (c) carrier concentration extracted from C-V measurements.

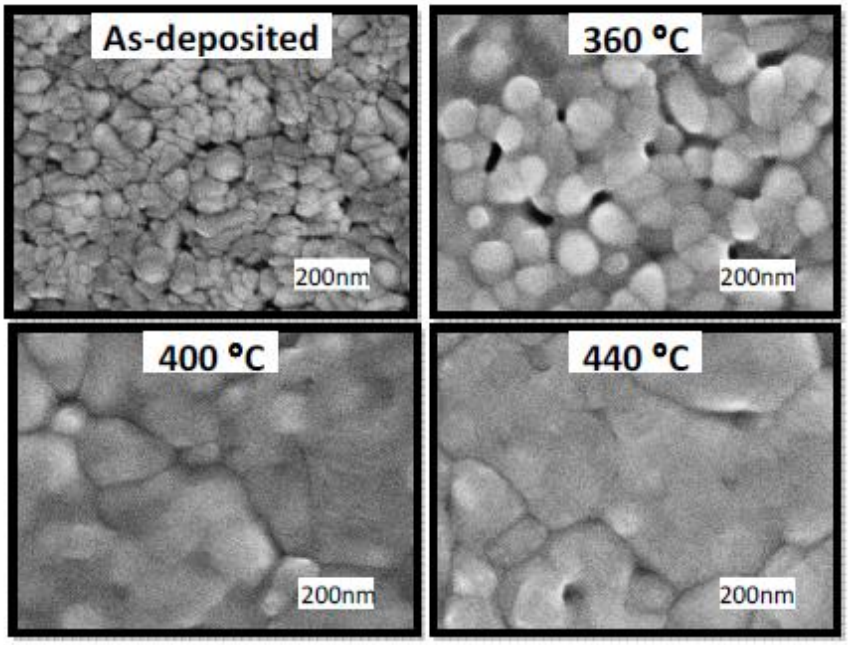

Figure 7. Effect of deposition temperature on the morphology of CdTe/CdS films. Samples were deposited at 220°C. (a) as-deposited and annealed at (b) 360°C, (c) 400°C and (d) 440°C for 30 minutes in N_2.

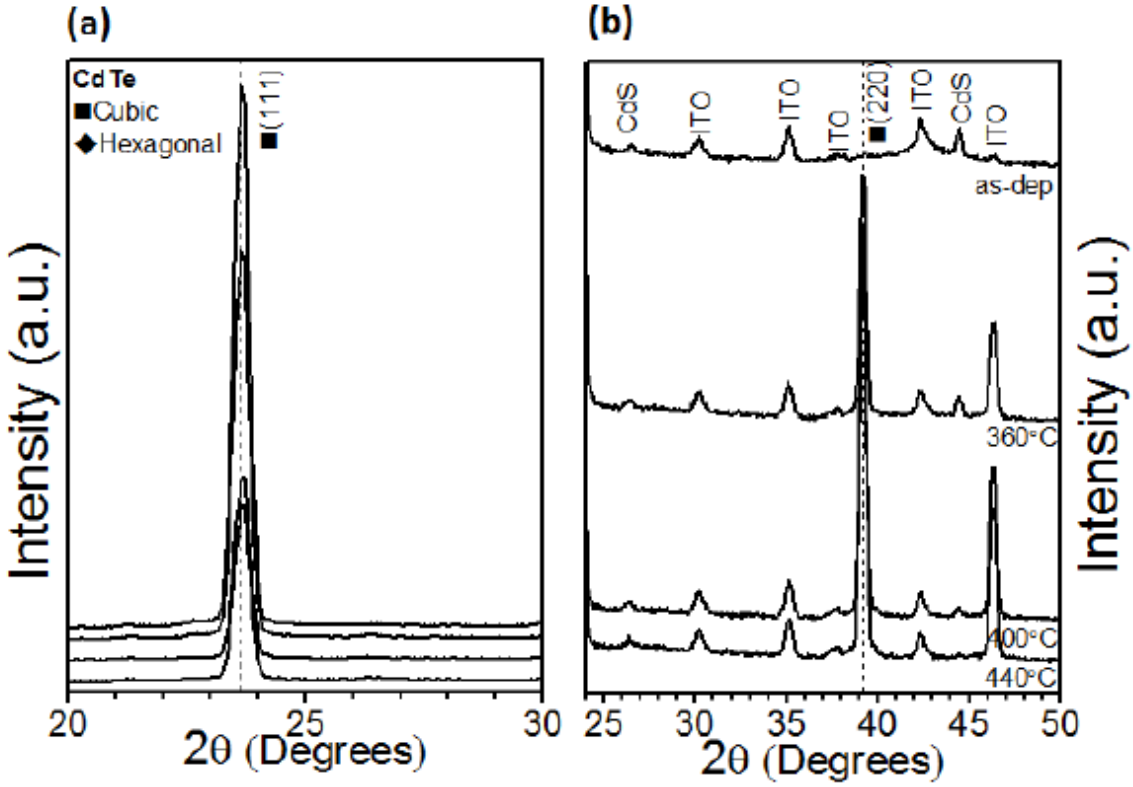

Figure 8. (a) Effect of the deposition temperature on the crystalline structure of CdTe/CdS films. Samples were deposited at 220°C and then annealed at 360°C, 400°C and 440°C for 30 minutes in N_2 after deposition. (b) XRD patterns for 2θ values show the increase of the phase (220) after the annealing process.

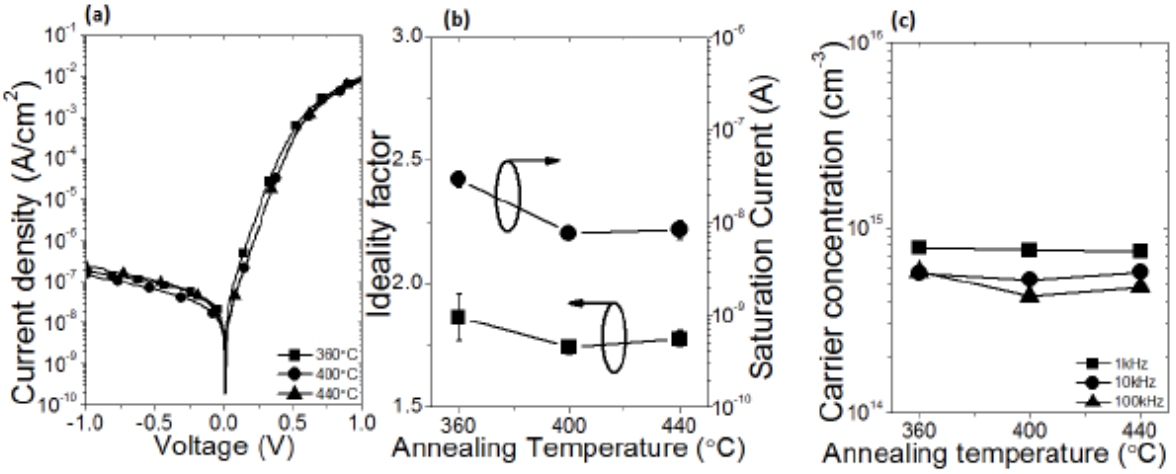

Figure 9. Effect of annealing temperature on the electrical behavior of CdTe/CdS diodes. Un-annealed films did not have rectification behavior. (a) I-V results, (b) ideality factor and reverse saturation current, and (c) carrier concentration extracted from the C-V measurements.

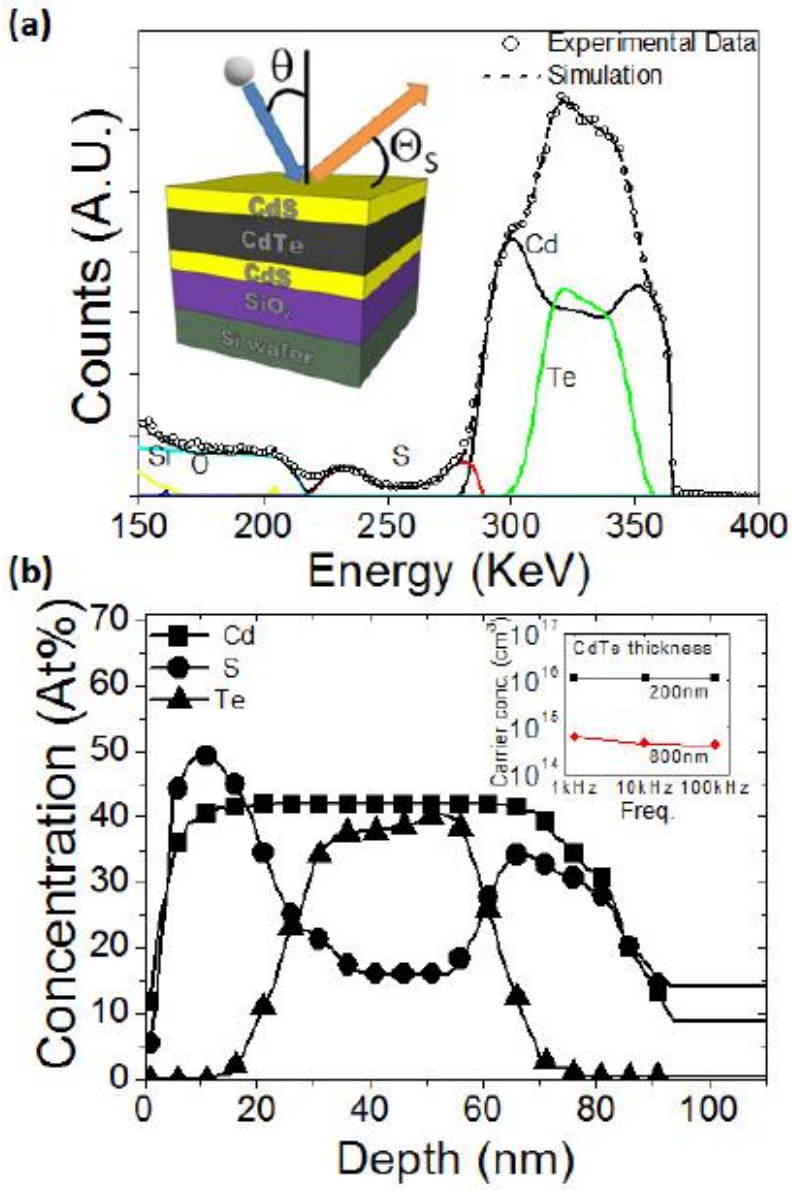

Figure 10. (a) Fitting between experimental and simulation from RBS raw data. The inset shows the device structure used for the RBS measurement). (b) Atomic concentration depth profile for the CdS/CdTe/CdS films extracted from the fitting of the RBS data. The inset shows the carrier concentration for CdTe/CdS devices using different CdTe thickness layer.

Highlights

- In situ Pulse laser deposited CdTe/CdS heterojunctions with sharp interfaces
- 220 °C deposition and 400 °C anneal yield diodes with very low reverse currents.
- RBS results show sulfur diffusion from CdS into the CdTe films
- These diodes are ideal for photodetectors given the low reverse current