Embellishments of the present disclosure include nanowire field-effect transistors, systems for temperature history detection, methods for thermal history detection, a matrix of field effect transistors, and the like.

**Abstract**

1. **Start**
2. Determine a transition temperature of a volume of a nanowire
3. Test a polarity of the nanowire
4. Nanowire exhibiting n-type conduction?
   - **N**
     - Determine that the nanowire has not been exposed to the transition temperature
   - **Y**
     - Determine that the nanowire has been exposed to the transition temperature
5. **End**
**FIG. 4A**

*Graph showing I_Ds (μA) vs V_DS (V) for p-type SnO NW FET.*

**FIG. 4B**

*Graph showing I_Ds (μA) vs V_DS (V) for n-type SnO_2 NW FET after 180 °C exposure.*
Start

Determine a transition temperature of a volume of a nanowire

Test a polarity of the nanowire

Nanowire exhibiting n-type conduction?

No

Determine that the nanowire has not been exposed to the transition temperature

Yes

Determine that the nanowire has been exposed to the transition temperature

End

FIG. 7
TABLE 1. Hall Mobility, Carrier Density, and Film Conductivity As Extracted from Room Temperature Hall Effect Measurements

<table>
<thead>
<tr>
<th>$O_{2p}$ Dep. Pressure</th>
<th>1.5 mTorr</th>
<th>1.7 mTorr</th>
<th>1.8 mTorr</th>
<th>1.9 mTorr</th>
<th>2.0 mTorr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobility (cm²/V·s)</td>
<td>n</td>
<td>9.60</td>
<td>14.48</td>
<td>17.22</td>
<td>17.01</td>
</tr>
<tr>
<td>Carrier Density (cm⁻³)</td>
<td>n</td>
<td>2.42E+17</td>
<td>2.57E+17</td>
<td>3.12E+17</td>
<td>3.33E+17</td>
</tr>
<tr>
<td>Conductivity (S/cm)</td>
<td>0.2379</td>
<td>0.2996</td>
<td>0.3139</td>
<td>0.3139</td>
<td>0.3139</td>
</tr>
<tr>
<td>Mobility (cm²/V·s)</td>
<td>10.43</td>
<td>13.97</td>
<td>18.71</td>
<td>8.79</td>
<td>4.45</td>
</tr>
<tr>
<td>Carrier Density (cm⁻³)</td>
<td>2.29E+17</td>
<td>2.38E+17</td>
<td>2.78E+17</td>
<td>2.78E+17</td>
<td>3.33E+17</td>
</tr>
<tr>
<td>Conductivity (S/cm)</td>
<td>0.3638</td>
<td>0.3196</td>
<td>0.3560</td>
<td>0.3300</td>
<td>0.2866</td>
</tr>
<tr>
<td>Mobility (cm²/V·s)</td>
<td>9.83</td>
<td>10.16</td>
<td>11.21</td>
<td>4.45</td>
<td>2.25</td>
</tr>
<tr>
<td>Carrier Density (cm⁻³)</td>
<td>7.53E+16</td>
<td>1.44E+17</td>
<td>7.42E+16</td>
<td>5.13E+16</td>
<td>2.3E+17</td>
</tr>
<tr>
<td>Conductivity (S/cm)</td>
<td>0.1195</td>
<td>0.2360</td>
<td>0.1665</td>
<td>0.2366</td>
<td>0.0636</td>
</tr>
<tr>
<td>Mobility (cm²/V·s)</td>
<td>9.33</td>
<td>7.48</td>
<td>5.68</td>
<td>3.82</td>
<td>1.95</td>
</tr>
<tr>
<td>Carrier Density (cm⁻³)</td>
<td>7.62E+16</td>
<td>1.91E+17</td>
<td>4.32E+16</td>
<td>9.77E+16</td>
<td>6.68E+16</td>
</tr>
<tr>
<td>Conductivity (S/cm)</td>
<td>0.1144</td>
<td>0.2305</td>
<td>0.6075</td>
<td>0.1468</td>
<td>X</td>
</tr>
<tr>
<td>Mobility (cm²/V·s)</td>
<td>4.82</td>
<td>4.50</td>
<td>4.00</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Carrier Density (cm⁻³)</td>
<td>7.83E+16</td>
<td>6.32E+16</td>
<td>5.73E+16</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Conductivity (S/cm)</td>
<td>0.0607</td>
<td>0.0451</td>
<td>0.0480</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

* The reported value is the average of 3 measurements performed on different samples of every deposition condition. A maximum Hall mobility of 10.7 cm²/V·s is obtained at 1.8 mTorr, 9% $O_{2p}$. 

**FIG. 9A**

**FIG. 9B**
FIG. 12A

FIG. 12B
FIG. 13A
THERMAL HISTORY DEVICES, SYSTEMS FOR THERMAL HISTORY DETECTION, AND METHODS FOR THERMAL HISTORY DETECTION

CLAIM OF PRIORITY TO RELATED APPLICATION

[0001] This application claims priority to co-pending U.S. provisional application entitled “THERMAL HISTORY DEVICES, SYSTEMS FOR THERMAL HISTORY DETECTION, AND METHODS FOR THERMAL HISTORY DETECTION” having Ser. No. 61/908,906, filed on Nov. 26, 2013, which is entirely incorporated herein by reference.

BACKGROUND

[0002] Many items are constantly exposed to varying temperature extremities during production, storage, and transportation. Typically, a thermal history sensor device monitor whether a portion of an item has been exposed to a certain maximum temperature. However, such monitoring often requires the use of power. In situations where power is not readily available, systems and methods of thermal history detection without consuming power may be necessary.

SUMMARY

[0003] Embodiments of the present disclosure include nanowire field-effect transistors, systems for temperature history detection, methods for thermal history detection, a matrix of field effect transistors, and the like.

[0004] An embodiment of the system for temperature history detection, among others, includes: at least one field effect transistor comprising a substrate comprising: a gate electrode made of a material with conductive properties; a plurality of gate dielectrics positioned in proximity to the gate electrode, wherein the gate dielectrics are insulators; and a plurality of nanowires, wherein an individual one of the nanowires is at least partially connected to a source electrode at one end and a drain electrode at another end, wherein the individual one of the nanowires has different volume dimensions than another individual one of the nanowires, and the individual one of the nanowires is configured to convert from p-type conduction to n-type conduction at a transition temperature.

[0005] An embodiment of the method for thermal history detection, among others, includes: determining a transition temperature that measures a temperature when a nanowire transitions from a p-type conduction to a n-type conduction, wherein the transition temperature is associated with a volume of the nanowire; testing a polarity of a field effect transistor comprising the volume of the nanowire; and determining whether the nanowire has been exposed to the transition temperature.

[0006] An embodiment of the matrix of field effect transistors, among others, includes: a substrate; a gate electrode positioned in proximity to the substrate; a gate dielectric placed in proximity to a source electrode and a drain electrode; a first nanowire with a first volume dimension, wherein one end of the first nanowire is coupled to the source electrode and another end of the first nanowire is coupled to the drain electrode; and a second nanowire with a second volume dimension, wherein one end of the second nanowire is coupled to the source electrode and another end of the second nanowire is coupled to the drain electrode, wherein the first volume dimension is different from the second volume dimension, wherein the first volume dimension and the second volume dimension are associated with a transition temperature that measures a temperature when the nanowire transitions from p-type conduction to n-type conduction.

BRIEF DESCRIPTION OF DRAWINGS

[0007] Further aspects of the present disclosure will be more readily appreciated upon review of the detailed description of its various embodiments, described below, when taken in conjunction with the accompanying drawings.

[0008] FIG. 1 illustrates a structure of a nanowire field effect transistor.

[0009] FIG. 2 illustrates the dimensions of the nanowire of the nanowire field effect transistor described in FIG. 1.

[0010] FIG. 3 illustrates a thermal history device with a set of nanowire field effect transistors.

[0011] FIG. 4A is a graph illustrating output characteristics of the nanowire field effect transistor described in FIG. 1 exhibiting p-type conduction.

[0012] FIG. 4B is a graph illustrating output characteristics of the nanowire field effect transistor device described in FIG. 4A exhibiting n-type conduction as a result of a phase transformation.

[0013] FIG. 5 is a graph illustrating the transfer characteristics of the nanowire field transistor described in FIG. 1.

[0014] FIG. 6 is a graph illustrating a phase transformation transition temperature as a function of nanowire volume dimensions.

[0015] FIG. 7 is a flowchart illustrating one example of a functionality implemented by a user of a thermal history device comprising at least one nanowire according to various embodiments of the present disclosure.

[0016] FIG. 8A is a phase stability map to obtain p-type tin monoxide.

[0017] FIG. 8B illustrates X-ray diffraction (XRD) patterns showing tin monoxide phase formation dependence.

[0018] FIG. 8C illustrates XRD patterns showing deposition pressure dependence.

[0019] FIG. 8D illustrates the XRD patterns described in FIG. 8C in a narrower range.

[0020] FIG. 9A is a graph illustrating room temperature Hall mobility of films deposited in a pressure range.

[0021] FIG. 9B is a table that illustrates further details of the Hall mobility, carrier density, and film conductivity shown in FIG. 9A.

[0022] FIGS. 10A-D illustrate conceptual designs of fabricated devices of the various embodiments disclosed herein.

[0023] FIGS. 11A-D are graphs illustrating output and transfer characteristics of thermal history devices fabricated on a fully transparent material.

[0024] FIGS. 11C-D are graphs illustrating output and transfer characteristics of thermal history devices fabricated on a flexible material.

[0025] FIG. 12A is a graph illustrating linear field effect mobility as a function of oxygen partial pressure.

[0026] FIG. 12B is a graph illustrating threshold voltage comparison for fully transparent and flexible devices.

[0027] FIG. 12C is a graph illustrating linear field effect mobility as a function of width-to-length ratios for transparent devices.

[0028] FIG. 12D is a graph illustrating multiple, dual sweep transfer curves for a thermal history device.
FIGS. 12E-F illustrate atomic force microscopy surface profiles for glass and plastic substrates, respectively.

FIG. 13A is a graph illustrating a comparison of reported field effect mobility versus maximum processing temperature for leading p-type oxides.

FIG. 13B is a graph illustrating transmission spectra of components of a thin film transistor.

FIG. 13C is a trace plot of optical band gap extraction.

DETAILED DESCRIPTION

This disclosure is not limited to particular embodiments described, and as such may, of course, vary. The terminology used herein serves the purpose of describing particular embodiments only, and is not intended to be limiting, since the scope of the present disclosure will be limited only by the appended claims.

Where a range of values is provided, each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range and any other stated or intervening value in that stated range, is encompassed within the disclosure. The upper and lower limits of these smaller ranges may independently be included in the smaller ranges and are also encompassed within the disclosure, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included in the disclosure.

Embodiments of the present disclosure will employ, unless otherwise indicated, techniques of material science, chemistry, physics, and the like, which are within the skill of the art. Such techniques are explained fully in the literature.

The following examples are put forth so as to provide those of ordinary skill in the art with a complete disclosure and description of how to perform the methods and use the compositions and compounds disclosed and claimed herein. Efforts have been made to ensure accuracy with respect to numbers (e.g., amounts, temperature, etc.), but some errors and deviations should be accounted for. Unless otherwise indicated, parts are parts by weight, temperature is in °C, and pressure is at or near atmospheric. Standard temperature and pressure are defined as 20° C. and 1 atmosphere.

Before the embodiments of the present disclosure are described in detail, it is to be understood that, unless otherwise indicated, the present disclosure is not limited to particular materials, reagents, reaction materials, manufacturing processes, dimensions, frequency ranges, applications, or the like, as such can vary. It is also to be understood that the terminology used herein is for purposes of describing particular embodiments only, and is not intended to be limiting. It is also possible in the present disclosure that steps can be executed in different sequence, wherein this is logically possible. It is also possible that the embodiments of the present disclosure can be applied to additional embodiments involving measurements beyond the examples described herein, which are not intended to be limiting.

It should be noted that, as used in the specification and the appended claims, the singular forms “a,” “an,” and “the” include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to “a support” includes a plurality of supports. In this specification and in the claims that follow, reference will be made to a number of terms that shall be defined to have the following meanings unless a contrary intention is apparent.

Discussion

Embodiments of the present disclosure include nanowire field-effect transistors, systems for temperature history detection, methods for thermal history detection, a matrix of field effect transistors, and the like. In particular, embodiments of the present disclosure relate to nanowire field-effect transistors based on p-type semiconductor material tin monoxide (SnO) of different volumes to be used as thermal history sensors relying on the conversion from p-type conduction to n-type conduction.

In an embodiment, the device structure can include a substrate, either rigid like glass, or flexible like plastic; a gate electrode; a source electrode made of a conductive material; a gate dielectric; and at least one tin monoxide nanowire as an active semiconducting channel.

In an embodiment, the tin monoxide nanowire can be structured as a rectangular cross section with volume dimensions determined by a nanowire planar width, length, and thickness. In an embodiment, the tin monoxide nanowire can have a circular cross-section and have a diameter and length. The thermal history detection system disclosed can include a plurality of tin monoxide nanowire field effect transistors. Each of the nanowire field effect transistors can have at least one nanowire with different widths (or diameter for a circular cross-section) of about 10 nanometers (nm) to about 500 nm, lengths of about 1 micrometer (μm) to 10 μm, and thicknesses of about 5 nm to 50 nm. Each of the nanowires can have different widths, thicknesses, and/or lengths. Alternatively, each of the nanowires can have the same width, thickness, and/or length.

Tin monoxide is a transparent semiconducting oxide that exhibits p-type conduction. As may be appreciated, a p-type semiconducting material has a larger hole concentration than electron concentration. Such a deficiency of electrons results in the holes of the p-type semiconducting material being the major charge carriers. Alternatively, an n-type semiconducting material has a larger electron concentration than hole concentration. In the n-type semiconducting material, electrons are the major charge carriers. As may be appreciated, the major charge carriers may be primarily responsible for transporting current in a semiconductor.

Tin monoxide can be a metastable form of the tin oxides. Tin monoxide can transform into the more thermodynamically stable n-type semiconducting material tin dioxide (SnO2). The temperature required to obtain this conversion can depend on the volume of the tin monoxide nanowire of the field effect transistor. Accordingly, conversion from p-type conduction to n-type conduction can be tuned by varying the width (i.e., diameter), length, and/or thickness of the nanowire in the various embodiments of the nanowire field effect transistor. The conversion from p-type tin monoxide to n-type tin dioxide can be a non-reversible reaction. Additional details are provided in the described description of the figures below.

FIG. 1 illustrates a structure of a nanowire field effect transistor 100. As may be appreciated, a field effect transistor can use an electric field to control the conductivity
of a channel of a charge carrier in a semiconducting material. The field effect transistor can include a semiconducting channel through which charge carriers, electrons or holes, flow from a source to a drain. The semiconducting channel of a field effect transistor can be doped to produce an n-type semiconductor or a p-type semiconductor. The doping of a channel can refer to intentionally introducing impurities into a semiconducting channel for the purpose of modulating its electrical properties. Further details of n-type and p-type semiconductors are described below.

The nanowire field effect transistor 100 can be positioned on a substrate. The substrate can be made of either rigid material, like glass, or flexible material, like plastic substrates, such as polyethylene terephthalate, polyethylene naphthalate, polyimide, or other material with plastic like properties. In one embodiment, the substrate can be opaque, similar to a silicon wafer. As may be appreciated, the substrate can be made of a material suitable to hold the various embodiments of the nanowire field effect transistor disclosed herein.

In one embodiment, the nanowire field effect transistor 100 can include a gate electrode 103, a gate dielectric 106, a source electrode 109, and a drain electrode 112, and at least one nanowire 115. The gate electrode 103, source electrode 109, and drain electrode 112 can be made of any conductive material, such as, but not limited to, titanium, gold, nickel, platinum, indium tin oxide, or aluminum zinc oxide. Alternatively, the gate electrode 103, source electrode 109, and drain electrode 112 can be made of films of silver nanowires or similarly structured films.

As may be appreciated, the gate electrode 103 can control the flow of electrical current between the source electrode 109 and the drain electrode 112. Specifically, the gate electrode 103 can permit electrons to flow through the nanowire field effect transistor 100. The gate electrode 103 can also block electron passage by creating or eliminating a channel between the source electrode 109 and drain electrode 112. Electrons or electron holes can flow from the source electrode 109 to the drain electrode 112 if influenced by an applied voltage.

The gate dielectric 106 can be made of a material with insulating properties, including, but not limited to, aluminum oxide, hafnium oxide, silicon nitride, strontium titanate, titanium oxide, gadolinium oxide, or any organic dielectric such as polyvinylidene difluoride, or polymethyl methacrylate. The gate dielectric 106 can be polarized by an application of an electric field. The gate dielectric 106 can be displaced between the gate and substrate in some embodiments of the disclosed nanowire field effect transistor.

The nanowire 115 can operate as the semiconducting channel of the nanowire field effect transistor 100, where the nanowire 115 functions as the channel through which electrons or electron holes flow from the source electrode 109 to the drain electrode 112. In one embodiment, the nanowire can be a transparent semiconducting oxide that exhibits p-type conduction. Specifically, the nanowire 115 can be a tin monoxide nanowire, and the fabrication of such a tin monoxide nanowire is further described below. Tin monoxide can be a metastable form of the tin oxides. The tin monoxide can transform into the more thermodynamically stable n-type semiconducting material tin dioxide (SnO₂). The temperature required to obtain this conversion can depend on the volume of the tin monoxide nanowire of the field effect transistor 100. Accordingly, conversion from p-type conduction to n-type conduction can be tuned by varying the width, length, and thickness of the nanowire 115 in the various embodiments of the nanowire field effect transistor 100. The conversion from p-type tin monoxide to n-type tin dioxide can be a non-reversible reaction. As may be appreciated, the nanowire 115 can be made of any other semiconducting material sufficient to function as a thermal history sensing nanowire field effect transistor according to the embodiments disclosed herein.

As may be appreciated, the tin monoxide nanowire field effect transistor can be structured as any conventional thin film transistor structure, including, but not limited to, a staggered gate transistor, coplanar gate transistor, staggered top gate transistor, or coplanar top gate transistor. The thermal history detection system disclosed can include a plurality of tin monoxide nanowire field effect transistors 100. Additional details of the embodiments of the nanowire 115 are provided below in FIGS. 2-12 and the Examples associated with them, respectively.

FIG. 2 illustrates the dimensions of the nanowire 115 (FIG. 1) of the nanowire field effect transistor 100 (FIG. 1) described in FIG. 1. The nanowire 115 can include a volume dimension comprising a width 203, a length 206, and a thickness 209. In one embodiment, the nanowire 115 can be a tin monoxide nanowire. As described above, in some embodiments, the tin monoxide nanowire, exhibiting p-type conduction, can undergo a phase transformation into a tin dioxide nanowire, exhibiting n-type conduction, at a certain transition temperature. A user of a thermal history device comprising a tin monoxide nanowire 115 can detect the polarity of the device to see if the maximum temperature the device has been exposed to based on the transition temperature of the nanowire 115.

Different volumes of the tin monoxide nanowire may be required to monitor the maximum temperature that the nanowire 115 has been exposed to. In an embodiment the temperature that can transform the nanowire 115 from a p-type semiconductor to an n-type semiconductor can be about 100°C to 200°C. The volume dimension of the nanowire 115 has a direct relationship with the transition temperature required to phase transform the nanowire 115 from a p-type semiconducting material to an n-type semiconducting material. Accordingly, in one embodiment, the greater the volume dimension of the nanowire 115, the higher the transition temperature required to transform the nanowire 115 from a tin monoxide material to a tin dioxide material.

In an embodiment, the nanowire 115 can be made of any active semiconductor material. In one embodiment, the nanowire 115 can be fabricated as a tin monoxide nanowire by either physical or chemical routes including: diode/radiofrequency reactive sputtering in which in a tin monoxide film is deposited from a tin metal target in a mixed gas atmosphere containing oxygen in a vacuum chamber; radiofrequency sputtering from a tin monoxide target; pulsed laser deposition vacuum chamber either from a tin monoxide target or in a reactive process from a metal target; thermal or electron-beam evaporation of a suitable tin monoxide source; atomic layer deposition using suitable tin monoxide precursors; solution processing techniques like drop casting or spin coating of suitable tin monoxide precursors or tin monoxide solution; chemical vapor deposition techniques involving the evaporation of tin monoxide or tin dioxide, or by another means available to deposit a thin film of semiconducting material on the nanowire 115. Paterning of the tin monoxide nanowire structure can be done by electron-beam lithography to accu-
rately control the dimensions of the tin monoxide active layer. Photolithography can be used to pattern the other components of the device structure.

[0054] FIG. 3 illustrates a thermal history device 300 with a set of nanowire field effect transistors 100 (FIG. 1). In one embodiment, the thermal history device 300 can include a plurality of nanowire field effect transistors 100 structured similarly to that described in FIG. 1. The nanowires 115a-e may each be associated with a volume dimension, similar to the volume dimensions described above in FIG. 2. As illustrated in FIG. 3, each of the nanowires 115a-e can have a different dimension from another nanowire 115a-e. For example, FIG. 3 shows nanowire 115a having a larger width than nanowire 115b and nanowire 115d. As another example, FIG. 3 shows nanowire 115c and nanowire 115f having shorter lengths than nanowire 115a. Because of each of nanowires 115a-e shown in FIG. 3 has a different volume dimension, each nanowire 115a-e can have a different transition temperature, respectively. In another embodiment, each of the nanowires 115a-e can have the same dimension as another nanowire 115a-e. The thermal history device 300 may record one or more temperatures that each nanowire 115a-e in the thermal history device 300 has been exposed to based on the transition temperature associated with the volume dimension of each nanowire 115a-e.

[0055] As may be appreciated, the set of nanowire field effect transistors 100 can be structured in various ways. In one embodiment, the nanowire field effect transistors 100, each with a gate electrode 103, a gate dielectric 106, a source electrode 109, and a drain electrode 112, and at least one nanowire 115, can be positioned separately in varying and/or distant locations throughout an item or substrate. Alternatively, a plurality of source electrodes 109, drain electrodes 112, and nanowires 115 can be displaced upon one gate dielectric 106 in proximity to each gate electrode 103 on a substrate. In another embodiment and as depicted in FIG. 3, one gate electrode 103 can supply the voltage to a plurality of interconnected gate dielectrics 106, source electrodes 109, drain electrodes 112, and nanowires 115.

[0056] In some embodiments, each of the nanowire field effect transistors 100 can include a plurality of nanowires 115 structured as a stack or in any way such that each nanowire 115 is coupled to one source electrode 109 and drain electrode 112 in proximity to a gate dielectric 106 and gate electrode 103. The plurality of nanowire field effect transistors 100 disclosed can be structured as an array, as shown in FIG. 3, a matrix, or in any random or sequenced structure. As may be appreciated, the structure of the nanowire field effect transistor 100 can be any conventional thin film transistor structure, including, but not limited to, a staggered bottom gate transistor, coplanar bottom gate transistor, staggered top gate transistor, or coplanar top gate transistor.

[0057] In an embodiment, the thermal history device 300 disclosed may or may not require power to operate. The thermal history device 300 can be fully transparent and can include either rigid or flexible substrates that can be easily attached to a product where a temperature exposure record is needed. The inexpensive thermal history device 300 can be used to monitor a maximum temperature a product has been exposed to during production, transportation, or storage based on the transition temperature of the nanowire 115 associated with the thermal history device 300.

[0058] FIGS. 4A-B show the electrical characterization of a nanowire field effect transistor 100 (FIG. 1) showing the transition from p-type to n-type conduction after being exposed to a given temperature. Specifically, FIG. 4A is a graph depicting output characteristics of a tin monoxide nanowire field effect transistor showing p-type conduction before being exposed to the transition temperature required to transform the tin monoxide nanowire into a tin dioxide nanowire. As illustrated in FIG. 4A, the tin monoxide nanowire exhibits p-type conducting carrying a negative source to drain current.

[0059] Next, FIG. 4B illustrates output characteristics of the same nanowire field effect transistor 100 (FIG. 1) after being exposed to 180°C. showing n-type conduction as a result of tin monoxide to tin dioxide phase transformation. The tin monoxide nanowire underwent a phase transformation due to exposing the nanowire 115 (FIG. 1) to the transition temperature of 180°C, resulting in a positive source to drain current indicated in FIG. 4B. The tin monoxide nanowire may have been of a certain volume dimension that required the tin monoxide to be exposed to 180°C to undergo phase transformation into tin dioxide.

[0060] FIG. 5 is a graph 500 illustrating an example of transfer characteristics of nanowire field effect transistor 100 (FIG. 1) having a nanowire 115 (FIG. 1) with a width 203 (FIG. 2) of 100 nm, a length 206 (FIG. 2) of 5 μm, and a thickness 209 (FIG. 2) of 20 nm. Transfer characteristic graph 500 includes a tin monoxide plot 503, a tin dioxide plot 506, a tin monoxide leakage 509, and a tin dioxide leakage 512. The tin monoxide plot 503 shows the initial negative gate voltage. The tin dioxide plot 506 shows a positive gate voltage that resulted from the tin monoxide nanowire being exposed to the transition temperature of 180°C. As illustrated in FIG. 5, tin monoxide leakage 509 and tin dioxide leakage 512 indicate that gate leakage currents are very low in some embodiments. Graph 500 may further illustrate the polarity change that can result from exposing the nanowire 115 to a pre-determined transition temperature.

[0061] FIG. 6 shows a graph of p-type tin monoxide to n-type tin dioxide transition temperatures as a function of nanowire 115 (FIG. 1) with a width 203 (FIG. 2) of about 100 nm, a length 206 (FIG. 2) of about 2 μm and a thickness 209 (FIG. 2) of about 10 nm. The transition temperature is a temperature at which a nanowire 115 of a nanowire field effect transistor 100 (FIG. 1) transitions from p-type conduction to n-type conduction. The transition temperature of a nanowire 115 is associated with a volume dimension of the nanowire 115. The volume dimension can include a width 203, a length 206, and a thickness 209. The volume dimension of the nanowire 115 can have a direct relationship with the transition temperature required to phase transform the nanowire 115 from a p-type semiconducting material to an n-type semiconducting material.

[0062] Accordingly, in one embodiment, the greater the volume dimension of the nanowire 115, the higher the transition temperature required to transform the nanowire 115 from a tin monoxide material to a tin dioxide material. FIG. 6 illustrates a specific embodiment of this concept by showing the transition temperature as a function of the nanowire width 203 while keeping the length 206 and thickness fixed 209. Other transition temperatures can be obtained by varying the length 206 or the thickness 209 of the nanowire.
[0063] In one embodiment including a matrix of nanowire field effect transistors 100 (FIG. 1), it is possible to detect the maximum temperature the thermal history device has been exposed to by identifying the conduction polarity of the nanowire 115 (FIG. 1) in the nanowire field effect transistors 100. The nanowire field effect transistor 100 can be designed with pre-configured volume dimensions to convert from p-type conduction to n-type conduction at a pre-determined transition temperatures based on the volume dimensions. For example, a tin monoxide nanowire can convert to a tin dioxide nanowire at a specific transition temperature. A tin monoxide nanowire having a first volume dimension can convert to a tin dioxide nanowire at a different transition temperature than another tin monoxide nanowire having a second volume dimension. By testing the polarity of the nanowire 115, it is possible to determine if nanowire 115 has been exposed to the transition temperature.

[0064] The thermal history device 300 can also be configured to programmatically determine whether each nanowire 115 is exhibiting p-type conduction or n-type conduction. In one embodiment, the thermal history device 300 can physically record the polarity of each nanowire. For example, a physical indicator in proximity to each nanowire 115 can display one color to indicate that the nanowire 115 is exhibiting p-type conduction or display another color to indicate that the nanowire 115 is exhibiting n-type conduction. The user can then determine whether the nanowire 115 has been exposed to the transition temperature based on the color of the physical indicator alone.

[0065] In another embodiment, the thermal history device 300 can be configured to automatically detect when each nanowire 115 converts from p-type conduction to n-type conduction. The thermal history device 300 can include a physical indicator representing whether the nanowire 115 has undergone phase transformation from a p-type semiconducting material to an n-type semiconducting material. In such an embodiment, a user of the thermal history device may not need to detect the polarity of each nanowire to determine if the nanowire 115 has been exposed to the transition temperature. Rather, the user of the thermal history device 300 can determine whether the nanowire 115 has been exposed to the transition temperature by looking at the physical indicator representing such phase transformation for each nanowire.

[0066] In one embodiment, the thermal history device can include a programmable device allowing the user to set a notification when a given maximum temperature has been reached. Such notification can include a flashing light and/or sound alarm that activates when the transition temperature has been reached.

[0067] In some embodiments, the thermal history device 300 can additionally include a timing recorder that records a time at which the nanowire 115 transformed from a p-type semiconductor to an n-type semiconductor. For example, suppose the thermal history device 300 is configured to automatically determine whether each nanowire 115 is exhibiting p-type conduction or n-type conduction. The thermal history device 300 can include a clock that is configured to record the time at which the thermal history device 300 determined that the nanowire 115 converted from p-type conduction to n-type conduction. Therefore, the user of the thermal history device 300 can look at the physical indicator and the timing recorder to determine when the nanowire 115 was exposed to the transition temperature associated with the volume dimension of the nanowire 115.

[0068] FIG. 7 is a flowchart illustrating one example of functionality implemented, by a user, thermal history device including at least one nanowire according to various embodiments of the present disclosure. It is understood that the flowchart of FIG. 7 provides merely an example of many different types of functional arrangements that can be employed to implement the operation of the portion of the securing device as described herein. As an alternative, the flowchart of FIG. 7 can be viewed as depicting an example of steps and methods implanted by the user according to one or more embodiments. For example, a user of some embodiments of the disclosed thermal history device can be a plastic water bottle transporter that is required to report the maximum temperature that the plastic water bottles have been exposed to.

[0069] The user of the thermal history device can begin in box 701, by determining a transition temperature of a volume dimension of a nanowire 115 (FIG. 1). For example, similar to the embodiment of the nanowire field effect transistor 100 described in FIG. 5, a nanowire 115 made of tin monoxide can have a width 203 of 100 nm, a length 206 of 5 μm, and a thickness 209 (FIG. 2) of 20 nm. Such a nanowire 115 can be associated with a transition temperature of 180° C. measuring the requisite temperature exposure for a phase transformation. Next, in box 704, the user may test the polarity of the nanowire 115 to determine whether the nanowire exhibits n-type conduction or p-type conduction, as depicted in box 707. If the user determines that the nanowire 115 is not exhibiting n-type conduction, as shown in box 710, then the user can recognize that the nanowire 115 is still exhibiting p-type conduction and has not undergone phase transformation. Thus, the user can determine that the nanowire has not been exposed to the transition temperature. Alternatively, if the user determines that the nanowire 115 is exhibiting n-type conduction, as shown in box 713, then the user can determine that the nanowire 115 has undergone phase transformation and thus has been exposed to the transition temperature. After which the process ends.

[0070] For example, suppose the user of the thermal history device is testing the polarity of a nanowire 115 described above, wherein the nanowire 115 is made of tin monoxide with a width 203 of 100 nm, a length 206 of 5 μm, and a thickness of 20 nm, and has a transition temperature of 180° C. The user of the thermal history device 300 can test the polarity of the nanowire 115 to determine whether it is exhibiting n-type conduction or p-type conduction. If the nanowire 115 is still a tin monoxide nanowire exhibiting p-type conduction, then the user can determine that the nanowire 115 has not been exposed to the transition temperature of 180° C. Alternatively, if the nanowire 115 is now a tin dioxide nanowire exhibiting n-type conduction, then the user can determine that the nanowire 115 has been exposed to the transition temperature 180° C. because of the phase transformation that occurred.

EXAMPLE

[0071] Now having described the embodiments of the disclosure, in general, the example describes some additional embodiments that may represent methods and systems relating to field-effect transistors used for thermal history detection. While embodiments of the present disclosure are described in connection with the example and the corresponding text and figures, there is no intent to limit embodiments of the disclosure to these descriptions. On the contrary,
the intent is to cover all alternatives, modifications, and equivalents included within the spirit and scope of embodiments of the present disclosure.

Example 1

[0072] Oxide semiconductors hold great promise as materials for use in many emerging electronic applications. Such applications include transparent and flexible displays, sensor arrays, flexible solar cells, and logic circuits for so-called invisible electronics. The use of oxide based thin-film transistors (TFT) has already been shown as a good solution to the increasingly demanding requirements of better display technologies. For example, transparent amorphous In—Ga—Zn—O with a mobility of 10 cm² V⁻¹ s⁻¹ has been demonstrated to be useful in switching/driving TFTs in the next generation of flat panel and flexible displays. Outstanding TFT results have been reported for display applications based on various oxide-based semiconducting films, although all such materials are based on n-type semiconductors. A p-type oxide with comparable performance (mobility, current-carrying capacity, optical transparency and mechanical flexibility) to that of previously developed n-type transparent semiconductor oxides not only will allow the realization of better display technologies but also will usher in a new era of transparent electronics.

[0073] The limiting factor for the full integration of oxide based devices, however, continues to be the development of a p-type oxide material with performance comparable to that of the n-type oxides. Cu-based oxides have been demonstrated to exhibit p-type behavior. The best performance (μp,~4.3 cm² V⁻¹ s⁻¹) has been exhibited when Cu₂O is deposited at 500°C. Despite their high hole mobility, Cu₂O-based oxides are of limited use because its optical transparency is hindered by their low optical bandgap of 2.2 eV. If plastic and other flexible substrates are the ultimate goal, low processing temperatures are essential. Recently, devices based on p-type tin monoxide (SnO) have been developed, but again their use is limited by either high deposition temperatures or low μp, similar to a-Si:H. Not even Hall-effect mobility (μH), in the range of n-type amorphous semiconductor oxides (10 cm² V⁻¹ s⁻¹) has been reported for SnO, preventing its use in practical applications.

Results and Discussion

Film Characterization.

[0074] The pathway to achieve high mobility involved a large number of experimental studies, each repeated several times, in which we carefully mapped out a very wide process window in our reactive DC magnetron sputtering process. It is known that Sn metal occurs in two possible oxidation states (±4), with SnO₂(±4) being the most thermodynamically stable phase. SnO is a metastable phase that easily oxidizes to n-type SnO₂. It is also known that depositing the correct p-type phase of SnO by physical vapor deposition is challenging due to the required fine control of oxygen pressure to prevent the formation of SnO₂ or any other intermediate phases such as Sn₂O₃ or SnO₃ with n-type characteristics. In our extensive experimental studies, we have found that the p-type transport in tin monoxide occurs only in a very narrow window of deposition conditions. This window occurs when the relative oxygen partial pressure (O₂/P) [where O₂/P = P/O₂/P(O₂+P₂O₅)] and deposition pressure (P) lie within the process boundaries illustrated by the bold black lines in FIG. 8A. Specifically, p-type tin monoxide transport occurs in the process regime where 7%–8%O₂/P15% and 1.5 mTorr ≤ P ≤ 2 mTorr. For the case where P > 2.0 mTorr or O₂/P > 15%, either amorphous phase or SnO₂ is formed. Pan and Fu have shown that in the presence of excess oxygen (and temperature), the metastable SnO phase transforms to SnO₂ via a process initiated by the local disproportionate redistribution of internal oxygen, known as the disproportionation mechanism. In the first step of the oxidation process, the metastable SnO phase coexists with intermediate products such as Sn₂O₃ and Sn, then the inward diffusion of external oxygen causes the full oxidation into the thermodynamically stable SnO₂ phase. In our films, the observation of an amorphous phase when P > 2.0 mTorr and 15% ≤ O₂/P ≤ 20% indicates that at these conditions the oxygen concentration is high enough not to form p-type SnO, but the thermal budget is not enough to crystallize the intermediate product (Sn₂O₃), or its diffusion intensity is too low to be detected by our tool. At higher O₂/P (>20%) oxygen content is enough to directly crystallize the films into SnO₂ phase after annealing. When O₂/P < 7% and/or P < 1.5 mTorr, metallic tin (β-Sn) is the dominant phase and the films exhibit either metallic or weak n-type conductivity. In this study, all the samples were deposited at room temperature following a postannealing treatment in air, in a tube furnace at 180°C. for 30 min.

[0075] The X-ray diffraction (XRD) patterns in FIG. 8B show the dependence of phase formation on the oxygen partial pressure (O₂/P) at a deposition pressure (P) of 1.8 mTorr, as an example. As indicated in FIG. 8A, films deposited at 13% ≤ O₂/P ≤ 11% show the presence of small traces of β-Sn in a matrix of SnO (this mixture is henceforth referred to as an SnO phase) SnO or SnO₃, while films deposited at 13% ≤ O₂/P ≤ 15% comprise pure tetragonal SnO. The Sn metal was uniformly distributed in the SnO matrix as seen in plane view transmission electron microscopy and as reflected by the excellent device uniformity, which will be discussed later. Films deposited at higher O₂/P form either amorphous SnO phase (a-SnO) or SnO₂ (e.g., 17% O₂/P) or SnO₂ (e.g., 20% O₂/P). Further, we found that the tin oxide phase formation (SnO, SnO, a-SnO, a-SnO₂, SnO₂) is extremely sensitive to the deposition pressure. FIG. 8C shows the influence of the deposition pressure on the SnO phase formation at 13% O₂/P. A pure polycrystalline SnO phase is obtained in the deposition pressure range of 1.7 mTorr to 2.0 mTorr. As the deposition pressure increases, the intensity of the SnO diffraction peaks increases up to P = 1.8 mTorr and then decreases at P > 1.9 mTorr to completely vanish at P > 2.0 mTorr, indicating the formation of amorphous films. The O₂/P is not only crucial to control which oxide phase will form, but also to control the amount of metallic tin present in the films. FIG. 8D shows XRD patterns in a narrower 20 range to clarify how the diffraction intensity of the Sn decreases as a function of O₂/P at 1.8 mTorr, which turned out to be the optimal deposition pressure for device performance as discussed below. X-ray photoelectron spectroscopy (XPS) analysis was used to estimate the metallic tin content in the SnO films. For the 1.8 mTorr deposition pressure, as the relative oxygen partial pressure (O₂/P) was reduced from 15% to 7%, the amount of metallic tin in the films increased from undetectable by XPS to nearly 5 atom%.

[0076] Noticeable differences in the intensities of the (101) and (110) diffraction peaks are observed with increasing O₂/P (FIG. 8D). The difference in intensities of the XRD peaks can have many origins, such as crystallite size, lattice defects, and
preferential crystallite orientation. We have identified preferential crystallite orientation (by pole density calculations) as well as lattice defects (by strain analysis) to be the main causes of the intensity differences.

[0077] FIG. 9A is a graph illustrating room temperature Hall mobility of the films deposited in the pressure range from 1.5 to 2.0 mTorr and 7% to 15% O<sub>2</sub>/Pr. The point at 7% O<sub>2</sub>/Pr, 1.5 mTorr showing n-type conduction as well as the 15% O<sub>2</sub>/Pr at 1.9 mTorr and 2.0 mTorr showing unreliable measurements, are set to zero. A maximum Hall mobility of 18.7 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> is obtained at 1.8 mTorr, 9% O<sub>2</sub>/Pr.

[0078] Room-temperature Hall effect measurements are summarized in the three-dimensional plot depicted in FIG. 9A. The plot summarizes the effect of the process parameters discussed above on the Hall mobility of the films. As shown in FIG. 8A, films deposited in the range of 7% O<sub>2</sub>/Pr=15% and a deposition pressure of 1.5 to 2.0 mTorr exhibit p-type behavior (a positive Hall effect coefficient). Films processed using conditions outside this window showed n-type or metallic behavior in accordance with the phase map in FIG. 8A. According to FIG. 9A, a maximum Hall mobility (μ<sub> Hall</sub>) of 18.7 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> is obtained for the films deposited at 1.8 mTorr and 9% O<sub>2</sub>/Pr, which surprisingly does not correspond to pure SnO films, but to mixed phase oxides (mp-SnO). The maximum μ<sub> Hall</sub>, obtained in this study is 8 times higher than the value reported for single-phase (001) epitaxial SnO and is of sufficiently large value that practical applications can be realized. The measured carrier density ranges from 4.83 x 10<sup>16</sup> cm<sup>-3</sup> to 3.33 x 10<sup>17</sup> cm<sup>-3</sup>, which is in the range of previously observed p-type SnO. Details of the Hall mobility, carrier density, and film conductivity are shown in Table 1 depicted in FIG. 9B.

Device Characterization.

[0079] The conceptual design of the fully transparent and flexible devices is depicted in FIGS. 10A and 10C, respectively, whereas FIGS. 10B and 10D show the actual fabricated devices. FIGS. 11A and 11C depict the output characteristics of fully transparent and flexible devices produced at 9% O<sub>2</sub>/Pr P=1.8 mTorr, respectively, in which clear linear and saturation regions can be observed. The absence of current crowding at low source-to-drain voltages (V<sub>DS</sub>) indicates an Ohmic contact of Ti/TiO<sub>x</sub> with SnO. FIGS. 11B and 11D present the transfer characteristics measured with V<sub>DS</sub>=−1 V for devices produced at 1.8 mTorr with different O<sub>2</sub>/Pr. In all cases, p-type behavior is observed, since the holes are generated at negative gate voltages (V<sub>GS</sub>). FIGS. 11B and 11D also show that the gate leakage currents are very low and are around 10<sup>−12</sup> amps.

[0080] FIG. 12A is a graph illustrating the linear field-effect mobility (μ<sub>FE</sub>) as a function of O<sub>2</sub>/Pr for the devices fabricated for this study at P=1.8 mTorr. FIG. 12B is a graph illustrating the threshold voltage (V<sub>T</sub>) comparison of the fully transparent and flexible devices. FIG. 12C is a graph illustrating the linear field-effect mobility as a function of width-to-length ratio for the transparent samples. FIG. 12D is a graph illustrating multiple, dual-sweep transfer curves for a device with a W/L=10 at the best performance condition (9% O<sub>2</sub>/Pr, 1.8 mTorr). FIGS. 12E and 12F show atomic force microscopy (AFM) surface profiles for the mp-SnO films deposited on glass and polyimide substrates, respectively.

[0081] Linear-region field-effect mobility (μ<sub>FE</sub>) and threshold voltage (V<sub>T</sub>) were calculated from the transfer characteristics and the obtained values are shown in FIGS. 12A and 12B, respectively. To rule out any artifacts in the TFT measurements, all the devices were characterized following the procedure recommended by J.F. Wager with multiple W/L ratios. The mobility data shown in FIG. 12A were extracted from devices with W/L=1, but W/L ratios from 1 to 10 were tested and gave very similar results as shown in FIG. 12C for the set of fully transparent devices. Multiple, dual sweep I<sub>DS</sub> vs V<sub>GS</sub> scans were performed, and it was found that the devices belong to type II in Wager’s classification which is nonequilibrium, steady-state behavior. An effective hysteresis density of NIHYS=1.8645x10<sup>5</sup> cm<sup>-2</sup> with a threshold voltage shift of 3.67 V at a V<sub>DS</sub> scan rate SR=366 mV/s is observed for the best performance device (9% O<sub>2</sub>/Pr, 1.8 mTorr) as shown in FIG. 12D with a W/L ratio of 10. The transparent TFTs on glass have a maximum μ<sub>FE</sub> of 6.75 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> while the mobility is nearly 20% lower for the TFTs made on flexible substrates. Results of SnO surface inspection by atomic force microscopy using the same area as in actual devices (50 μm x 50 μm) are presented in FIGS. 12E and 12F for glass and plastic substrates, respectively. It is evident that the mixed phase (mp-SnO) films deposited on flexible substrates have a higher surface roughness. The lower mobility of devices on flexible polyimide substrate can thus be attributed to the higher surface roughness of this substrate, which increases carrier scattering and hence reduces the mobility. For all O<sub>2</sub>/Pr conditions, the I<sub>ON</sub>/I<sub>OFF</sub> ratio is around 10<sup>4</sup>, leading to a maximum of 6×10<sup>5</sup> for the device with highest mobility.

[0082] As expected, devices produced at different O<sub>2</sub>/Pr exhibit different behaviors. μ<sub>FE</sub> follows a similar trend to that of μ<sub>eff</sub> shown in FIG. 9A. The hole mobility reaches its maximum in case of devices (and films) deposited at 9% O<sub>2</sub>/Pr, 1.8 mTorr, which corresponds to the mp-SnO films with ~3 atom% Sn.

[0083] FIG. 13A is a graph illustrating a comparison of reported field-effect mobility versus maximum processing temperature (either deposition or post annealing) for leading p-type oxides. The reference is indicated in square brackets. Mobility of a-IGZO (n-type) and a-Si:H are not plotted as a function of the temperature and are used just for comparison. FIG. 13B is a graph illustrating a transmission spectrum of the components of the TFT. FIG. 13C is a graph representing a typical plot of the optical band gap extraction (indicated by the dotted line) of the films deposited at 1.8 mTorr.

[0084] The transmittance spectra of the gate electrode and the gate dielectric, the mp-SnO layer, and the final stack are shown in FIG. 13B. The average optical transmission of the 15 mm mp-SnO layer in the visible region (400-700 nm) is 92%, while it is 63% for the entire device, mainly limited by the Ti layer. The use of the Ti source and drain contact interlayer results from the observation of enhanced device performance over some other contacts like Au, Ni, Pt, and ITO. The optical bandgap, E<sub>g</sub>, has been estimated from the absorption coefficient, a, calculated as a function of the incident photon energy. E<sub>g</sub> was obtained by extrapolating the linear portion in the (αhv)<sup>2</sup> vs hv plot, as shown in FIG. 13C by the dotted lines. The estimated E<sub>g</sub> ranges from 2.65 eV for 7% O<sub>2</sub>/Pr to 2.92 eV for 15% O<sub>2</sub>/Pr, matching well with that of pure SnO.

Conclusions

[0085] We have demonstrated the highest hole mobility reported to date for a p-type oxide processed at low temperature by careful process control. A detailed phase map for nanoscale physical vapor deposition of tin monoxide has been
developed for the first time. We have shown that control of the phase formation of thin oxide films greatly enhances the carrier mobility yielding $\mu_{\text{flat}} = 18.7 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$. Residual second phases must be carefully optimized to obtain maximum hole mobility. Furthermore, we have demonstrated record device performance for a transparent p-type oxide semiconductor on both rigid and flexible substrates, with a linear-region field-effect mobility of 6.75 cm$^2$ V$^{-1}$ s$^{-1}$ and 5.87 cm$^2$ V$^{-1}$ s$^{-1}$, respectively, a threshold voltage of $-1 \text{V}$ and an $I_{ON}/I_{OFF}$ ratio of $6 \times 10^3$.

**Experiment**

**Film Fabrication and Characterization.**

[0086] Pure SnO and mixed phase (mp-SnO) films were deposited onto soda-lime glass substrates by direct current (DC) reactive magnetron sputtering using a 2 in. (5.08 cm) tin metal target from Angstrom Science, Canada, with a purity of 99.99%. The reactive sputtering was performed at room temperature in a mixture of argon and oxygen gases, in an AMOD-model thin film deposition tool designed by Angstrom Engineering. To determine optimal deposition conditions, the oxygen partial pressure was varied from 3% to 50%. The deposition pressure was scanned from 1 to 4 mTorr while the DC power was held at 30 W (9.55 W/in$^2$ power density). The distance between the target and the substrate was 20 cm, while the gun was located at 160° with respect to the horizon, achieving a deposition rate of 0.8 Å/s. Post-annealing in air was performed in a tube furnace at 180° C. for 30 min.

**TFT Fabrication and Characterization.**

[0087] The bottom gate indium tin oxide (ITO) layers were deposited by radio frequency magnetron sputtering at room temperature. The ITO$_2$ (220 nm) gate dielectric was deposited on top of 150 nm ITO-coated glass/polyimide substrates by atomic layer deposition. The active layer consisted of 15 nm of SnO deposited at different oxygen partial pressures. The stack was completed with 8 nm electron-beam evaporated Ti and 90 nm sputtered ITO source and drain contacts followed by thermal treatment at 180° C. in air, for 30 min, to crystallize both the SnO and ITO layers. The devices were patterned by photolithography and lift-off technique and measured on a probe station in air using a Keithley 4200-SCS semiconductor parameter analyzer at room temperature in the dark. The performance of the TFTs was evaluated on devices with a width-to-length ratio (W/L) of 1 having W and L of 50 µm, respectively. Linear-region field-effect mobility ($\mu_{FE}$), threshold voltage ($V_T$) and subthreshold swing (S) were evaluated with the conventional metal-oxide-semiconductor field effect transistor model described in eqs 1 and 2:

$$S = \frac{dV_S}{d(\log I_D)} = \frac{kT}{q} \ln \left( 1 + \frac{qC_S}{C_m} \right)$$

(1)

$$\Q \mu_{FE} = \frac{W}{L} \left( \frac{V_G - V_T}{V_G - V_F} \right) \left( \frac{V_F}{2} \right) \text{ for } V_G < V_F - V_T \text{ and } V_G > V_F + V_T$$

(2)

$C_m$ is the capacitance per unit area of the gate insulator and measured to be 60 nFcm$^{-2}$ with no more than 3% variation in the frequency range from 1 kHz to 1 MHz and an extracted dielectric constant of $\epsilon=14$.

**REFERENCES FOR EXAMPLE 1**


[0122] It should be noted that ratios, concentrations, amounts, and other numerical data may be expressed herein in a range format. It is to be understood that such a range format is used for convenience and brevity, and thus, should be interpreted in a flexible manner to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. To illustrate, a concentration range of “about 0.1% to about 5%” should be interpreted to include not only the explicitly recited concentration of about 0.1 wt % to about 5 wt %, but also include individual concentrations (e.g., 1%, 2%, 3%, and 4%) and the sub-ranges (e.g., 0.5%, 1.1%, 2.2%, 3.3%, and 4.4%) within the indicated range. In an embodiment, the term “about” can include traditional rounding according to figures and the measurement techniques. In addition, the phrase “about ‘x’ to ‘y’” includes “about ‘x’ or about ‘y’”. When a range includes “zero” and is modified by “about” (e.g., about one to zero or about zero to one), about zero can include, 0, 0.1, 0.01, or 0.001.

[0123] While only a few embodiments of the present disclosure have been shown and described herein, it will become apparent to those skilled in the art that various modifications and changes can be made in the present disclosure without departing from the spirit and scope of the present disclosure. All such modification and changes coming within the scope of the appended claims are intended to be carried out thereby.

Therefore, the following is claimed:

1. A system for temperature history detection comprising:
   a gate electrode made of a material with conductive properties;
   a plurality of gate dielectrics positioned in proximity to the gate electrode, wherein the gate dielectrics are insulators; and
   a plurality of nanowires, wherein an individual one of the nanowires is at least partially connected to a source electrode at one end and a drain electrode at another end, wherein the individual one of the nanowires has different volume dimensions than another individual one of the nanowires, and the individual one of the nanowires is configured to convert from p-type conduction to n-type conduction at a transition temperature.
2. The system of claim 1, wherein the individual one of the nanowires is a tin monoxide nanowire.

3. The system of claim 2, wherein the individual one of the nanowires has a same volume dimension than the other individual one of the nanowires.

4. The system of claim 1, wherein the volume dimensions comprise a width, a length, and a thickness.

5. The system of claim 4, wherein the width is about 10 nanometers and 500 nanometers.

6. The system of claim 4, wherein the length is about 1 micrometer to and micrometers.

7. The system of claim 4, wherein the thickness is about 5 nanometers and 50 nanometers.

8. A method for thermal history detection comprising: determining a transition temperature that measures a temperature when a nanowire transitions from a p-type conduction to a n-type conduction, wherein the transition temperature is associated with a volume of the nanowire; testing a polarity of a field effect transistor comprising the volume of the nanowire; and determining whether the nanowire has been exposed to the transition temperature.

9. The method of claim 8, wherein the transition temperature is about 100° C. and 200° C.

10. The method of claim 8, wherein the nanowire is a tin monoxide nanowire.

11. The method of claim 10, wherein the nanowire converts from the tin monoxide to tin dioxide.

12. The method of claim 8, wherein the volume comprises a width, a length, and a thickness, wherein the width is about 10 nanometers and 500 nanometers, wherein the length is about 1 micrometer to and micrometers, and wherein the thickness is about 5 nanometers and 50 nanometers.

13. A matrix of field effect transistors, each field effect transistor comprising:
   a substrate;
   a gate electrode positioned in proximity to the substrate;
   a gate dielectric displaced in proximity to a source electrode and a drain electrode;
   a first nanowire with a first volume dimension, wherein one end of the first nanowire is coupled to the source electrode and another end of the first nanowire is coupled to the drain electrode; and
   a second nanowire with a second volume dimension, wherein one end of the second nanowire is coupled to the source electrode and another end of the second nanowire is coupled to the drain electrode, wherein the first volume dimension is different from the second volume dimension, wherein the first volume dimension and the second volume dimension are associated with a transition temperature that measures a temperature when the nanowire transitions from p-type conduction to n-type conduction.

14. The matrix of field effect transistors of claim 13, wherein the first volume dimension comprises a width of about 10 nanometers to 500 nanometers.

15. The matrix of field effect transistors of claim 13, wherein the first volume dimension comprises a length of about 1 micrometer to 10 micrometers.

16. The matrix of field effect transistors of claim 13, wherein the first volume dimension comprises a thickness of about 5 nanometers to 50 nanometers.

17. The matrix of field effect transistors of 13, wherein the first and second nanowires each comprise a thin film of tin monoxide at least partially in contact with the source electrode at one end and the drain electrode at the other end, the thin film of tin monoxide operating as a semiconducting channel between the source electrode and the drain electrode.

18. The matrix of field effect transistors of claim 17, wherein the tin monoxide converts to tin dioxide at the transition temperature.

19. The matrix of field effect transistors of claim 13, wherein a maximum exposure temperature is determined based on the transition temperature.

20. The matrix of field effect transistors of claim 13, wherein the gate electrode is made of a material with conductive properties.

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