Zinc Oxide Integrated Wavy Channel Thin Film Transistor Based High Performance Digital Circuits

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***Abstract*— High performance thin film transistor (TFT) can be a great driving force for display, sensor/actuator, integrated electronics, and distributed computation for Internet of Everything applications. While semiconducting oxides like zinc oxide (ZnO) present promising opportunity in that regard, still wide area of improvement exists to increase the performance further. Here, we show a wavy channel (WC) architecture for ZnO integrated TFT which increases transistor width without chip area penalty, enabling high performance in material agnostic way. We further demonstrate digital logic NAND circuit using the WC architecture and compare it to the conventional planar architecture. The WC architecture circuits have shown 2× higher peak-to-peak output voltage for the same input voltage. They also have 3× lower high-to-low propagation delay times, respectively, when compared to the planar architecture. The performance enhancement is attributed to both extra device width and enhanced field effect mobility due to higher gate field electrostatics control.**

***Index Terms*:— Wavy channel, Zin Oxide, Thin Film Transistor, Digital Circuits, NAND.**

I. Introduction

For more than a decade, amorphous metal oxide semiconductors (AOS) have been explored as promising candidates for flexible, transparent, and large-area displays and electronics [1, 2]. N-type oxides are particularly of interest due to their higher field-effect mobility (10 $cm^2/V.s$) compared to p-type oxides [2, 3]. Amorphous Indium Gallium Zinc Oxide (In-Ga-Zn-O) mobility was optimized to ~20 $cm^2/V.s$ for Indium (In) rich films [4]. For display applications, field effect mobility in excess of 20 $cm^2/V.s$ had been previously set as a benchmark for future Active Matrix Oxide Light Emitting Diode (AMOLED) displays [5]. An even higher mobility benchmark of 80 $cm^2/V.s$ mobility is set to be on par with low temperature poly silicon (LTPS) technology [6]. Recent material development for n-type oxides has led to field effect mobility in excess of 100 $cm^2/V.s$ for Zinc Oxynitride (ZnON) films [7], which was even higher than $InGaO_3(ZnO)_5$ single crystalline films [8]. However, for beyond display large-area macro-electronics applications such as: digital logic applications for distributed computing and sensors/actuators integrated electronics for Internet of Everything applications, optimization of TFT switching speed becomes an important benchmark. Field effect transistor transit frequency, f_T, is typically used to quantify the speed of the devices. Expression for transit frequency is given by [9]:

$$f_T = \frac{g_m}{2 \times \pi \times C_{ox}} \sim \frac{\mu \times (V_{GS} - V_T)}{2 \times \pi \times L_{ch}^2} \qquad (1)$$

Where, g_m is the transconductance, C_{ox} is the oxide gate capacitance, μ is the carrier mobility, L_{ch} is the channel length, and (V_{GS}–V_T) is the gate overdrive voltage of the TFT, where V_T is the threshold voltage. Although material related properties such as channel mobility, μ, and oxide dielectric capacitance, C_{ox}, are still relevant for optimization of f_T, other parameters in equation (1) are still critical. For a given semiconductor/dielectric gate stack, besides V_T engineering, gate length (L_g) scaling has traditionally been the major approach for improving f_T. There are two main approaches for L_g scaling: (i) top down lithographic scaling shown for amorphous In-Ga-Zn-O (IGZO) TFT down to L_g of 0.18 µm. This approach; however, is both expensive and suffers from sensitivity of TFT properties such as saturation mobility to processing variations in the gate-to-contact spacing, and the shape of the active area [10]; and (ii) non-lithographically defined gate length using vertical channel TFT architecture [11]. Although, it is less expensive compared to the first approach, the TFT properties suffer immensely from both gate leakage and gate-to-source/drain overlap capacitance. Finally, L_g scaling is known to induce negative V_T shift which in return increases the OFF current, I_{OFF}, value and degrades the device static power consumption [12]. Therefore, we showed a novel approach, which improves I_{ON} per unit chip area by increasing the device width vertically without extra chip area penalty, as well as, enhances the field effect mobility, μ_{FE}, and thus g_m per unit device width due to better electrostatics, as reported in our previous works [13-17]. This allows boosting performance of the smallest reliable L_g without changing V_T or I_{OFF}.

II. TFT and Circuit Characterization

The idea behind the device is to introduce corrugations to the substrate using anisotropic etching to increase the device width without extra chip area penalty. Details of device fabrication can be found in our previous work [17]. Fig. 1(a) shows an optical image of L_g = 10 µm device. Fig. 1(b) shows a side view

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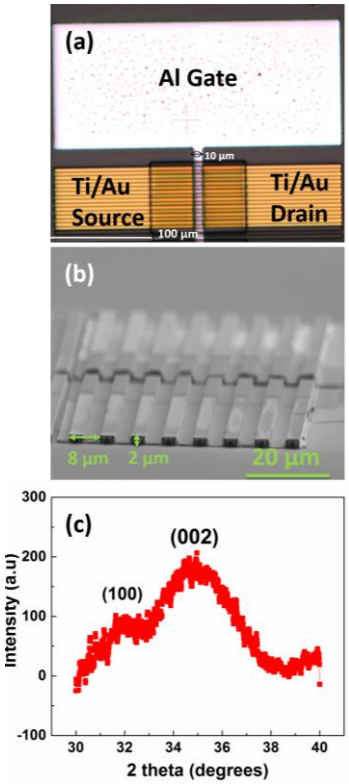

Fig. 1 (a) Digital image showing L_g =10 µm device, and (b) Titled view SEM image of the device in (a) showing 4 µm wide fin, where the fin height is 2 µm, and the fin pitch is 8 µm pitch(4 µm 1-1 device). (c) Grazing incidence XRD of the ZnO film showing weak Wurtzite peaks.

SEM image of WC TFT which we refer to as 4 µm 1-1 device, showing 4 µm wide fin-like feature, with 2 µm fin height and 8 µm fin pitch. The device has 50% larger width when compared to a planar device consuming the same chip area. Fig. 1(c) shows Grazing Incidence X-ray Diffraction (GIXRD) pattern of the ZnO film, showing a weak (100) and a dominant (002) Wurtzite peaks, which have been reported in the literature for ALD films deposited at similar conditions [18, 19]. The film crystallinity was further checked with SEM images, which showed rice-like grains with sizes < 20 nm, confirming the film is polycrystalline.

Figs. 2(a, b) show the transfer and output characteristics of L_g = 10 µm device, the WC and planar devices have V_T values of 2.7 and 2V, respectively. Output characteristics show that the WC TFT has 2× the output current of the planar TFT consuming the same chip area, where the WC and planar TFTs have I_{DS} of 1.8 mA and 0.9 mA, respectively, at V_{GS} = 10V. No increase in the I_{OFF} value can be seen in Fig. 2(a), which is desirable for reducing the static power consumption. The increase in the drive current is not only proportional to the 50% extra device width, rather it had boost up from other sources due to the device architecture. Hence, analyzing the saturation mobility of both devices, μ_{sat}, it was found that WC devices had a peak value of 7.1 cm^2/V.s while planar devices had a peak value of 4.8 cm^2/V.s, as shown in Fig. 2(c). This amounts to ~50% higher mobility for WC TFTs, when compared to the planar counterparts. The calculation was done taken into account the 50% extra device width, W_{extra}, of the WC TFT according to the saturation mobility expression [20]:

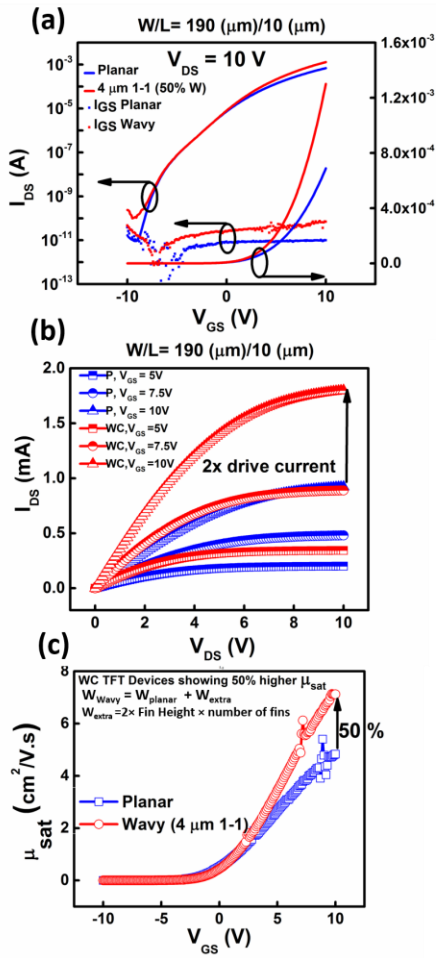

Fig. 2 (a) Transfer, and (b) output characteristics of L_g=10 µm devices. (c) WC devices showing 50% higher saturation mobility, μ_{sat}.

$$\mu_{sat} = \left(\frac{2L_g}{W}\right)\left(\frac{1}{C_{ox}}\right)\left(\frac{d\sqrt{I_{DS}}}{dV_{GS}}\right) \qquad (2)$$

Where W is the device width. This means that WC device has 50% higher transconductance per unit device width, which cannot be accounted for by W_{extra}. Therefore, in order to explain the enhancement in field effect mobility, the device geometry and electrostatics need to be analyzed. When analyzing the fin cross-section, we found that the device has a zigzag like sidewall gate stack, as shown in Figs. 3(a, b). This is due to the etch profile of the anisotropic reactive ion etching that depends on two steps of: i) side wall passivation and ii) subsequent etching, which gives rise to the sidewall scallops. Hence, to evaluate the effect on charge accumulation in the channel due to the gate metal zigzag profile, a COMSOL™ simulation of the device electrostatics was performed to scale of the SEM image in Figs. 3(b). The ZnO material parameters were taken from the literature for polycrystalline ZnO films [21]. Simulation has shown a 2.3× higher electric field in the around the sharp corner of the zigzag gate as shown in Fig. 3(c), which, as a result, led to 15% higher carrier concentration as shown in Fig. 3(d) compared to a planar gate, when biased at V_{GS} = 10V. Fig. 2(c) shows that μ_{sat} is higher for WC TFT when V_{GS}>5V, which shows gate-field dependent mobility enhancement.

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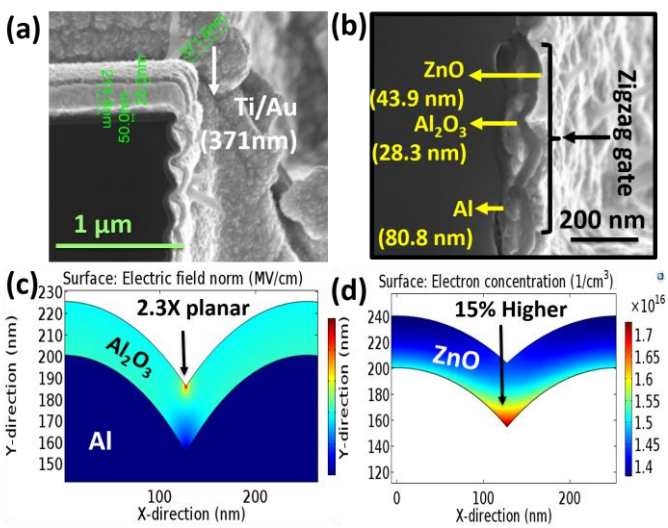

Fig. 3 (a) Sidewall cross-section showing thickness of various device parameters, and (b) Zoomed in image of the gate stack. COMSOL simulation of (c) Surface Electric Field norm in Al_2O_3 gate dielectric and (d) electron concentration in the ZnO channel, both to scale with (b) biased at V_{GS}= 10V.

Modelling study has shown that in a polycrystalline ZnO TFT, nanoscale grains induce a strong overlap of the double Schottkey barriers with a higher activation energy in the crystallite and a lower barrier potential in the grain boundary [21]. Here the grain boundary Schottky Barrier Height (SBH) is modulated by the gate field [21], which was confirmed experimentally as well [22]. Hence the 2.3× higher field in the channel could qualitatively explain why WC devices have a higher field effect mobility, compared to planar devices. The simulation results also have relevance for AOS based TFTs because of gate field dependent effective mobility. Here percolation transport mechanism dominates transport at high gate fields, in which the field effect mobility, μ_{FE}, is controlled by percolation through non-localized states through the path of least resistance among the potential barriers whose height is controlled by the gate field [23]. Thus, we believe the WC architecture could enhance μ_{FE} for AOS based TFTs.

We wanted to measure the effect of the new architecture on leveraging higher performance for the same channel material, when compared to the conventional planar architecture. This is the case since the increase in the current is not just proportional to the increase in device width. Hence, the WC devices should manifest faster switching since they have larger transconductance, g_m, per device width. Thus, to compare the circuit performance of the new architecture, we have chosen NAND circuit for the comparison between the two architectures using NMOS logic design.

Fig. 4(a) shows NAND circuit design using transistor with L_g = 10 µm, drive transistor widths of 600 µm and pull-up transistor width of 30 µm. The two devices in comparison occupy the same chip area. The two gates are driven by the same input square wave of 10 V peak-to-peak voltage, i.e. $V_{input\ Low}$ = 0V and $V_{input\ High}$ = 10V, one NAND input is driven with a frequency f = 200 Hz, and the other with 100 Hz. Figs. 4(b,c) show the output of the WC and planar NAND circuit, where WC NAND circuit has shown more than 2× increase in

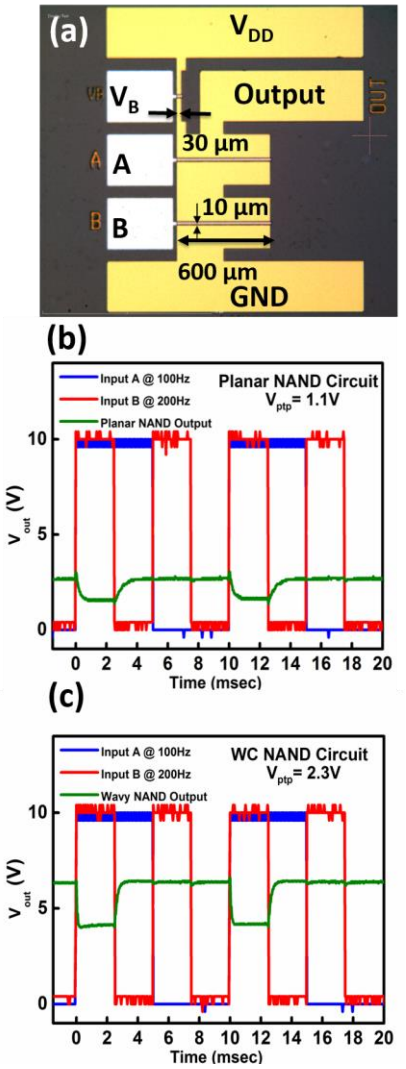

Fig. 4 (a) Digital image of L_g= 10 µm NAND circuit, showing device dimensions. (b-c) Comparison showing 100% higher $V_{out\ ptp}$ for WC NAND and 3× lower high-to-low propagation delay t_{PHL}.

the output peak-to-peak voltage, $V_{out\ ptp}$, when compared to the planar circuit. It could also be noticed that the high-to-low propagation delay time, t_{PHL}, was shorter for WC NAND circuit when compared to the planar counterpart. The propagation delay time is defined as the maximum time from the input crossing 50% to the output crossing 50% [24]. The t_{PHL} of the fabricated circuits were 120, and 40 µs for planar and WC NAND circuits, respectively, thus showing 3× lower t_{PHL} for WC NAND.

III. Conclusion

We have presented wavy architecture based ZnO integrated TFT based digital logic circuit components. NAND WC circuits has shown 2× $V_{out\ ptp}$ and 3× faster high-to-low propagation delay when compared to conventional planar circuits, thus enabling high performance digital logic circuits even for low mobility channel materials.

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