Out-of-plane Strain Effect on Silicon-Based Flexible FinFETs

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We report out-of-plane strain effect on silicon based flexible FinFET, with sub 20 nm wide fins and hafnium silicate based high-κ gate dielectric. Since ultra-thin inorganic solid state substrates become flexible with reduced thickness, flexing induced strain does not enhance performance. However, detrimental effects arise as the devices are subject to various out-of-plane stresses (compressive and tensile) along the channel length.

With the emergence of Internet of Things (IoT) we expect to see flexible versions of state-of-the-art electronics deployed on curvilinear surfaces in wearable format. To overcome performance, integration density limitation, we have devised a CMOS compatible low-cost process to transform any traditional electronics into flexible ones while retaining its performance, and integration density. We use our soft-back etch process to thin down the silicon-on-insulator (SOI) based FinFET devices into an ultra-thin flexible platform (48 μm thick) **(Fig. 1)**. We perform the process from the backside using deep reactive ion etching (DRIE) in patterned substrate, utilizing the inverse proportionality between flexural modulus ($E_{flexural}$) and substrate thickness (t) ($E_{flexural} \alpha 1/t^3$) to transform the rigid bulk high performance FinFETs into a flexible form. We used a Keithley 4200-SCS parameter analyzer, on a manual Semi-probe probe station, and custom designed curved aluminum surfaces for characterization.

Fig. 2 shows the experimental setup with bending directions' illustrations. Bending was done along the fins (parallel to the line connecting source and drain). **Fig. 3** shows the finite element analysis results for compressive versus tensile stressed surfaces, predicting that compressive stress might be the more expressed condition in terms of altering device behavior (nearly doubling of the applied stress at the surface containing the devices). **Figs. 4 and 5** show transfer/output characteristics for NMOS and PMOS devices bent along the channel length, respectively, for unstressed, tensile and compressively stressed FinFETs (up to 0.1% nominal strain). Evidently, there is a clear trend of increased leakage (off current) and reduced drive (on current), with the exception of PMOS under stress applied along the channel length that showed no obvious degradation for "on" current. Performance metrics analysis suggests incongruent influence of globally applied out-of-plane-stress with well-studied enhancement effects due to localized strain, using compressive SiGe source/drain or tensile Si_3N_4 spacer. Effective mobility is extracted at V_{ds} = 50 mV to ensure uniformity of channel charges. **Figs. 6 and 7** show the change in effective mobility and gate leakage *vs.* overdrive voltage ($V_{gs} - V_{t,linear}$) for NMOS FinFETs and PMOS FinFETs, respectively. PMOS FinFETs under compressive stress along the channel had only the peak mobilities affected while NMOS devices stressed along the channel have lower mobilities under both tensile and compressive stress (explained by the $>10^4$ higher leakage currents in **Fig. 6b**). **Fig. 7b** shows that gate leakage for PMOS stressed along the channel did not degrade with flexing. The results show that empirically, there are shifts in threshold voltages, degradation in subthreshold slopes, and increases in "off" currents through the channel as well as through the gate dielectric when the devices are under out-of-plane stresses; but still the functionality is not affected. Furthermore, PMOS is less sensitive and more suitable for flexible applications than NMOS which showed greater overall deviations.

We have discussed the effect of out-of-plane stress on flexible silicon based FinFETs on silicon that attained flexibility. The analysis shows that global out of plane stress does not affect the devices in the same way the well-studied biaxial/uniaxial local stress does. Moreover, the orientation of the devices relative to the bending axis is critical. This study is a step forward in devising suitable consumer electronics applications that demand flexibility in form factor of the electronics as well as high performance in its functionality and highlights the effects of carriers type (n-type/ p-type) with stress type (compressive/ tensile).

References

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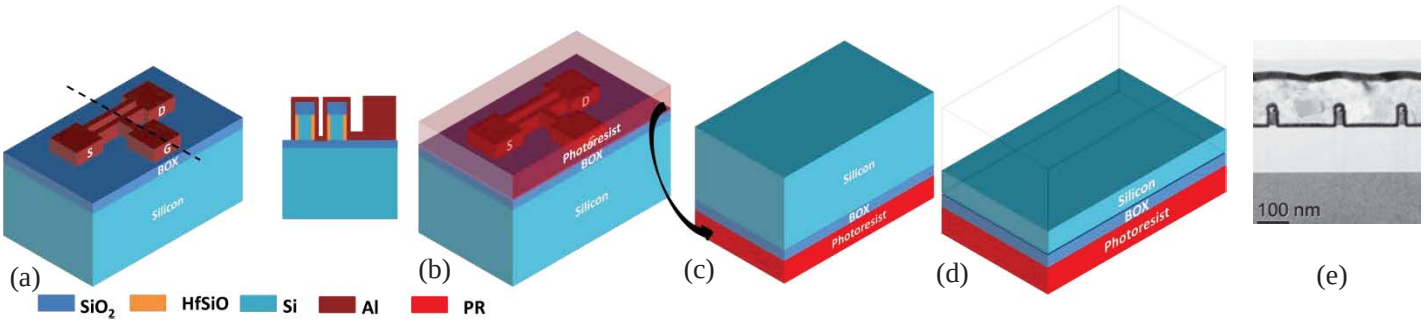

Fig. 1. Fabrication process flow, a) fabricated FinFET devices on standard 90 nm SOI with 145 nm BOX, b) PR coating for chip-protection during back etch process, c) die flipped upside down, (d) FinFET die etched back using soft-back etch DRIE technique and (e) a cross-section TEM of the fin array.

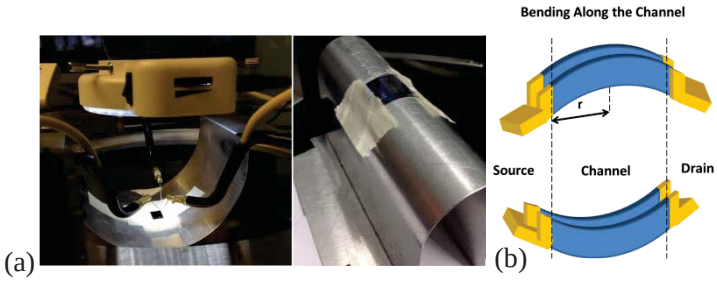

Fig. 2. (a) Experimental setup, and (b) illustration of bending along the channel

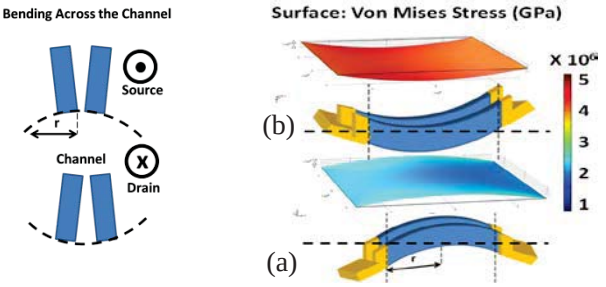

Fig. 3. FEM analysis of (a) tensile *vs.* (b) compressive stress.

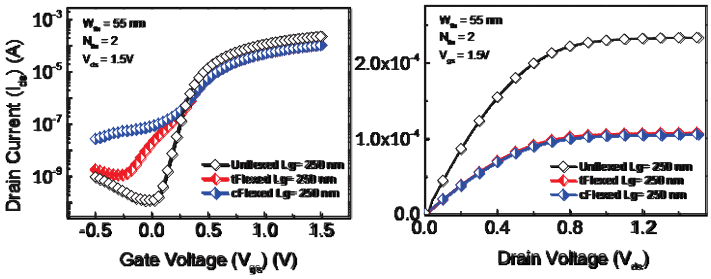

Fig. 4. Transfer and output characteristics of short channel NMOS (250 nm), under unstrained, tensile strained, and compressive strained conditions. Strain conditions are out-of-plane and along the channel length.

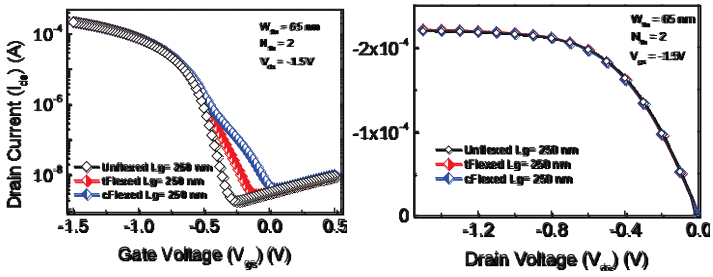

Fig. 5. Transfer and output characteristics of short channel PMOS (250 nm), under unstrained, tensile strained, and compressive strained conditions. Strain conditions are out-of-plane and along the channel length.

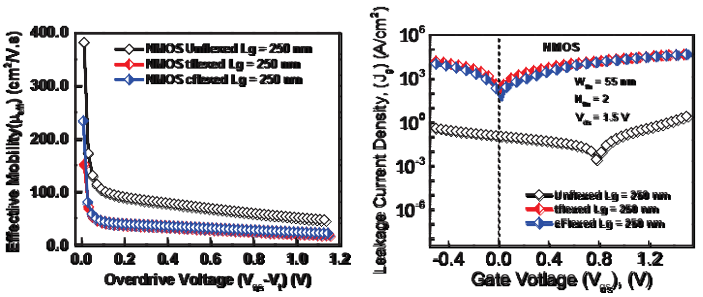

Fig. 6. (a) Mobility plot for along the channel strained N-type FinFETs and (b) Gate leakage of N-Type FinFETs subjected to along the channel strain conditions.

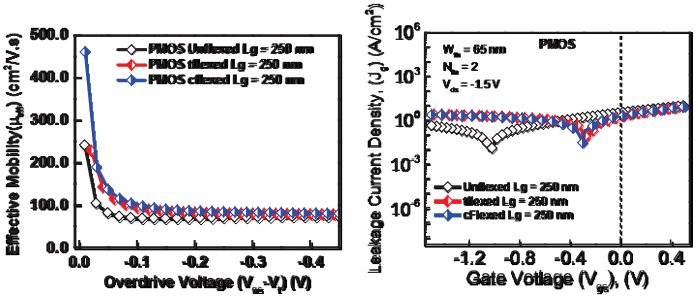

Fig. 7. (a) Mobility plot for along the channel strained P-type FinFETs, and (b) Gate leakage of P-Type FinFETs subjected to along the channel strain conditions.