Gain Enhancement of Low Profile On-chip Dipole Antenna Via Artificial Magnetic Conductor At 94 GHz

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***Abstract*—The bottleneck for realizing high efficiency System-on-Chip is integrating the antenna on the lossy silicon substrate. To shield the antenna from the silicon, a ground plane can be used. However, the ultra-thin oxide does not provide enough separation between the antenna and the ground plane. In this work, we demonstrate one of the highest reported gains to date for low profile 94 GHz on-chip dipole antenna while the ground plane is in the lowest metal in the oxide (M1). This is achieved by optimizing an Artificial Magnetic Conductor (AMC) structure midway the antenna and M1. The dipole antenna without the AMC has a gain of – 11 dBi while with the AMC structure a gain of + 4.8 dBi and hence achieving a gain enhancement of + 15.8 dB.**

***Index Terms*—mm-wave, on-chip antenna, SoC, artifical magnetic conductor (AMC) and High-Impedance-Surface (HiS).**

I. Introduction

Integrated millimeter-wave antennas on CMOS silicon substrate have been an active research area for the last decade. The System-on-Chip (SoC) is an attractive approach to reduce the overall size and cost. However, integrated on chip antennas face several challenges that arise from the fact that silicon is not suited as the antenna substrate. The silicon substrate has a low resistivity (typically 10-20 Ωcm) and relatively high silicon dielectric constant ($\varepsilon_r \approx 11.7$) causing most of the RF power to be absorbed in the substrate rather than radiating into free space and consequently lowering the overall system efficiency [1-3].

Many attempts have been conducted in literature to increase the efficiency of on chip antennas and hence compensate for the shortcomings of the silicon substrate. In [3], a hemispherical lens is abutted to the silicon substrate to convert the surface wave power into useful radiation. The previous approach suffers from the need of additional post processing that reduces the mass manufacturing and hence increases the overall cost.

To avoid additional post processing, silicon substrate can be shielded by the use of one of the metal layers (usually the first bottom layer) that acts as a ground plane for the antenna. Although this approach provides solid shielding from the silicon, the antenna being in close proximity to the ground plane generates image currents in opposite direction that cancel out its radiation. To counteract the image current problems, recently the concept of Artificial Magnetic Conductor (AMC) has been used to replace the perfect electric conductor and enhance the antenna performance [4].

In this work, a 94 GHz on chip dipole antenna has been designed with the aim of increasing its radiation efficiency. This is done through incorporating an AMC beneath the antenna. Despite the fact that it becomes challenging to design an AMC with extremely thin substrate due to excessive heat losses [5], the ground plane of the AMC structure has been chosen to be within the silicon dioxide to completely isolate the silicon losses. Gain enhancement of about 15.8 dB is achieved compared to a dipole without AMC. This is one of the best reported results, to our best knowledge, to date for a 94 GHz on chip antenna with the ground plane being at M1.

II. On-Chip Antenna

The stack up used is shown in Fig.1. The antenna is shield from the silicon substrate by a 2 um thick copper ground plane (M1). The overall separation between the ground plane and the antenna at the top metal is 40 um ($\lambda_0/100$), where λ_0 is the wavelength in free space. Finally, the AMC structure is placed midway the antenna and the ground plane. All simulations are carried out with CST Microwave Studio.

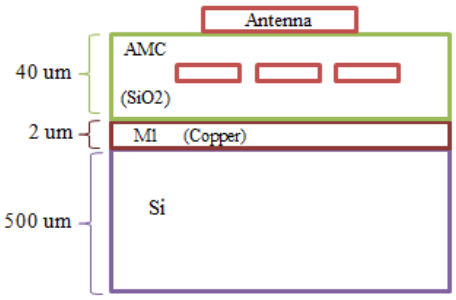

Fig.1. Lateral view of the considered CMOS compatible stack up.

A. Dipole on Thin Grounded Oxide

A λ/2 dipole is simulated at a distance of 40 um away from the ground plane. The ground plane shields the antenna from the lossy silicon. To reduce the simulation time, the stack up is simulated without the silicon beneath M1. The

simulation results show that placing the ground plane at M1 has a profound effect on the antenna gain. The antenna shows a gain of -11 dBi. The considerably low value for the gain originates from (1) the current images generated due to the ground plane are in close proximity to the original currents and hence canceling out their radiation and (2) the fact that the close by ground plane lowers the input impedance of the antenna to Z_{input}= 1.3 Ω which not only introduces huge mismatch but also makes it difficult to match it with conventional methods.

B. Dipole on Thin Oxide with AMC

To circumvent the aforementioned drawbacks of the ultra-thin oxide, a patterned periodic surface, often called Frequency Selective Surface (FSS) or Partial Reflective Surface (PRS), is inserted midway M1 and the antenna. The combination of M1 and the patterned periodic surface imitate a Perfect Magnetic Conductor (AMC) i.e. achieves a reflection coefficient of Γ= +1. This implies the reflected and incident waves are in-phase. Hence, the combination is called an Artificial Magnetic Conductor (AMC).

First, the AMC unit cell is simulated with periodic boundary condition applied to the transverse direction of AMC unit cell (xy-plane), while open boundary condition applied on the longitudinal directions. A wave port is placed at a distance of $\lambda_o \approx 3$mm to ensure the removal of any effects of scattered fields. The reflection phase is very sensitive to mesh settings. Mesh density of 25 steps per wavelength has been optimized. The AMC is optimized to have in-phase at 94 GHz as shown in Fig.2

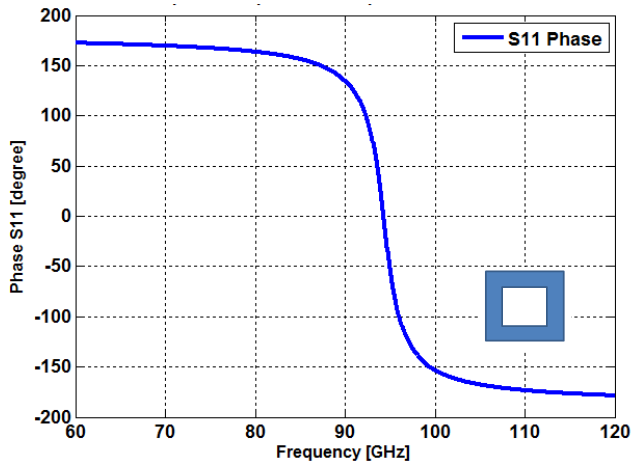

Fig. 2. In-phase response of the proposed AMC.

The dipole is simulated with a 4x4 AMC unit cells being at midway between it and the ground plane. The dipole with the AMC structure has input impedance, at resonance, of about Z_{input}= 15.2 Ω. Fig.3 compares the input impedance of the dipole with and without the AMC structure, the AMC structure increase the dipole impedance to about 15 times which makes it easier to match it to any preceding feeding circuitry. The AMC structure provides a significant gain enhancement of 15.8 dB as the antenna with the AMC has a gain of 4.8 dBi. Fig. 4 compares the dipole gains with and without AMC in both E and H planes.

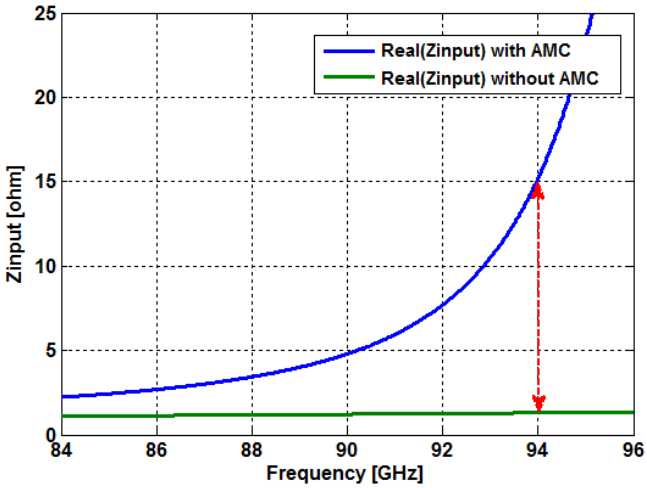

Fig.3. Input impedance of the dipole with and without AMC.

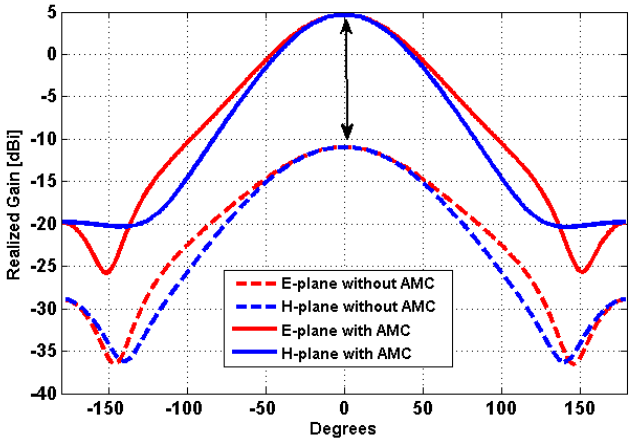

Fig. 4. Realized gain of the dipole antenna with (solid lines) and without (dashed lines) AMC in the E-plane and H-planes.

III. FABRICATED PROTOTYPE AND MEASURED RESULTS

The proposed stack-up shown in Fig.1 has been fabricated in our cleanroom facility. Due to fabrication limitation and material availability, only 0.5 microns of gold has been fabricated instead of 2 microns of copper. To reduce the area without affecting the performance, only 2x4 unit cells has been fabricated .The fabricated prototype is shown in Fig.5.

Fig.5. Photo of the fabricated prototype.

Comparing the measured reflection coefficient to simulated one, both curves show same trend. However, there is a shift in frequency of operation. This shift in frequency might be due to: (1) fabrication tolerance as simulated results are sensitive to +/- 1 micron of a silicon dioxide change and (2) lack of material characterization at 94 GHz as the silicon dioxide has been deposited via Plasma Enhanced Chemical Vapor Deposition (PECVD) which has different dielectric properties (relative permittivity ε_r and tangent loss tanδ) than thermal grown silicon dioxide (ε_r=4 and tanδ≈0).

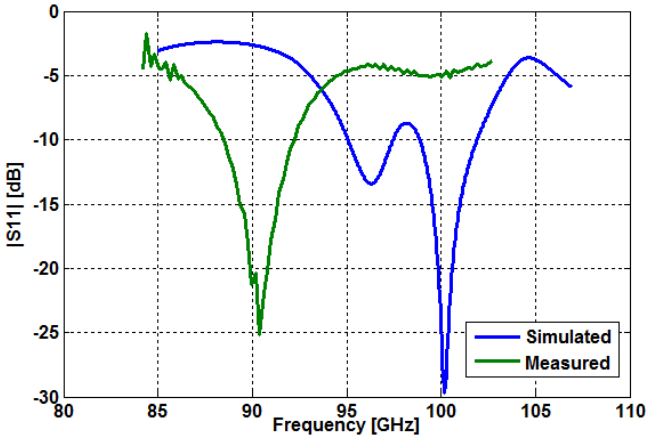

Fig. 6. Measured and simulated reflection coefficient

Table I shows a list of recent published work on mm-wave on-chip antennas. Compared with other work, our proposed antenna shows one of the highest reported gains.

IV. CONCLUSION

In this work, we presented gain enhanced Bi-CMOS on chip dipole antenna. This is achieved by incorporating an AMC midway the antenna and Metal 1. Although the measured reflection coefficient showed same trend as in simulation, there is a shift in frequency of operation which needs further investigation in terms of finding the exact deposited silicon dioxide thickness and its electrical properties at 94 GHz. Despite the ultra-thin oxide thickness (λ_0/100), simulated gain of 4.8 dBi is achieved. The proposed design is superior to many other efficiency enhancement approaches that requires either external components or post processing steps and thus enables a true and efficient SoC.

Table I: Performance Comparison of on-chip antennas

Reference	Antenna Type	Frequency (GHz)	Gain (dBi)
This work	Dipole	94	+4
[4]	Loop	60	-4.4
[5]	Leaky wave	94	-2.5
[6]	Elliptical slot	90	-6
[7]	Patch	79	-1.3

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