

Low-cost silicon wafer dicing using a craft cutter

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Abstract This paper reports a low-cost silicon wafer dicing technique using a commercial craft cutter. The 4-inch silicon wafers were scribed using a crafter cutter with a mounted diamond blade. The pre-programmed automated process can reach a minimum die feature of 3 mm by 3 mm. We performed this scribing process on the top polished surface of a silicon wafer; we also created a scribing method for the back-unpolished surface in order to protect the structures on the wafer during scribing. Compared with other wafer dicing methods, our proposed dicing technique is extremely low cost (lower than \$1,000), and suitable for silicon wafer dicing in microelectromechanical or microfluidic fields, which usually have a relatively large die dimension. The proposed dicing technique is also usable for dicing multiple project wafers, a process where dies of different dimensions are diced on the same wafer.

1 Introduction

The technology of silicon wafer dicing to separate each die from the wafer has been developed over the past five decades. Mechanical wafer dicing using a dicing saw was the industry standard in the semiconductor industry for more

than three decades (Efrat 1993; Takyu et al. 2006; Zhou et al. 2013). However, due to the natural physical contact between the dicing blade and the wafer's surface, chipping and cracking were hard to avoid. When the industry started to use thinner wafers, which are more fragile, mechanical dicing was no longer suitable for the wafer dicing process. In the mean time, with the development of laser techniques, laser ablation was found to be a useful alternative for performing wafer dicing (Jianhua et al. 2007; Kumagai et al. 2007; Venkatakrishnan et al. 2008). Compared to mechanical wafer dicing, laser dicing usually has a higher dicing speed, no physical contact, and a narrower dicing street. Different laser dicing technologies have been reported with laser wavelengths ranging from UV lasers (Zeng et al. 2004) to CO₂ laser (Lizotte 2003); the pulse duration used for wafer dicing has ranged from femtoseconds (Jianhua et al. 2007) to nanoseconds (Panzner et al. 2002). However, heating is the main drawback of laser ablation dicing. Because laser dicing is based on the melting of silicon, the heat generated by the laser may damage the circuitry on chips, leading to a degradation of the mechanical strength of each die. Another group used DRIE (deep reactive-ion etching) to separate the dies from the wafer (Sari et al. 2010), but the DRIE instrument is too expensive and the DRIE process is also time consuming to etch through the entire thickness of a silicon wafer (3 μm/min for 525 μm).

With the development of microelectromechanical (MEMS) and microfluidics technologies, researchers and industries are seeking to lower material and fabrication costs, especially for disposable point-of-care microfluidic chips. Usually, the structures on microfluidic chips are relatively large (~1–30 mm) compared to integrated circuits (ICs), and thus they require lower precision. Nowadays, most of the fabrication instruments for microfluidic chips

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are inherited from the IC industry, which unnecessarily raise the cost of fabrication.

In our proposed technique, a commercial craft cutter is used for silicon wafer dicing. Compared to dicing with a rotary saw or laser ablation, the proposed method lowers equipment cost from more than \$50,000 to \$1,000 for silicon wafer dicing. The minimum die dimension that the proposed method can achieve is 3 mm by 3 mm, which, in most cases, meets the fabrication requirement of microfluidic chips.

2 Fabrication

In this proposed low-cost silicon wafer dicing technique, only three instruments are needed: a commercial craft cutter (Silver Bullet, That's Scrap, Inc., MN, USA), an ordinary office printer and a computer for controlling the cutter and printer. The system setup is shown in Fig. 1.

The detailed silicon wafer dicing process is shown in Fig. 2. A 4-inch silicon wafer (100 orientation) with dies of four different dimensions (10 mm by 10 mm, 7 mm by 7 mm, 5 mm by 5 mm, and 3 mm by 3 mm) were fabricated to demonstrate this dicing process (Fig. 2a). Each die contained a sputtered metal pattern (the laboratory logo), where the metal layer was a combination of a 100 nm thick gold layer on top of a 50 nm thick chromium layer (used to enhance the adhesion to the silicon surface).

The wafer dicing process starts with a series of alignment processes. The first step is aligning the cutting mat (A4 size covered with a low tack adhesive, That's Scrap, Inc.) with a transparency film (PP2500, 3M Inc., Italy) that has the printed cutting patterns (Fig. 2b). The patterns on the transparency film help align the wafer on the cutting mat for the alignment process shown in Fig. 2c. Figure 3 shows the alignment methods between the cutting mat, the silicon wafer, and the transparency film. Figure 3c shows the alignment mark used to align the cutting mat and the transparency film. Figure 3b shows the alignment between the transparency film and the silicon wafer; the metal sputtered lines on the silicon wafer are aligned with the patterns on the transparency film to fix all the degree of freedom. The intersection point on the cutting mat (shown in the red circle) is used later in the process by the craft cutter as the origin point for the programmed wafer-scribing route.

After aligning the wafer on the cutting mat (shown in Fig. 2c) with the help of the transparency film, the transparency film was removed (Fig. 2d). Because the cutting mat has an adhesive layer, the silicon wafer can safely attach to the cutting mat during the wafer scribing process, and it is easily detached after scribing. After all the alignment processes, the final step was scribing.

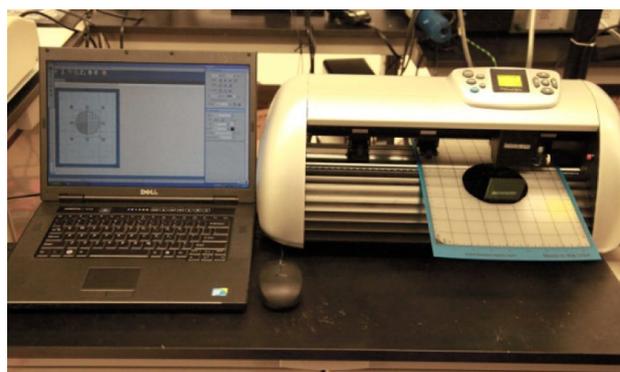


Fig. 1 Wafer dicing system setup

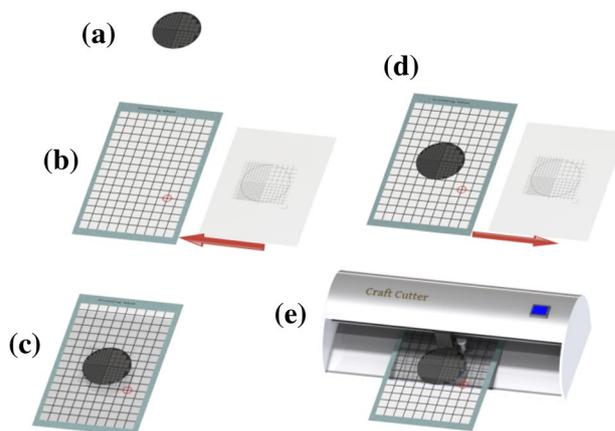


Fig. 2 Wafer alignment and dicing process. **a** Silicon wafer with sputtered metal patterns. **b** Alignment between cutting mat and transparency film. **c** Alignment between silicon wafer and transparency film. **d** Removal of transparency film. **e** Wafer scribing process using craft cutter

The cutting mat with the attached silicon wafer was fed into the craft cutter. The diamond blade was carefully aligned to the intersection point (center of the red circle in Fig. 3a) on the cutting mat. This intersection point is the origin point (bottom right point) in the designed cutting routine (drawings were designed using CorelDRAW X4). The craft cutter was controlled by software (Sure cuts a lot 3) to perform the dicing process; the speed of the diamond blade was 40 mm/s while the scribing force between the diamond tip and silicon wafer was 0.6 N. After scribing, the wafer was carefully removed from the cutting mat and cleaned with nitrogen gas. Then the wafer was snapped along the cutting line using tweezers to finish the dicing process.

The procedure of backside silicon wafer dicing using the craft cutter was similar to the previously mentioned front side dicing method. A layer of 4- μ m-thick photoresist (ECI 3027, AZ Electronic Materials, Somerville, NJ, USA) was

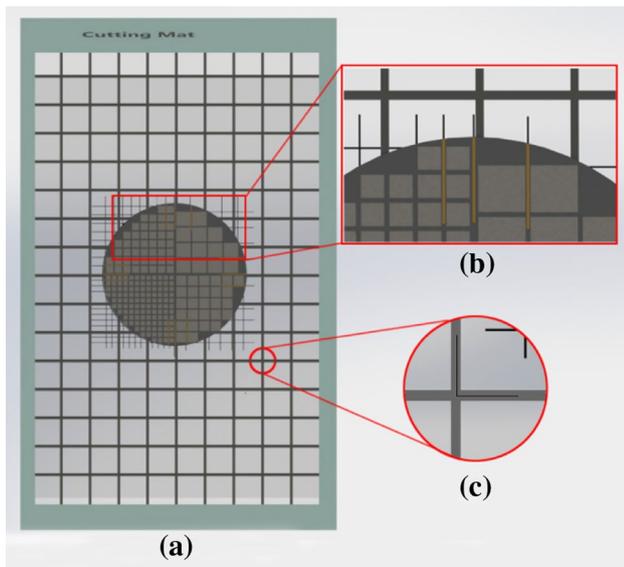


Fig. 3 **a** The alignment between the cutting mat, silicon wafer, and transparency film; **b** alignment between the wafer and transparency film; **c** alignment between the transparency film and cutting mat

spin-coated on the front surface of the wafer to protect the structures; then the wafer was aligned using the same method described in Fig. 2 on the cutting mat, but this time, the front surface was touching the adhesive layer on the cutting mat. During the backside scribing, the diamond blade was scribing on the backside of the wafer, leaving the scribed grooves only on the backside. After scribing, the wafer was removed from the cutting mat, and the protective photoresist was dissolved using acetone. Comparing both front side and back side scribing, the wafer with the backside scribing has a cleaner top surface because no contamination from the silicon fragments was generated during scribing.

3 Results and discussion

The dicing process was accomplished using the scribing method presented followed by snapping of the silicon wafer. The silicon wafer after scribing is shown in Fig. 4a. The die dimensions are 3 mm by 3 mm and 5 mm by 5 mm, respectively. The separated dies are shown in Fig. 3b, from visual observation, the scribing line is slightly shifted (~0.3 mm) from the center due to imperfect alignment. In this proposed low-cost silicon wafer dicing method, the alignment process has three steps; each step needs careful alignment of the fiducial marks by hand. Due to the multiple manual alignment processes, the minimum die dimension is limited to a degree of several millimetres. After careful evaluation of random users without alignment

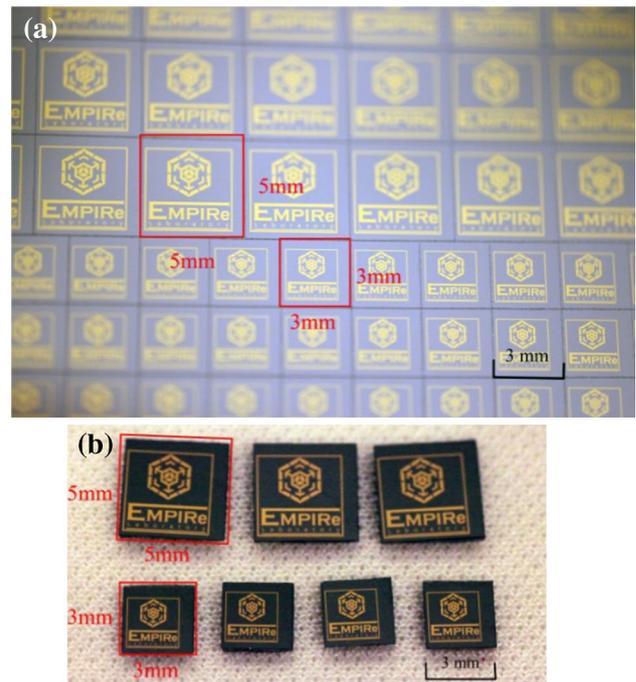


Fig. 4 Silicon wafer after dicing with die dimensions of 5 mm by 5 mm and 3 mm by 3 mm

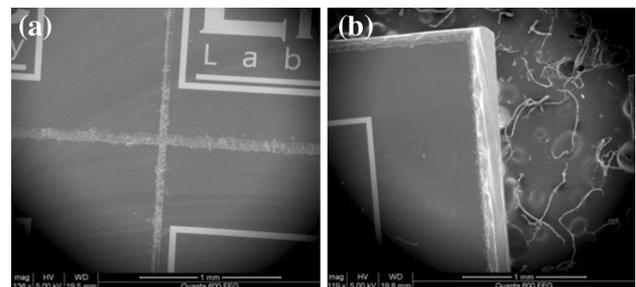


Fig. 5 **a** SEM image of the dicing streets; **b** edges of single 3 mm by 3 mm die

experience, a die feature of 3 mm by 3 mm could easily be achieved without intensive user training.

The SEM (scanning electron microscope) images are provided in Fig. 5 to show the dicing streets and edge quality. The surface of the dicing street is a little bit rough due to the mechanical scribing of the diamond grains on the silicon surface. The profile of the dicing streets is shown in Fig. 6 measured by profilometer (Ambios XP-200); the dicing streets have a consistent width of 52 μm and a depth of 7.5 μm.

The proposed silicon wafer dicing method could easily achieve the multiple project wafers (MPW) dicing, where dies of different dimensions are diced on the same wafer. Another advantage compared to dicing tapes used

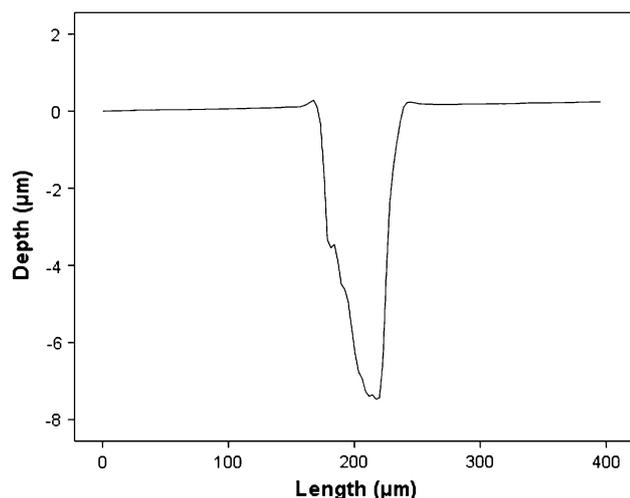


Fig. 6 Cross-section profile of a dicing street

in traditional dicing (mechanical and laser) process is that, in our proposed method, the cutting mat could be reused, which further lowers the fabrication cost.

4 Conclusion

This paper proposed a low-cost silicon wafer dicing method using a commercial craft cutter. Compared to traditional wafer dicing methods using a rotary dicing saw or laser ablation, our proposed method significantly lowers the instrument and fabrication cost. The low-cost silicon wafer dicing methods from both the front-side and backside were introduced. The minimum die dimension of 3 mm by 3 mm could easily be achieved using the proposed technique. This silicon wafer dicing method is suitable in the MEMS or microfluidics chip fabrication process, which usually have a large die dimension and require low fabrication cost.

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References

- Efrat U (1993) Optimizing the wafer dicing process. In: Electronic Manufacturing Technology Symposium, 1993, Fifteenth IEEE/CHMT International, 4–6 Oct 1993, pp 245–253. doi:[10.1109/iemt.1993.398195](https://doi.org/10.1109/iemt.1993.398195)
- Jianhua L, Hyeon H, Eun-Chul A, Qiang C, Pyoungwan K, Teakhoon L, Myeongkee C, Taeyeong C (2007) Laser dicing and subsequent die strength enhancement technologies for ultra-thin wafer. In: Electronic Components and Technology Conference, 2007. ECTC '07. 57th Proceedings. May 29 2007–June 1 2007, pp 761–766. doi:[10.1109/ectc.2007.373883](https://doi.org/10.1109/ectc.2007.373883)
- Kumagai M, Uchiyama N, Ohmura E, Sugiura R, Atsumi K, Fukumitsu K (2007) Advanced dicing technology for semiconductor wafer—stealth dicing. *Semicond Manuf IEEE Trans* 20(3):259–265. doi:[10.1109/tsm.2007.901849](https://doi.org/10.1109/tsm.2007.901849)
- Lizotte T (2003) Laser dicing of chip scale and silicon wafer scale packages. In: Electronics Manufacturing Technology Symposium, 2003. IEMT 2003. IEEE/CPMT/SEMI 28th International, 16–18 July 2003, pp 1–5. doi:[10.1109/iemt.2003.1225869](https://doi.org/10.1109/iemt.2003.1225869)
- Panzner M, Kasper J, Wust H, Klotzbach U, Beyer E (2002) In: Processing of silicon by Nd:YAG lasers with harmonics generation 2002, pp 496–504
- Sari I, Zeimpekis I, Kraft M (2010) A full wafer dicing free dry release process for MEMS devices. *Procedia Eng* 5:850–853
- Takyu S, Kurosawa T, Shimizu N, Harada S (2003) Novel wafer dicing and chip thinning technologies realizing high chip strength. In: Electronic Components and Technology Conference, 2006. Proceedings 56th, 0–0 2006, p 5. doi:[10.1109/ectc.2006.1645874](https://doi.org/10.1109/ectc.2006.1645874)
- Venkatakrishnan K, Sudani N, Tan B (2008) A high-repetition-rate femtosecond laser for thin silicon wafer dicing. *J Micromech Microeng* 18(7):075032
- Zeng XJ, Mao X, Greif R, Russo RE (2004) Ultraviolet femtosecond and nanosecond laser ablation of silicon. In: Proceedings of the SPIE, vol 5448, pp 1150–1158. doi:[10.1117/12.544401](https://doi.org/10.1117/12.544401)
- Zhou H, Qiu S, Huo Y, Zhang N (2013) High-speed dicing of silicon wafers conducted using ultrathin blades. *Int J Adv Manuf Technol* 66(5–8):947–953. doi:[10.1007/s00170-012-4379-6](https://doi.org/10.1007/s00170-012-4379-6)