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# Gate-last TiN/$HfO_2$ band edge effective work functions using low-temperature anneals and selective cladding to control interface composition

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Silicon N-metal-oxide-semiconductor (NMOS) and P-metal-oxide-semiconductor (PMOS) band edge effective work functions and the correspondingly low threshold voltages ($V_t$) are demonstrated using standard fab materials and processes in a gate-last scheme employing low-temperature anneals and selective cladding layers. Al diffusion from the cladding to the TiN/$HfO_2$ interface during forming gas anneal together with low O concentration in the TiN enables low NMOS $V_t$. The use of non-migrating W cladding along with experimentally detected N-induced dipoles, produced by increased oxygen in the TiN, facilitates low PMOS $V_t$. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3701165]

Recent publications in advanced high-k and metal gate (HK/MG) stack technology[1–8] demonstrate the division between gate-first and gate-last strategies employed by those in the field. Gate-first HK/MG technologies have been presented for the 45 nm (Ref. 9) and 32 nm (Ref. 10) generations, while a number of researchers have investigated the ability to set near band edge work functions for gate-first using selective capping layers such as $La_2O_3$ for N-metal-oxide-semiconductor (NMOS)[11] and $Al_2O_3$ for P-metal-oxide-semiconductor (PMOS).[12] However, there are a number of issues to using this technique particularly for PMOS where an ideal capping layer that does not cause equivalent oxide thickness (EOT) and mobility degradation has been elusive.[12] Conversely, gate-last technologies have also been demonstrated for the 45 nm (Ref. 13) and 32 nm (Refs. 14 and 15) generations, but less is known about the exact integration techniques and effective work function (EWF) setting mechanisms for the gate-last scheme. In this letter, band edge EWFs and the resulting low threshold voltages ($V_t$s) for NMOS and PMOS are demonstrated using standard fab materials and processes by controlling the HK/MG interfacial composition and structure using different cladding layers and low temperature anneals. Additionally, the mechanism that N-induced dipoles at the HK/MG interface have a large effect on determining the PMOS EWF, suggested previously using first-principle calculations,[16] is demonstrated using backside dynamic secondary ion mass spectroscopy (DSIMS) experimental results.

Gate-last NMOS and PMOS field-effect transistors (FETs) were separately fabricated using a gate stack comprised of 1.0 nm thermally grown $SiO_2$ and 2.0 nm atomic layer deposition (ALD) $HfO_2$ using tetrakis dimethyl amino hafnium (TDMA-Hf) and ozone as the metal organic precursor and oxidant, respectively. A 60 s, 700 °C post-deposition anneal was performed in $N_2$ after $HfO_2$ deposition. TiN metal gates of 10 nm thickness were deposited using radio frequency (RF) sputtering. Rapid thermal anneals (RTAs) were performed *post-TiN deposition* in trace $O_2$ in $N_2$ or in 10% $O_2$ in a balance of $N_2$ (10% $O_2/N_2$) at atmospheric pressure for 30 s. Films of either 500 nm Al or W were RF sputtered as a cladding layer and metal contact prior to gate metal patterning. All devices underwent a 400 °C forming gas anneal (FGA) in 10% $H_2$ in a balance of $N_2$ to complete processing. Cation-SIMS (CSIMS)[16] was performed on annealed samples of blanket 10 nm TiN films sputtered *in-situ* following a thick amorphous-Si sputter deposition where the TiN is capped with Al or W cladding post-TiN anneal for direct comparison with the electrical test device samples. Backside DSIMS was performed on the device structures following thinning of the Si substrate to minimize any knock-on effects from the metal cladding.

The drain current vs. gate voltage ($I_d$-$V_g$) data in Fig. 1 demonstrate low $V_t$ for 1.1 nm EOT NMOS Al/TiN/$HfO_2$ and PMOS W/TiN/$HfO_2$ at 0.08 V and −0.20 V, respectively, obtained through control of the HK/MG interfacial composition. The curves correspond to Al- and W-clad devices either with FGA-only or with a 30 s, 450 °C anneal in 10% $O_2/N_2$ post-TiN deposition. The W-clad devices always exhibit a higher EWF than their Al-clad counterparts while the 10% $O_2/N_2$ anneal shows significantly higher EWFs than the FGA-only samples (Fig. 2).

Physical characterization of the gate stacks provides insight into the mechanisms occurring to set the various EWFs demonstrated in these materials systems. Figure 3 shows backside DSIMS data of the Al and W cladding elements throughout the gate stacks as a function of post-TiN anneal. Al migration (following FGA) through the TiN that

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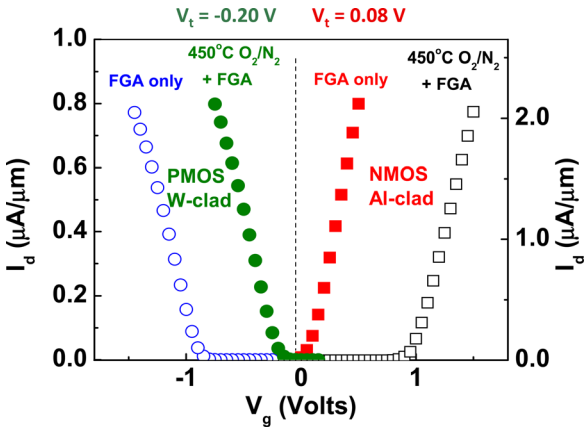


FIG. 1. $I_d$-$V_g$ of 1.1 nm EOT $HfO_2$/TiN PMOS and NMOS FETs with various low-temperature anneals and selective metal cladding layers. Employing a 450 °C 10% $O_2/N_2$ post-TiN anneal with a W-cladding layer allows for a PMOS $V_t = -0.20$ V. Using Al-cladding with no post-TiN anneal gives an NMOS $V_t = 0.08$ V.

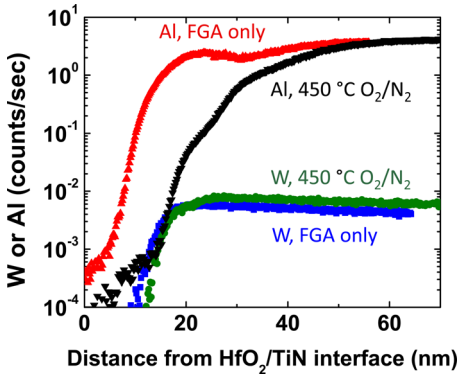


FIG. 3. Backside DSIMS data of metal cladding concentration. During FGA, the Al-cladding diffuses through the unoxidized TiN, reaching the $HfO_2$/TiN interface setting a low NMOS EWF. The Al migration is significantly suppressed through oxidized TiN. The W-cladding does not migrate to the $HfO_2$/TiN interface.

was not exposed to a post-TiN anneal allows for segregation of low-WF Al at the TiN/$HfO_2$ interface for those specific Al-clad samples. There is no analogous migration of the cladding metal for the W-clad samples, which explains the difference in the EWFs for the $HfO_2$/TiN with no post-TiN anneal with the two different cladding layers. This Al segregation at the interface is critical in obtaining low NMOS $V_t$. Interestingly, the samples exposed to the 450 °C post-TiN anneal in 10% $O_2/N_2$ show a significantly suppressed Al migration (although there is still more metal diffusion than for the W-clad samples) compared to the previous unannealed sample. (It is noted once again that the low temperature oxidizing anneals are performed post-TiN deposition *prior* to cladding layer deposition.) The increased oxygen levels in the TiN following that anneal apparently act as an Al diffusion barrier.

As reported previously,[16] by employing these different annealing ambients, the concentration of oxygen at the $HfO_2$/TiN interface may be accurately controlled. However, it was previously postulated through analysis of density functional theory (DFT) calculations that the role of oxygen alone is incapable of producing the necessary shifts to achieve band-edge PMOS EWFs, even when considering the filling of oxygen vacancies in the $HfO_2$. The simulation results (not shown) indicate that the dipoles resulting from the substitution of N with O in the bulk of the TiN result in only $\Delta EWF \sim 30$ meV due to metallic screening within the electrode. The filling of O-vacancies (8.3% concentration) in the $HfO_2$ increases the EWF by ~120 meV, which is a much smaller amount than the observed $V_t$ shifts. To confirm this experimentally, TiN/$SiO_2$ gate stacks (i.e., without $HfO_2$) were fabricated and exposed to the same annealing conditions described above. An EWF increase of ~400 meV after the 450 °C 10% $O_2/N_2$ post-TiN anneal is observed (Fig. 4). Assuming that $SiO_2$ has a lower concentration of O-vacancies than $HfO_2$, the filling of O-vacancies in the $HfO_2$ is not adequate by itself to explain the EWF shift.

The DFT simulations suggest that the largest effect on the EWF is dipoles resulting from N atoms, displaced from the TiN during the low temperature oxidizing anneal, migrating to the metal/dielectric interface.[16] Backside DSIMS analysis of these gate stacks provides evidence that this N displacement truly is occurring. As can be seen in Fig. 5, the N concentration profile is different for the sample exposed to the 450 °C 10% $O_2/N_2$ post-TiN anneal compared to the sample with no post-TiN anneal (both W-clad in this figure). The N concentration of the annealed gate stack is increased at the $HfO_2$/TiN interface and extends into the $HfO_2$ by approximately 1 nm compared to the unannealed stack while the top TiN surface is N deficient due to the oxidation of the TiN. The O and Ti concentrations are shown in the insets of

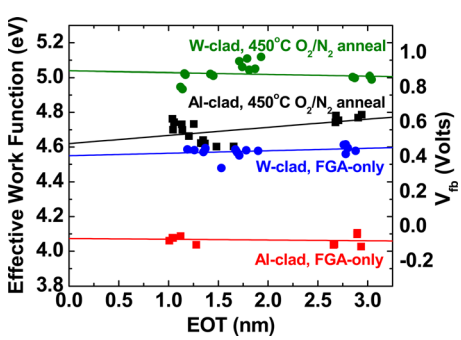


FIG. 2. Flatband voltage ($V_{fb}$) vs. EOT plots for the $HfO_2$/TiN gate stacks with different post-TiN anneals and cladding layers. The left axis displays the extracted EWF for each set of devices.

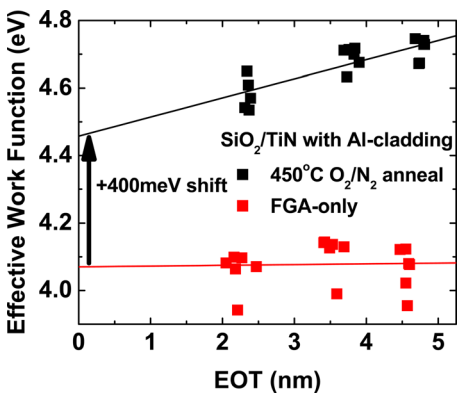


FIG. 4. TiN/$SiO_2$ gate stacks exhibit EWF shifts of ~400 meV after 450 °C $O_2/N_2$ anneal. This suggests that the filling of O-vacancies in $HfO_2$ is not adequate by itself to explain the EWF shift.

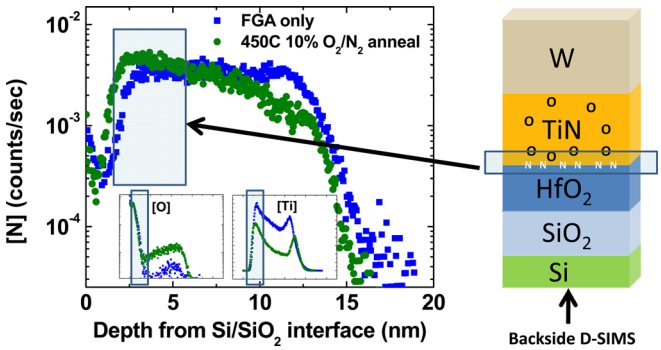


FIG. 5. Backside DSIMS data showing N displacement from the TiN to the $HfO_2$/TiN interface and slightly into the $HfO_2$ following the 450 °C 10% $O_2/N_2$ post-TiN anneal. The insets emphasize that the $HfO_2$/TiN interfacial edge, defined by the O and Ti concentrations, overlaps for both samples, indicating that the difference in N concentration near that interface is indeed evidence of N displacement.

Fig. 5 for comparison that the interface edges for both the annealed and unannealed stacks overlap for those elemental species. This indicates that the N extension into the $HfO_2$ is real and not due to mis-calibration of the depth scale.

It should also be noted that the EOT and the subthreshold slopes of the differently processed devices are identical, regardless of whether they were exposed to a 450 °C 10% $O_2/N_2$ post-TiN anneal or not. This suggests that the low-temperature oxidizing anneals do not significantly degrade the electrical thickness or channel interface.

In summary, low NMOS and PMOS $V_t$ of TiN/$HfO_2$ gate stacks with minimal EOT and interface degradation can be obtained via low temperature anneal and selective cladding layers using only fab-friendly materials and processes. For NMOS work functions, Al migration from the cladding to the TiN/$HfO_2$ interface during FGA in conjunction with low O concentration in the TiN enables a low EWF. For PMOS work functions, the use of non-migrating W cladding along with a N-induced dipole, resulting from displacement of N during the low temperature oxidizing anneal of the TiN, facilitates a high EWF.

[1]H. J. Li and M. I. Gardner, IEEE Electron Device Lett. **26**, 441 (2005).
[2]J. K. Schaeffer, L. R. C. Fonseca, S. B. Samavedam, Y. Liang, P. J. Tobin, and B. E. White, Appl. Phys. Lett. **85**, 1826 (2004).
[3]E. Cartier, F. R. McFeely, V. Narayanan, P. Jamison, B. P. Linder, M. Copel, V. K. Paruchuri, V. S. Basker, R. Haight, D. Lim, R. Carruthers, T. Shaw, M. Steen, J. Sleight, J. Rubino, H. Deligianni, S. Guha, R. Jammy, and G. Shahidi, Dig. Tech. Pap. – Symp. VLSI Technol. **2005**, 230.
[4]B. Chen, R. Jha, H. Lazar, N. Biswas, J. Lee, B. Lee, L. Wielunski, E. Garfunkel, and V. Misra, IEEE Electron Device Lett. **27**, 228 (2006).
[5]J. Lee, H. Park, H. Choi, M. Hasan, M. Jo, M. Chang, B. H. Lee, C. S. Park, C. Y. Kang, and H. Hwang, Appl. Phys. Lett. **92**, 263505 (2008).
[6]E. Cartier, M. Steen, B. P. Linder, T. Ando, R. Iijima, M. Frank, J. S. Newbury, Y. H. Kim, F. R. McFeely, M. Copel, R. Haight, C. Choi, A. Callegari, V. K. Paruchuri, and V. Narayanan, Dig. Tech. Pap. – Symp. VLSI Technol. **2009**, 42.
[7]W. Mizubayashi, K. Akiyama, W. Wang, M. Ikeda, K. Iwamoto, Y. Kamimuta, A. Hirano, H. Ota, T. Nabatame, and A. Toriumi, Dig. Tech. Pap. – Symp. VLSI Technol. **2008**, 42.
[8]E. Cartier, M. Hopstaken, and M. Copel, Appl. Phys. Lett. **95**, 042901 (2009).
[9]M. Chudzik, B. Doris, R. Mo, J. Sleight, E. Cartier, C. Dewan, D. Park, H. Bu, W. Natzle, W. Yan, C. Ouyang, K. Henson, D. Boyd, S. Callegari, R. Carter, D. Casarotto, M. Gribelyuk, M. Hargrove, W. He, Y. Kim, B. Linder, N. Moumen, V. K. Paruchuri, J. Stathis, M. Steen, A. Vayshenker, X. Wang, S. Zafar, T. Ando, R. Iijima, M. Takayanagi, V. Narayanan, R. Wise, Y. Zhang, R. Divakaruni, M. Khare, and T. C. Chen, Dig. Tech. Pap. – Symp. VLSI Technol. **2007**, 194.
[10]X. Chen, S. Samavedam, V. Narayanan, K. Stein, C. Hobbs, C. Baiocco, W. Li, D. Jaeger, M. Zaleski, S. Yang, N. Kim, Y. Lee, D. Zhang, L. Kang, J. Chen, H. Zhuang, A. Sheikh, J. Wallner, M. Aquilino, J. Han, Z. Jin, J. Li, G. Massey, S. Kalpat, R. Jha, N. Moumen, R. Mo, S. Kershnan, X. Wang, M. Chudzik, M. Chowdhury, D. Nair, C. Reddy, Y. W. Teh, C. Kothandaraman, D. Coolbaugh, S. Pandey, D. Tekleab, A. Thean, M. Sherony, C. Lage, J. Sudijono, R. Lindsay, J.-H. Ku, M. Khare, and A. Steegen, Dig. Tech. Pap. – Symp. VLSI Technol. **2008**, 88.
[11]H. N. Alshareef, H. R. Harris, H. C. Wen, C. S. Park, C. Huffmann, K. Choi, H. F. Luan, P. Majhi, B. H. Lee, R. Jammy, D. J. Lichtenwalner, J. S. Jur, and A. I. Kingon, Dig. Tech. Pap. – Symp. VLSI Technol. **2006**, 7.
[12]K. Tatsumura, T. Ishihara, S. Inumiya, K. Nakajima, A. Kaneko, M. Goto, S. Kawanaka, and A. Kinoshita, Tech. Dig. - Int. Electron Devices Meet. **2008**, 25.
[13]K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C. H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, Tech. Dig. - Int. Electron Devices Meet. **2007**, 247.
[14]P. Packan, S. Akbar, M. Armstrong, D. Bergstrom, M. Brazier, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, J. Jopling, C. Kenyon, S.-H. Lee, M. Liu, S. Lodha, B. Mattis, A. Murthy, L. Neiberg, J. Neirynck, S. Pae, C. Parker, L. Pipes, J. Sebastian, J. Seiple, B. Sell, A. Sharma, S. Sivakumar, B. Song, A. St. Amour, K. Tone, T. Troeger, C. Weber, K. Zhang, Y. Luo, and S. Natarajan, Tech. Dig. - Int. Electron Devices Meet. **2009**, 659.
[15]C.-H. Jan, M. Agostinelli, M. Buehler, Z.-P. Chen, S.-J. Choi, G. Curello, H. Deshpande, S. Gannavaram, W. Hafez, U. Jalan, M. Kang, P. Kolar, K. Komeyli, N. Lazo, T. Leo, J. Lin, N. Lindert, S. Ma, L. McGill, C. Meining, A. Paliwal, J. Park, K. Phoa, I. Post, N. Pradhan, M. Prince, A. Rahman, J. Rizk, L. Rockford, G. Sacks, H. Tashiro, C. Tsai, P. Vandervoorn, J. Xu, L. Yang, J.-Y. Yeh, J. Yip, K. Zhang, and P. Bai, Tech. Dig. - Int. Electron Devices Meet. **2009**, 647.
[16]C. L. Hinkle, R. V. Galatage, R. A. Chapman, E. M. Vogel, H. N. Alshareef, C. Freeman, E. Wimmer, H. Niimi, A. Li-Fatou, J. B. Shaw, and J. J. Chambers, Appl. Phys. Lett. **96**, 103501 (2010).