Nanoscale gadolinium oxide capping layers on compositionally variant gate dielectrics

H. N. Alshareef, J. A. Caraveo-Frescas, and D. K. Cha

Citation: Applied Physics Letters **97**, 202108 (2010); doi: 10.1063/1.3519363
View online: http://dx.doi.org/10.1063/1.3519363
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/97/20?ver=pdfcov
Published by the AIP Publishing

Nanoscale gadolinium oxide capping layers on compositionally variant gate dielectrics

H. N. Alshareef,[1,a)] J. A. Caraveo-Frescas,[1] and D. K. Cha[2]
[1]*Materials Science and Engineering, King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia*
[2]*Advanced Nanofabrication, Imaging and Characterization Laboratory, King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia*

(Received 5 September 2010; accepted 28 October 2010; published online 19 November 2010)

Metal gate work function enhancement using nanoscale (1.0 nm) Gd_2O_3 interfacial layers has been evaluated as a function of silicon oxide content in the $Hf_xSi_yO_z$ gate dielectric and process thermal budget. It is found that the effective work function tuning by the Gd_2O_3 capping layer varied by nearly 400 mV as the composition of the underlying dielectric changed from 0% to 100% SiO_2, and by nearly 300 mV as the maximum process temperature increased from ambient to 1000 °C. A qualitative model is proposed to explain these results, expanding the existing models for the lanthanide capping layer effect. © *2010 American Institute of Physics*. [doi:10.1063/1.3519363]

Metal gate work function engineering in transistor devices is a subject of great interest in the semiconductor community. Rare-earth oxide capping has been demonstrated as an effective method to tune the work function of metal gates on Hf-based dielectrics.[1] La_2O_3 has received the greatest attention, although Gd_2O_3 is especially significant because of its potential in non-Si based devices (although normally in solid solution with Ga_2O_3).[2,3] Most analysis of the role of the lanthanides focused on the thickness and composition of the capping rare-earth oxide layer. However, the dependence on the underlying gate dielectric composition and thermal budget has not been systematically investigated. In this article, we show that the amount of work function tuning by the Gd_2O_3 capping layer strongly depends on the SiO_2 content in the underlying $Hf_xSi_yO_z$ gate dielectric and propose a mechanism to explain the observed results.

Capacitors were built on heavily doped p-type substrates with a dopant concentration of 1.2×10^{18} cm^{-3}. Pregate cleaning was performed using diluted hydrofluoric acid (HF) followed by O_3-last cleaning. The SiO_2 gate dielectric was grown using thermal oxidation, while the HfO_2 and $Hf_xSi_yO_z$ films (2.0 nm) were grown by atomic layer deposition. The 1.0 nm Gd_2O_3 interfacial layer and 10 nm TaN gate electrode were then deposited at room temperature using a physical vapor deposition system. The stack was then capped with polycrystalline silicon (poly-Si), implanted by phosphorous, and then annealed at 1000 °C for 10 s to activate the dopants. In some samples, no poly-Si was deposited, instead, a 40 nm thick TaN was used to allow studying of the stack at lower temperatures (no poly-Si activation). The backside of the wafer was coated with Al metal to improve the electrical contact. The C-V curves were fitted using the NCSU model to extract the equivalent oxide thickness (EOT), flat-band voltage (V_{FB}), and substrate doping concentration.[4] The effective work function of each electrode was extracted from the plots of V_{FB} versus EOT using a series of SiO_2 thicknesses (1.0–4.0 nm) formed by wet-etching of a thermally grown 4.0 nm SiO_2 layer.

Figure 1 shows the capacitance-voltage (C-V) curves obtained from $TaN/Gd_2O_3/Hf_xSi_yO_z/SiO_2/Si$ stacks. Figure 1 demonstrates that these devices have well-behaved C-V curves and show a marked shift in V_{FB} as the SiO_2 content in the gate dielectric increases from 0% to 100% in $Hf_xSi_yO_z$ [$\%SiO_2=y/(x+y)^*100$]. The dashed curve is for a reference device without Gd_2O_3 ($TaN/Hf_{0.4}Si_{0.6}O_z/SiO_2/Si$). With the 1.0 nm Gd_2O_3 capping layer, nearly 400 mV shift in V_{FB} is observed. In fact, the absolute value of V_{FB} shift (ΔV_{FB}) varies nearly linearly with the fraction of SiO_2 in the gate dielectric, $\Delta V_{FB}(mV)=aX_{SiO2}+b$, where $X_{SiO2}=y/(x+y)$, a and b are constants that depend on the stack and are equal to 370 and 60 mV, respectively, for the $Gd_2O_3/Hf_xSi_yO_z$ system. Figure 2 shows V_{FB} versus EOT plots for four devices: (a) reference device without Gd_2O_3 and [(b)–(d)] devices with 1.0 nm Gd_2O_3 capping layer deposited on $Hf_xSi_yO_z$ dielectric containing 0%, 60%, and 100% SiO_2, respectively. The curve shows a shift in V_{FB} as a function of $\%SiO_2$ independent of the interfacial SiO_2 layer thickness (which was

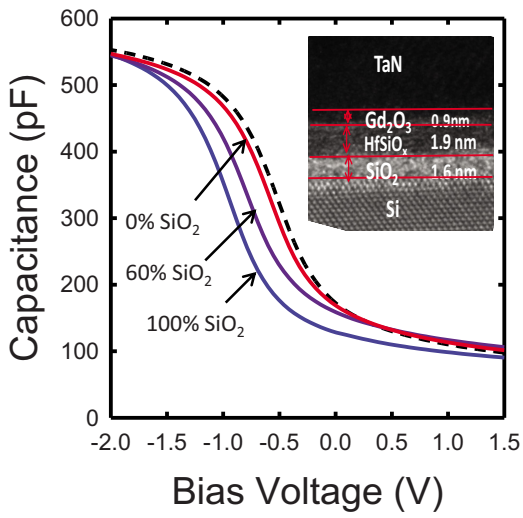

FIG. 1. (Color online) C-V curves of devices with nearly the same EOT showing the gradual shift in C-V curve with $\%SiO_2$ in the gate dielectric. The dotted line is for a device without the Gd_2O_3 capping layer. The inset shows a TEM x-section of the stack.

a)Author to whom correspondence should be addressed. Electronic mail: husam.alshareef@kaust.edu.sa.

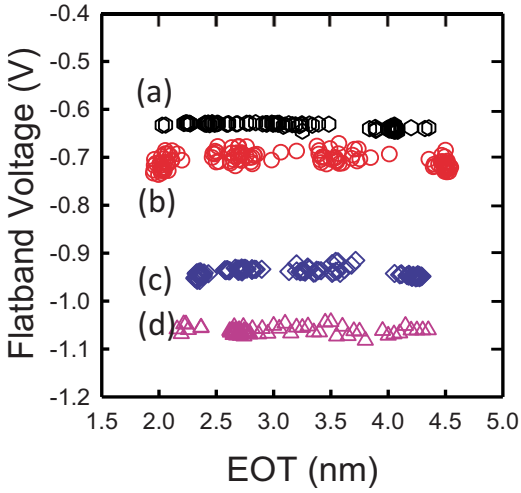

FIG. 2. (Color online) V_{FB}-EOT plots showing the shift in V_{FB} over a range of EOTs for samples (a) without Gd_2O_3 capping layer and for samples with 1.0 nm Gd_2O_3 capping layer where gate dielectric contains (b) 0% SiO_2, (c) 60% SiO_2, and (d) 100% SiO_2. Negligible interfacial fixed charges are obtained.

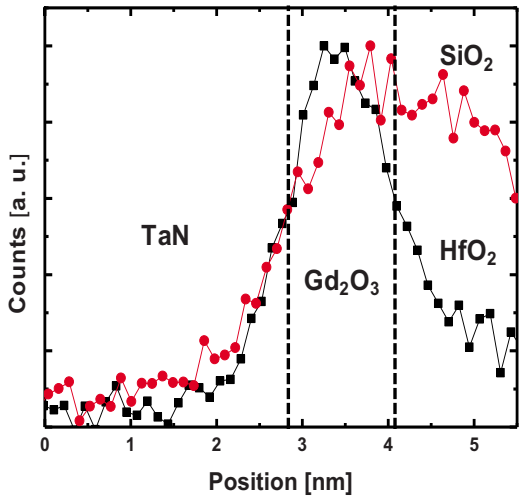

FIG. 4. (Color online) EELS chemical profile recorded across Gd_2O_3 containing gate stacks. The results show the Gd element signal variation with depth in Gd_2O_3/SiO_2 and Gd_2O_3/HfO_2 stacks. The Gd has diffused toward the Si interface, but not into TaN. Furthermore, the normalized concentration plot shows that more Gd has diffused in the case of SiO_2 than HfO_2.

varied from 1.0 to 4.0 nm, giving 2.0–4.5 EOTs). Furthermore, it is interesting to note that the fixed-charge concentration in all these devices is relatively small, around $1-6 \times 10^{10}$ cm^{-2}, as calculated from the slope of the V_{FB} versus EOT plots in Fig. 2. The effective work function of the TaN metal gate used here was extracted from Fig. 2 and is shown in Fig. 3 for stacks with 1.0 nm Gd_2O_3 on HfO_2 (0% SiO_2), $Hf_{0.4}Si_{0.6}O_z$ (60% SiO_2), and SiO_2 (100% SiO_2). Note that the largest shift in the work function caused by the Gd_2O_3 capping layer occurs for the 100% SiO_2 dielectric, consistent with the V_{FB} shifts observed earlier.

It has been shown that rare-earth oxides deposited directly on SiO_2 tend to diffuse toward the SiO_2/Si layer often resulting in silicate formation even at temperatures as low as 400 °C.[5–8] It is not surprising that such reactions occur since the free energy of oxide formation ΔG_f for rare-earth oxides is significantly more negative than SiO_2 (−856 versus −1730 kJ/mol for SiO_2 and Gd_2O_3, respectively).[9] In our samples, Gd intensity profiles were obtained from electron energy loss spectroscopy (EELS) analysis and show that Gd has clearly diffused within the gate stack, although the original Gd_2O_3 capping layer remains distinct (Fig. 4). Figure 4 shows that the Gd levels are significantly higher in the gate dielectric region compared to the TaN gate region, indicating downward diffusion. Furthermore, Fig. 4 shows that the normalized intensities of Gd are higher in the case of underlying SiO_2 dielectric than in the case of HfO_2 dielectric, providing significant information to help understand the observed device behaviors, as will be discussed shortly. The V_{FB} shift observed with lanthanide capping on Hf-based dielectrics has been correlated with three main mechanisms including (1) positive fixed charges generated due to substitution of lanthanide cations on Hf^{4+} sites forming positively charged O vacancies,[10] (2) dipole formation involving the rare-earth (RE) atoms at the interface,[11,12] and (3) work function of the metal of the metal-oxide capping layer (Gd, La, etc.) and dielectric constant discontinuity.[13] Relating these models to %SiO_2 content in the gate dielectric or thermal budget has not been specifically discussed.

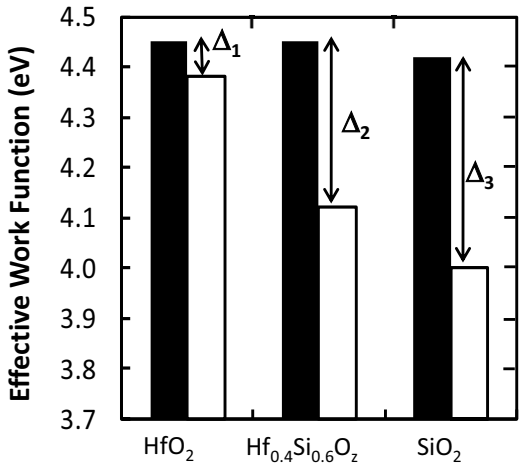

FIG. 3. Extracted effective work function (EWF) values as a function of %SiO_2 in the gate dielectric where all devices had 1.0 nm Gd_2O_3 capping layer. The magnitude of the increase in EWF is marked by Δ_1, Δ_2, and Δ_3.

The low values of fixed charges in our stacks for all dielectric compositions studied ($1-5 \times 10^{10}$ cm^{-2}) clearly show that the observed V_{FB} shifts cannot simply be due to fixed charge accumulation (such as oxygen vacancies generated from Gd^{3+} substitution on Hf^{4+} or Si^{4+} sites). This assertion is also supported by the fact that Al and La capping layers produce shifts in opposite directions despite having the same valence, ruling out the fixed charge model.[14,15] On the other hand, the dipole model can predict the V_{FB} shifts both in sign and in magnitude by calculating the dipole moment of the RE–O, Si–O, Hf–O bonds using bond distances and electronegativity.[11] To determine if the dipole model can explain the composition and temperature dependence of the V_{FB} shifts caused by Gd_2O_3 in our samples, we reiterate that our data indicate that significant Gd diffusion takes place in our gate stacks. The driving force for this diffusion is most likely the difference in the free energy of oxide formation between the lanthanide capping layer and SiO_2 as mentioned earlier. Due to the presence of the SiO_2 interfacial layer, there will always be a higher concentration of SiO_2 near silicon substrate which acts to drive the lanthanide element layer closer to the bottom interface as previously

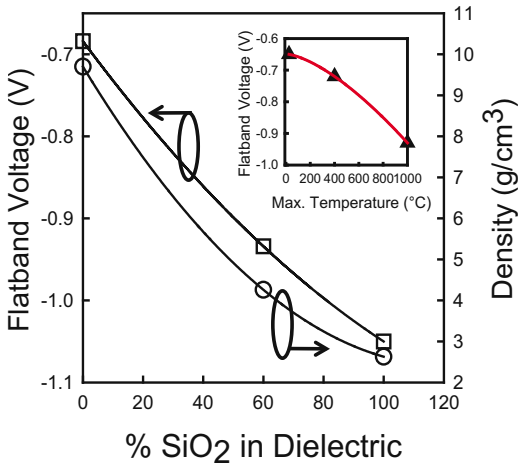

FIG. 5. (Color online) Results showing the V_{FB} shift as a function of $\%SiO_2$ in the gate dielectric and gate dielectric density. The inset shows the impact of maximum thermal budget on V_{FB} shift for 60% SiO_2 dielectric.

demonstrated.[4,6,7] The kinetics (rate) of this diffusion reaction depends on many factors. In our data, Fig. 5 shows two important effects. One is that the atomic density of the gate dielectric correlates well with the observed V_{FB} shifts. HfO_2 has a relatively large density of 9.7 g/cm^3, hence producing the smallest V_{FB} shifts. This is believed to be a result of limited lanthanide metal diffusion through the dense HfO_2 to the lower interface and possibly leading to smaller dipole concentration. In an open structure like that of SiO_2 (tetrahedral network), the lanthanide atoms can more easily reach the interface. The $Hf_{0.4}Si_{0.6}O_z$ dielectric has an intermediate density between SiO_2 and HfO_2, resulting in intermediate V_{FB} shift. The inset of Fig. 5 also shows that the maximum temperature reached by the device causes a big V_{FB} shift. In fact, the absolute value of the shift follows an Arrhenius behavior indicating a thermally activated process, most likely diffusion of the lanthanide atoms. Quantitatively, the absolute value of V_{FB} shift relative to samples without Gd_2O_3 is given by $\Delta V_{FB}=a\exp(-Q^*10^3/kT)$, with a equal to 1005 mV and $Q=0.13$ eV, a relatively small activation energy. The evidence for this thermally activated process could also be seen in the work of Kirsch *et al.*[11] where they proposed the dipole model. They found that Sr produced the largest amount of V_{FB} shift while Sc produced the smallest amount of the V_{FB} shift.[11] While this difference was largely attributed to electronegativity differences, it is interesting to note that the melting point of Sr is 795 °C while that of Sc is 1539 °C, which in our judgment was a key reason for the large difference in V_{FB} shift reported, as more significant diffusion and accumulation of Sr occurred at the lower interface. This likely resulted in higher dipole concentration at the interface in the case of Sr.

The model of Lin *et al.*[13] suggests that the V_{FB} shift relates to the work function of the metal in the metal-oxide capping layer and predicts that capping layers which produce large discontinuity in the dielectric constant will produce the maximum V_{FB} shifts. Since the dielectric constant difference ($\Delta\varepsilon_r$) between Gd_2O_3 (capping layer in our samples) and the underlying gate dielectric increases with $\%SiO_2$ in the gate dielectric, the model seems to be consistent with the observation that the V_{FB} shifts increase with $\%SiO_2$ in gate dielectric. Assuming a dielectric constant of 22, 25, 14, and 4 for Gd_2O_3, HfO_2, $Hf_{0.4}Si_{0.6}O_z$, and SiO_2, respectively, we calculate that the measured V_{FB} shifts are linearly related to $\Delta\varepsilon_r$, where $\Delta V_{FB}(\text{mV})=-1.84+20.5\Delta\varepsilon_r$, and are consistent with Lin's prediction. However, it is not clear how the temperature dependence of the V_{FB} shift (Fig. 5 inset) can be explained by Lin's model. At higher temperature, the diffusion of Gd, which was confirmed by the EELS spectra, should actually reduce $\Delta\varepsilon_r$, and the V_{FB} shifts should therefore become smaller, not larger, as experimentally observed.

In conclusion, we have demonstrated that the V_{FB} shift in Gd_2O_3 capped gate stacks depends on the composition of the underlying gate dielectric and the thermal budget of the process. The V_{FB} shift appears to be related to the diffusion of the Gd toward the interface, although the Gd_2O_3 layer is not consumed. We believe that the interfacial dipole model can explain these results, but it must be modified to explain that the extent of the V_{FB} shift is not only controlled by the theoretical dipole moment at the interface, but also by the diffusion rate of the lanthanide element.

[1]H. N. Alshareef, M. A. Quevedo, H. C. Wen, R. Harris, P. Kirsch, P. Majhi, B. H. Lee, R. Jammy, D. J. Lichtenwalner, J. S. Jur, and A. I. Kingon, Appl. Phys. Lett. **89**, 232103 (2006).
[2]M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, and A. M. Sergent, Science **283**, 1897 (1999).
[3]M. Passlack, N. Medendorp, R. Gregory, and D. Braddock, Appl. Phys. Lett. **83**, 5262 (2003).
[4]J. R. Hauser, CVS©2000, NCSU Software, Version 5.0, Department of Electrical and Computer Engineering, NC State University, Raleigh, NC.
[5]D. J. Lichtenwalner, J. S. Jur, A. I. Kingon, M. P. Agustin, Y. Yang, S. Stemmer, L. V. Goncharova, T. Gustafsson, and E. Garfunkel, J. Appl. Phys. **98**, 024314 (2005).
[6]M. Copel, E. Cartier, V. Narayanan, M. C. Reuter, S. Guha, and N. Bojarczuk, Appl. Phys. Lett. **81**, 4227 (2002).
[7]S. Stemmer, J.-P. Maria, and A. I. Kingon, Appl. Phys. Lett. **79**, 102 (2001).
[8]M. Copel, S. Guha, N. Bojarczuk, E. Cartier, V. Narayanan, and V. Paruchuri, Appl. Phys. Lett. **95**, 212903 (2009).
[9]*Lange's Handbook of Chemistry*, 15th ed., edited by J. A. Dean (McGraw-Hill, New York, 1999), p. 81.
[10]S. Guha, V. K. Paruchuri, M. Copel, V. Narayanan, Y. Y. Wang, P. E. Batson, N. A. Bojarczuk, B. Linder, and B. Doris, Appl. Phys. Lett. **90**, 092902 (2007).
[11]P. D. Kirsch, P. Sivasubramani, J. Huang, C. D. Young, M. A. Quevedo-Lopez, H. C. Wen, H. Alshareef, K. Choi, C. S. Park, K. Freeman, M. M. Hussain, G. Bersuker, H. R. Harris, P. Majhi, R. Choi, P. Lysaght, B. H. Lee, H.-H. Tseng, R. Jammy, B. Boscke, D. J. Lichtenwalner, J. S. Jur, and A. I. Kingon, Appl. Phys. Lett. **92**, 092901 (2008).
[12]K. Kakushima, K. Okamoto, M. Adachi, K. Tachi, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, Solid-State Electron. **52**, 1280 (2008).
[13]L. Lin and J. Robertson, Microelectron. Eng. **86**, 1743 (2009).
[14]H. J. Li and M. I. Gardner, IEEE Electron Device Lett. **26**, 441 (2005).
[15]B. P. Linder, V. Narayanan, V. K. Paruchuri, E. Cartier, and S. Kanakasabapathy, Technical Digest SSDM, Tsukuba, 2007, p. 16.