Potential of carbon nanotube field effect transistors for analogue circuits

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Abstract: This Letter presents a detailed comparison of carbon nanotube field effect transistors (CNFETs) and metal oxide semiconductor field effect transistors (MOSFETs) with special focus on carbon nanotube FET's potential for implementing analogue circuits in the mm-wave and sub-terahertz range. The latest CNFET lithographic dimensions place it at-par with complementary metal oxide semiconductor in terms of current handling capability, whereas the forecasted improvement in the lithography enables the CNFETs to handle more than twice the current of MOSFETs. The comparison of RF parameters shows superior performance of CNFETs with a g_m, f_T and f_{max} of 2.7, 2.6 and 4.5 times higher, respectively. MOSFET- and CNFET-based inverter, three-stage ring oscillator and LC oscillator have been designed and compared as well. The CNFET-based inverters are found to be ten times faster, the ring oscillator demonstrates three times higher oscillation frequency and CNFET-based LC oscillator also shows improved performance than its MOSFET counterpart.

1 Introduction

The exponential growth of transistors in integrated circuits as described by the Moore's law has continued for almost half a century. However, the 2010 International Technology Roadmap for Semiconductors (ITRSs) predicts the growth to slow down by the end of 2013 [1]. This is primarily because the scaling of complementary metal oxide semiconductor (CMOS) is fast approaching its physical limits and presents many obstacles such as higher sub-threshold conduction, increased gate oxide and junction leakage, lower output resistance and transconductance and increased heat production [2]. This has led semiconductor industry to explore different materials and devices and more-than-Moore technologies (as coined by ITRS). Among the materials and devices investigated, carbon nanotube field effect transistors (CNFETs) have gained special interest because of their small size, high mobility, near-ballistic transport, large current density and lower intrinsic capacitances [3–6].

Since the introduction of CNFETs, the research has been mainly focused towards their use in digital circuits [7–12]. In [12], even medium scale thin film carbon nanotube (CNT) integrated circuits have been reported on flexible plastic substrates. However, the on/off ratio (also called the noise margin) is typically very small for the currently manufactured CNFETs because of the existence of metallic CNTs [13], thus requiring more investigation on their usage for digital circuits. In contrast, CNFETs have more potential for high-performance analogue circuits, where the transistors do not need to be fully turned off. Moreover, the characteristic performance metrics for analogue or RF transistors are more suited to the materials and device properties of CNTs and the manufacturing tolerances can also be more relaxed [14].

In comparison with digital devices and circuits, fewer RF circuits based on CNFETs have been reported. In [15], a 100 KHz CNT-based, amplitude-modulated demodulator has been demonstrated whereas a 500 MHz CNT transistor oscillator has been reported in [16]. Similarly, [17] reports an RF mixer mixing at 50 GHz using a single-walled (SW) CNT transistor. References [18, 19] provide a quantitative measure of RF performance of array-based CNFETs; however, the analysis is limited to the transistor level. Most of the above works, firstly, do not reflect the true RF potential of the CNFETs, and secondly do not provide a detailed improvement comparison over CMOS circuits so that the CNFET results can be put into perspective, especially at high frequencies.

In this Letter, a detailed performance comparison of metal oxide semiconductor field effect transistors (MOSFETs) and CNFETs for RF circuits is presented. As the fabrication of CNFETs and its circuits is an emerging and extremely challenging area, most of the published work, except for a few basic fabricated devices [15–17], is either analytical or simulation based. In this work, a 32 nm CMOS predictive model from Arizona State University [20] and an HSpice (v.2.2.1) CNFET model from Stanford University have been used [13, 21, 22].

The Letter is organised as follows: Section 2 describes the types and structure of CNFETs. Section 3 deals with the current–voltage (*I–V*) curves and characterises the relation of CNFET current with different parameters such as number of tubes, pitch and transistor width. The comparison of RF figures-of-merit (FOMs) of MOSFETs and CNFETs is presented in Section 4. The device speed and delay of an inverter, ring oscillator and LC oscillator performance are compared in Section 5 and conclusions are drawn in Section 6.

2 CNFET basics

To compare CNFET performance with MOSFETs, it is important to understand the similarities and differences in their structures which are discussed below.

2.1 Structure of MOSFETs and MOSFET-like CNFETs

Fig. 1 depicts the structure of MOSFET and MOSFET-like CNFET. In a conventional MOSFET, the source and drain regions are formed by two heavily doped regions in a silicon substrate and the gate is formed by poly-silicon material, which is insulated from the substrate by a thin layer of silicon dioxide. If a voltage is applied to the gate terminal, a continuous channel underneath the gate is formed for current flow between the source and drain. On the other hand for CNFETs, the gate, source and drain contacts are made of metals like Chrome or Tungsten with a work function of 4.5 eV. H_g is the height of the metal contacts and L_g is the gate length as shown in Fig. 1*b*. It is worth mentioning that out of the two types of CNFETs namely Schottky barrier and MOSFET like, the latter is chosen as it has higher I_{ON}/I_{OFF} ratio,

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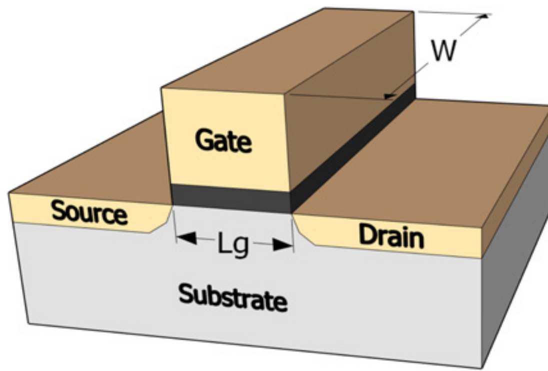
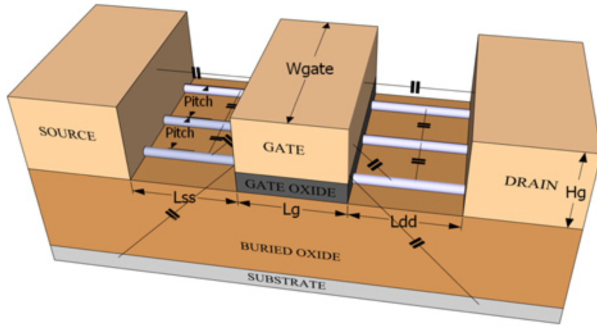


a



b

Fig. 1 *Structure*
a MOSFET
b MOSFET-like CNFET

transconductance (g_m), transition frequency f_T, lower parasitic capacitances, better AC performance and higher fabrication feasibility [18]. In the MOSTFET-like CNFET (henceforth, called just CNFET), the current flow between the source and drain contacts is achieved using CNTs. These CNTs can be pictured as folded graphene sheets into a tubular structure and can be single-walled or multi-walled depending on the number of shells that form the tubular structure. The SWCNTs are usually characterised by its chirality which determines its properties and diameter. The chirality is represented by a pair of indices (n_1, n_2) called the chirality vector which is (19, 0) for the CNFET model chosen in this work. The tubes under the gate are un-doped, whereas the tubes connecting the gate to source and drain are heavily doped, and hence the doped tubes are referred to as source–drain extension regions. The gate, along with the source–drain extension region excluding the source and drain metal contacts, is considered as intrinsic structure of the CNFET. The introduction of source and drain metal contacts adds the parasitics or extrinsic capacitances, hence, completing the device model of the CNFET. The distance between the centres of two adjacent tubes is called the pitch. The gate oxide with a dielectric constant of 16 (e.g. hafnium oxide) has a height of roughly 4 nm. The tubes are sitting on a thick silicon oxide (10 µm) with a silicon substrate at the bottom [21]. The default values of the device parameters are mentioned in Table 1.

The structures of MOSFETs and CNFETs look similar, but have some differences. The main difference is that the MOSFET channel is continuous along the transistor width which is not the case in CNFETs. Instead, there is an array of CNTs that facilitate the electron transport. This poses some challenges for fair comparison of their performances. For instance, the width in CNFETs does not have the same meaning as the width in MOSFETs. In MOSFETs, the DC drain current rises by increasing the transistor width, whereas in CNFETs the drain current only rises by either increasing the number or the diameter of CNTs. The pitch, on the other hands, does not affect the drain current unless the tubes are very close

Table 1 Default values of the device parameters

Parameters	Descriptions	Default values
L_g	gate channel length	32 nm
L_{ss}/L_{dd}	the length of the doped CNT source/drain extension region	32 nm
H_g	height of the metal contacts	64 nm
W_{gate}	width of the metal gate contact	variable
pitch	the distance between the centre of two adjacent tubes under the same gate	20 and 5 nm
tubes	the number of tubes in the device	variable
(n_1, n_2)	the chirality of tube	(19, 0)
D	diameter of the tubes	1.5 nm

(<20 nm apart) because of the screening effect, which will be explained later. Furthermore, the metal gate width (W_{gate}) of the CNFETs is only seen to affect the parasitic capacitances. Therefore, W_{gate} is a parameter used to show the extrinsic performance of a CNFET and is not an exact counterpart for the channel width in MOSFETs.

For the SWCNTs with a chirality vector (n_1, n_2), the diameter is given by Deng and Wong [21]

$$D_{CNT} = \frac{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \quad (1)$$

where 'a' is the lattice constant for the carbon atom and has a value of 2.49 A. If the difference between n_1 and n_2 is divisible by 3, the tubes are metallic, otherwise non-metallic. Thus, in this work the chirality vector of (19, 0) makes the tubes non-metallic and the diameter of the CNTs from (1) is about 1.5 nm. It is evident, that the chirality has to be changed in order to change the diameter of the CNTs. If the tubes with a given diameter are placed at an equal distance from each other, the width of a CNFET could be expressed by the pitch and number of tubes. It is important to note that if the number of tubes is fixed and the pitch is >20 nm, then the change in pitch does not affect the DC current. However, when the number of tubes is not fixed, then for a given width, the pitch is an important parameter describing the density of the tubes. For example, 20 and 5 nm pitches are equivalent to a tube density (number of tubes/µm) of 50 nanotubes/µm and 200 nanotubes/µm for a 1 µm transistor, respectively. Thus, it must be noted that just mentioning the diameter and the width of the CNFET is not enough to characterise the transistor, the pitch information also needs to be included to describe the density of the CNTs. In this work, a width of 1 µm with pitches of 5 nm and 20 nm is chosen as default values unless stated otherwise. This is because 20–25 nm pitches have been reported in some earlier works [23], whereas the 5 nm pitch projects a future nanotube density when lithographic techniques become advanced enough to support it.

The 32 nm technology node is chosen for comparison because for the lower 16 nm node, the CNFET HSpice model approaches its limitation of 10 nm, as according to Deng and Wong [13], a sub-10 nm regime is not supported because of the complex quantum mechanisms. All simulations are performed using HSpice and CScope that are used for visualising the results.

3 Transistor DC characterisation

This section presents the DC performance of CNFETs with its various parameters and also compares the I–V curves with its MOSFET counterpart.

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3.1 *Drain current against pitch, number of CNTs and transistor width*

The effect of pitch on the drain current of CNFETs is first observed. A supply voltage of 1 V is connected to both drain and gate terminals, whereas source and substrate terminals are grounded.

Fig. 2 plots the CNFET drain current against pitch for a fixed number of tubes. It can be seen that the drain current is independent of pitch unless the tubes are very close. However, when the pitch is <20 nm, the inter-CNT capacitance becomes more prominent and the drain current reduces because of the screening effect. The screening effect is defined as the change in the electrostatic fields and the Coulomb potentials of charged particles because of the presence of other charges in its vicinity [21]. Therefore, because of the electrostatic repulsion between the tubes at lower pitches, the electrons are repelled away from the centre of the tube, resulting in the reduction of the current. Fig. 2 also includes the results from [21] for validation.

Fig. 3 shows the relation between CNFET drain current and the number of tubes for two different pitches while the transistor width is not fixed. It is evident that the current increases linearly with the number of tubes; however, as the screening effect is more prominent at 5 nm pitch, the current per CNT is less as compared with 20 nm pitch.

As a next step, we aim to compare the current handling of CNFETs and MOSFETs at different widths (Fig. 4). Since the CNT diameter is fixed (1.5 nm), transistor width in case of CNFETs is equal to the product of number of CNTs and pitch. As the tube density is controlled by selecting the pitch, thus the width is increased by increasing the number of CNTs. Two pitch values of 20 and 5 nm are selected. As we are comparing the drain current at a certain width and the two values of the pitches,

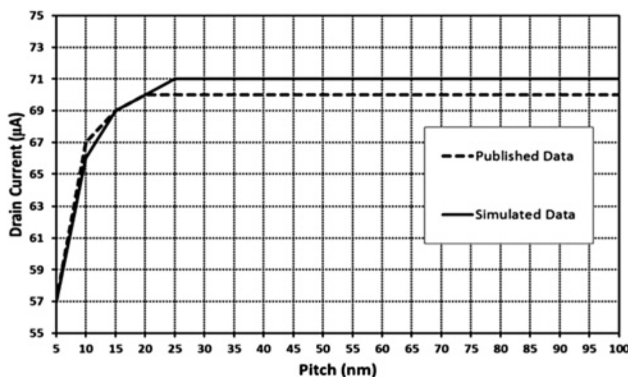

Fig. 2 *Drain current against pitch for three CNTs*
Simulation results validated with published results [21]

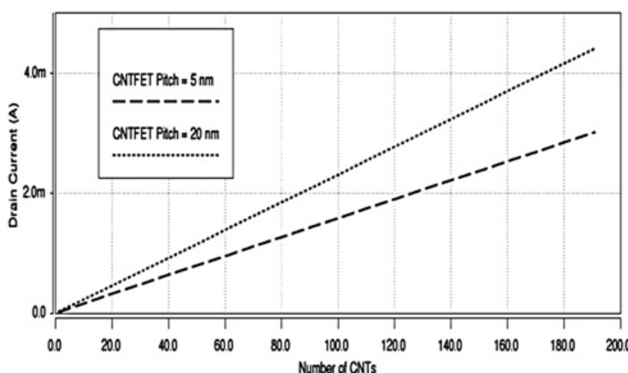

Fig. 3 *Drain current against number of CNTs at 20 and 5 nm pitches for CNFETs while the width is not fixed*

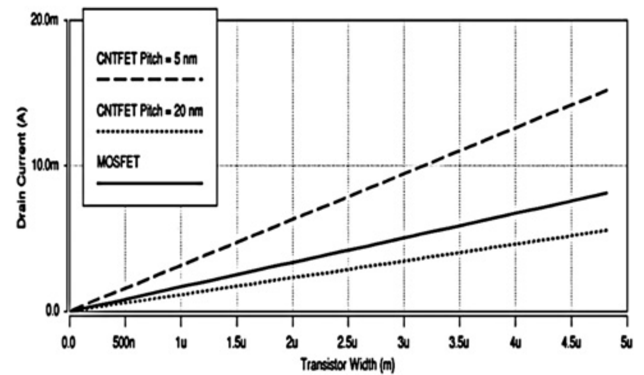

Fig. 4 *Drain current against transistor width for MOSFET and CNFETs for two different pitches*
CNFET width is increased by increasing the number of tubes

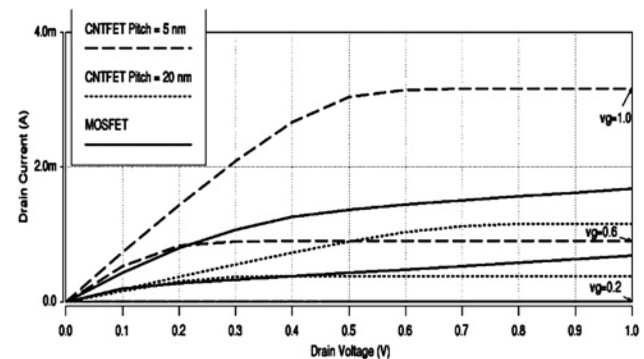

Fig. 5 *Drain current against drain voltage for gate voltages of 0.2, 0.6 and 1 V*

the number of tubes can no longer be the same. For instance, for moving from a width of 1 to 2 µm, the number of tubes increases from 200 to 400 for 5 nm pitch and from 50 to 100 tubes for 20 nm pitch. Thus, there is higher drain current at 5 nm, because the tube density is much higher than 20 nm pitch. It is worth noting that for a certain width, say 2 µm, MOSFET has more drain current than the CNFET with 20 nm pitch. However, when the pitch is decreased to 5 nm, which in turn increases the tube density, CNFET outperforms the MOSFET. Thus, it is important to improve the lithographic techniques for CNFETs to exploit their true potential. Moreover, it is interesting to note that even though the current per tube is less at 5 nm pitch as compared with 20 nm pitch, the overall drain current increases at 5 nm pitch because more CNTs can fit-in the same width.

3.2 *Drain current against drain voltage (at sweeping gate voltage)*

Fig. 5 shows the typical drain current against drain voltage ($I_D - V_D$) plots for MOSFET and CNFETs for different gate voltages (V_G). The gate voltage values are 0.2, 0.6 and 1 V and width of the transistors is 1 µm. Again, in comparison with a 20 nm pitch CNFET, MOSFET can provide higher currents. However, at 5 nm pitch, the drain current of CNFET becomes twice as compared with MOSFETs. It is also evident that the almost zero slopes in the saturation region for the CNFETs bode well for their use as current sources.

4 RF characterisation

This section presents the RF performance comparison between MOSFETs and CNFETs.

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4.1 *Transconductance, g_m*

Transconductance (g_m) is a measure of change in drain current of a transistor for variation in gate voltages. It is an important benchmarking parameter especially for analogue circuits such as amplifiers, because it represents gain and amplification of an FET. Furthermore, other RF FOMs, such as transition frequency, are related to g_m. Generally, g_m is given by

$$g_m = \frac{\Delta I_D}{\Delta V_G} \quad (2)$$

where I_D and V_G are the drain current and gate voltage, respectively.

The transconductances of MOSFET and CNFET for two different pitches are shown in Fig. 6. The drain voltage is 1 V and the comparison is done at 1 μm gate width. At a pitch of 20 nm, the MOSFET g_m is comparable with CNFET. However, for a reduced pitch of 5 nm, the CNFET g_m is considerably higher than the MOSFET g_m. At a gate voltage of 1 V, the CNFET has 2.7 times the g_m of MOSFET. The better g_m of CNFET at 5 nm pitch is because of higher drain current which is consistent with Section 3. The maximum g_m values are tabulated in Table 2.

4.2 *Transition or unity current gain cut-off frequency, f_T*

Transition frequency or unity current gain cut-off frequency (f_T), is a measure of the intrinsic speed of a transistor and is often used as a benchmarking parameter between different transistors. Fig. 7 shows f_T values as a function of gate voltage for both intrinsic and extrinsic CNFETs. With the drain voltage set to 1 V, the f_T for the intrinsic CNFET is about 1.2 THz, whereas the extrinsic, that includes the effect of parasitic capacitances, exhibits a f_T of 900 GHz which is much higher than the MOSFET f_T of 340 GHz (Fig. 8). The main reason for higher f_T of CNFETs is attributed to 2–3 times lower parasitic capacitances in comparison with MOSFETs as reported in [13, 21, 22]. The above CNFET f_T values indicate a high potential for their use in millimetre and sub-terahertz frequency bands.

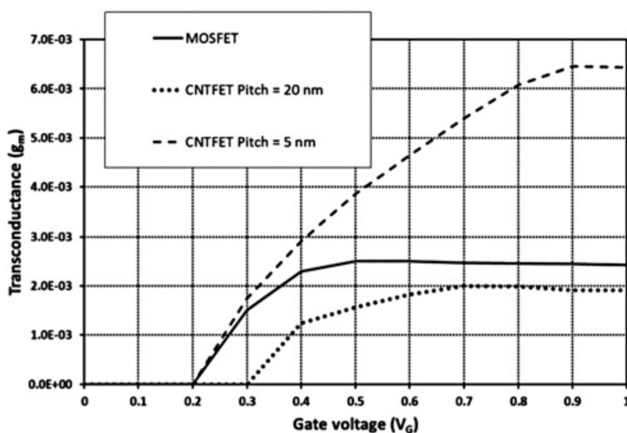

Fig. 6 *Transconductance against gate voltage for MOSFET and CNFETs with 20 and 5 nm pitches while the width is fixed at 1 μm*

Table 2 Comparison of the transconductance values

Transistors	Maximum transconductances
MOSFET	2.44 mS
CNFET (pitch = 20 nm)	1.91 mS
CNFET (pitch = 5 nm)	6.46 mS

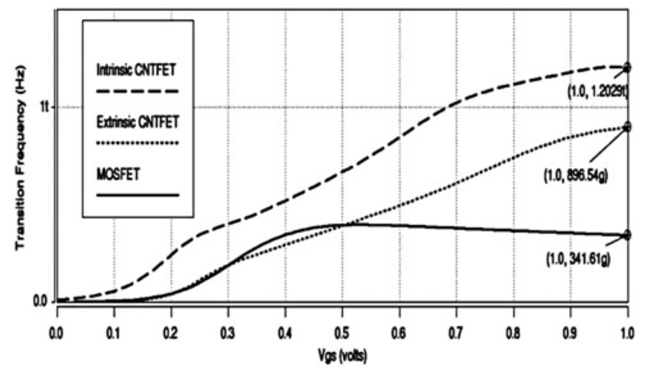

Fig. 7 *Unity current gain cut-off frequency against gate voltage for MOSFET, intrinsic CNFET and extrinsic CNFET*

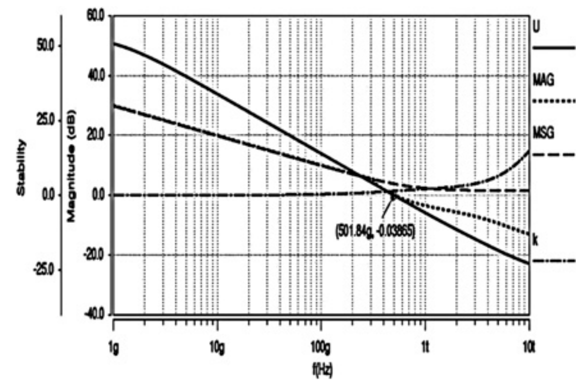

Fig. 8 *Unilateral power gain (U), MSG, MAG and Karokawa stability factor (k) against frequency for MOSFET*

A second method, using the current gain of the transistor, has also been utilised to verify the f_T values obtained in Fig. 7. The generalised current gain of a two-port liner network is given by

$$|h_{21}| = \left|\frac{i_2}{i_1}\right| = \left|\frac{y_{21}}{y_{11}}\right| \quad (3)$$

Using the y-parameters, the current gain h_{21} has been analysed against frequency both for MOSFET and CNFETs (both intrinsic and extrinsic). The frequency at which the current gain falls to zero dBs is termed as the transition frequency, f_T. Table 3 compares the f_T values obtained using the above-mentioned two methods showing a good agreement.

4.3 *More RF FOMs: F_{max}, maximum available gain (MAG), maximum stable gain (MSG) and k*

This sub-section presents the other well-known RF FOMs. These include Mason's unilateral power gain (U), MAG, MSG, Kurokawa stability factor (k) and maximum oscillation frequency (f_{max}). These RF parameters have been derived by two-port linear network analysis using y-parameters. The stability is determined by k (known as the Rollet's factor) and Δ. In terms of y-parameters, k is given by Gupta [24]

$$k = \frac{2\text{Re}(y_{11})\text{Re}(y_{22}) - \text{Re}(y_{12}y_{21})}{|y_{12}y_{21}|} \quad (4)$$

The transistor is considered to be conditionally stable when k is <1 and unconditionally stable when greater or equal to 1. Δ which is the second condition for stability is defined as the determinant of the scattering matrix ($\boldsymbol{S}_{11}\boldsymbol{S}_{22} - \boldsymbol{S}_{12}\boldsymbol{S}_{21}$) and its magnitude

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Table 3 Transition frequency (F_T) using two methods

	f_T (method 1)	f_T (method 2)
MOSFET	340 GHz	324 GHz
CNFET (intrinsic)	1.2 THz	1.1 THz
CNFET (extrinsic)	900 GHz	892 GHz

has to be <1 for a device to be unconditionally stable [24]. MSG is the available gain when the device is conditionally stable and MAG is the available gain when it is unconditionally stable. When $k < 1$, MAG is infinite which means the device is oscillating. Comparing the MSG, MAG and k curves in Figs. 8 and 9, it becomes clear that CNFETs are more stable at higher frequencies as compared with MOSFETs. As evident from their definitions, MAG and MSG are dependent on the stability of the device, whereas the power gain (U) is defined regardless of whether the device is active or passive, conditionally stable or unconditionally stable [24]. Analytically, U represents the gain of a two-port network having no output-to-input feedback and with the input and output conjugates matched to the signal source and load, respectively. It is given by Gupta [24]

$$U = \frac{|y_{21} - y_{12}|^2}{4[\mathrm{Re}(y_{11})\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12})\mathrm{Re}(y_{21})]} \tag{5}$$

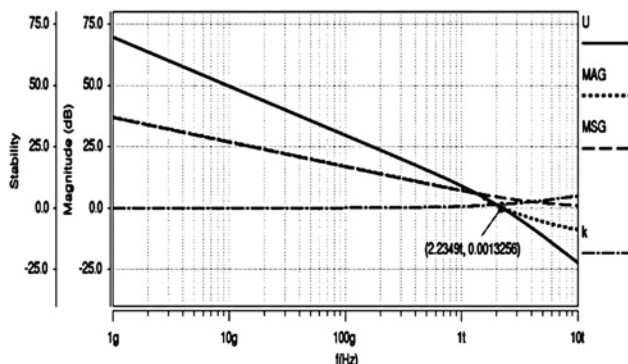

Fig. 9 *Unilateral power gain (U), MSG, MAG and Karokawa stability factor (k) against frequency for CNFET*

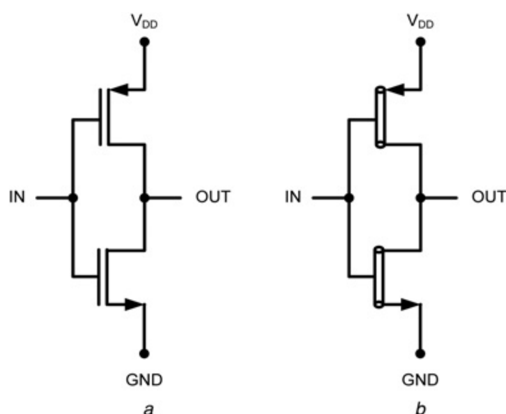

Fig. 10 *A basic inverter stage using*
a MOSFETs
b CNFETs, the gate is represented as a tube to differentiate from MOSFET

Although the simulations in this work are carried at a different technology node in comparison with [19], but the trends in Figs. 8 and 9 still match to its published RF FOMs.

To evaluate the power gain of two active devices, a comparison of their U values over the entire frequency of interest is required. However, it is more convenient to have a single-number benchmark. Such a practical FOM derived from the power gain is called $f_{\max}$, the frequency at which the magnitude of U becomes zero decibels. It is the frequency above which power gain cannot be obtained from an active device. At $f_{\max}$, the magnitude of MSG and MAG also becomes 0 dB [24]. Figs. 8 and 9 show an $f_{\max}$ of 500 GHz for MOSFET and 2.24 THz for CNFET. Owing to the significantly higher f_T and $f_{\max}$, CNFETs have major advantage over MOSFETs for RF circuits. The comparison is summarised in Table 4.

5 RF circuits comparison

To demonstrate the feasibility and superiority of CNFET-based RF circuits, the performance of an inverter, a three-stage ring oscillator and LC oscillator using MOSFETs and CNFETs are compared.

5.1 *Inverter delay*

Inverters are basic building blocks of many integrated circuits (Fig. 10). For instance, a ring oscillator operating at RF frequencies is composed of few inverter stages cascaded together and the combined delay of the series of inverters determines the oscillation frequency of the ring oscillator. This sub-section compares the unloaded inverter delay between MOSFETs and CNFETs. For consistency, the channel width is chosen to be 1 μm for both p-FETs and n-FETs. Since the CNFETs have lower parasitic capacitances as compared with the MOSFETs [13], the device is much faster. Moreover, when the tube density is increased by reducing the pitch, the on-current increases (as shown in Section 3) because of increase in effective width of the transistor. As a consequence, at a pitch of 5 nm, the inverter using CNFETs is roughly ten times faster than the MOSFETs-based inverter, whereas at a pitch of 20 nm the CNFET-based inverter is 3.5 times faster than the MOSFET counterpart. This is summarised in Table 5.

5.2 *Ring oscillator*

Ring oscillator is an integral part of phase locked loops (PLLs) in high frequency transceivers. In this sub-section, it is used as a bench-marking circuit between MOSFET and CNFETs, specifically comparing the oscillation frequency and power consumption of a three-stage ring oscillator. As clear from Fig. 11, three inverter stages are cascaded together to realise a three-stage ring oscillator. The drain voltage and transistor width are 1 V and 1 μm, respectively. Since, the delay of individual inverter is lesser for CNFETs, the

Table 4 Comparison of f_T and $f_{\max}$

Transistors	f_T	$f_{\max}$
MOSFET	341 GHz	500 GHz
CNFET (intrinsic)	1.2 THz	2.23 THz
CNFET (extrinsic)	896 GHz	2.23 THz

Table 5 Comparison of the inverter delay

Inverters	Inverter delays	Comparative speeds
MOSFET	1.45 ps	×
CNFET pitch = 20 nm	425 fs	3.4×
CNFET pitch = 5 nm	140 fs	10.35×

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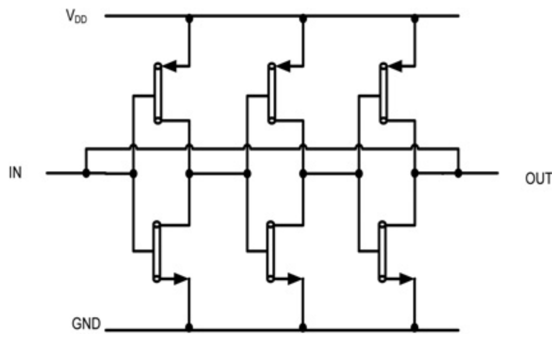

Fig. 11 *Three-stage ring oscillator using CNFETs*

ring oscillator based on CNFETs has a much higher oscillation frequency. Moreover, as the inverter delay is the least for CNFET at 5 nm pitch, the oscillation frequency of 171 GHz is the highest among the three cases as shown in Table 6.

However, there is a trade-off between the oscillation frequency and the power consumption of a CNFET-based three-stage ring oscillator. If we compare Figs. 4 and 12, it is evident that the higher power consumption is because of higher drain current at 5 nm pitch and power consumption rises with increasing transistor width. On the other hand, for the oscillator based on 20 nm pitch CNFET, the power consumption is slightly lower than the MOSFET counterpart, but the oscillation frequency is 2.5 times higher.

5.3 LC oscillator

A typical LC oscillator (Fig. 13) consists of an inductor and capacitor forming a tank circuit and a negative-g_m cell, which compensates the losses of the tank for achieving sustained oscillation. LC-based oscillators, specially, voltage controlled oscillators are widely used in millimetre wave RF circuits to generate local oscillator signals for PLLs.

The oscillation frequency $\left(f_{\rm OSC} = 1/2\pi\sqrt{LC}\right)$ depends primarily on the total values of inductance and capacitance in the circuit. The latter not only includes the contribution from the tank, but also from the parasitic capacitances of FETs. For comparison of MOSFET- and CNFET-based LC oscillators, typical values of 50 pH for tank inductance, 40 fF for tank capacitance and 1 µm wide transistors are used. Table 7 shows the oscillation frequency, output amplitude and parasitic capacitance of oscillators. In comparison with MOSFET-based oscillator, it can be seen that the lower parasitic capacitance for CNFETs results in a higher $f_{\rm OSC}$. The oscillator based on 20 nm pitch CNFETs demonstrate the lowest parasitic capacitance, hence the highest $f_{\rm OSC}$. In addition, as the FET capacitance is higher at 5 nm pitch because of increased inter-tube capacitance, its $f_{\rm OSC}$ is slightly lower than the 20 nm pitch CNFET oscillator.

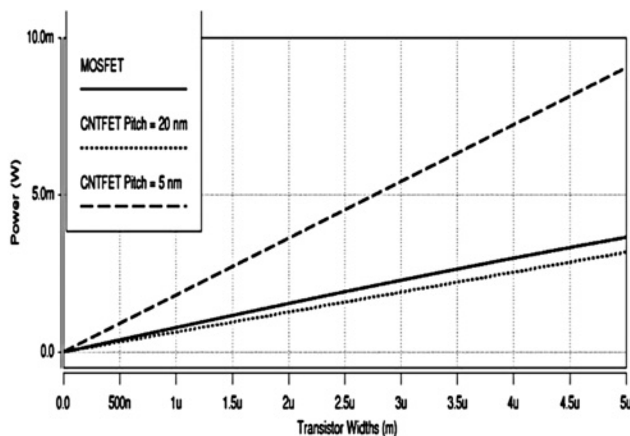

Fig. 12 *Power consumption against transistor width for three-stage ring oscillator*

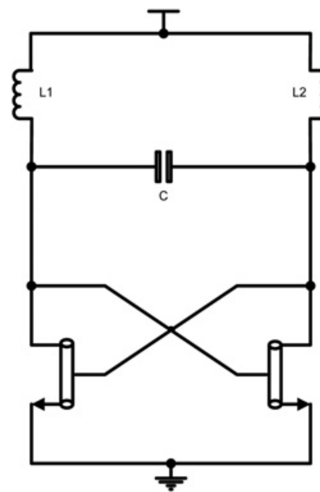

Fig. 13 *LC oscillator using CNFETs*

Table 6 Comparison of the oscillation frequency

Ring oscillators (W = 1 µm)	Oscillation frequencies
MOSFET based	58.39 GHz
CNFET-based pitch = 20 nm	140.64 GHz
CNFET-based pitch = 5 nm	170.96 GHz

Table 7 Comparison of the LC oscillator performance

L = 50 pH C = 40 fF LC oscillators	Oscillation frequencies, GHz	Differential peak-to-peak voltages, V	FET parasitic capacitances, fF
MOSFET based	109.6	4.4	2.19
CNFET-based pitch = 20 nm	111.2	4.3	0.96
CNFET-based pitch = 5 nm	110.5	4.7	1.50

6 Conclusion

The performance of CNFETs has been compared with MOSFETs for typical RF circuits and the obtained results reflect their immense potential. For a given width and a pitch of 20 nm, CNFETs have slightly less current carrying capability as compared with MOSFETs. However, when the tube density is increased by reducing the pitch to 5 nm, CNFETs demonstrate twice the current capability to that of MOSFETs. Therefore the improvement of lithographic techniques is crucial to tap into the full potential of the CNFETs. The comparison of RF parameters of MOSFETs and CNFETs reveals superior performance of the latter with a g_m, $f_{\rm T}$ and $f_{\rm max}$ 2.7, 2.6 and 4.5 times higher, respectively. The CNFET-based inverter is up to ten times faster, ring oscillator has three times higher oscillation frequency and CNFET-based LC oscillator offers two times lesser parasitic capacitance than its MOSFET counterpart.

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