ORIGINAL ARTICLE

Thermoelectricity from wasted heat of integrated circuits

**Hossain Fahad · Md. Hasan · Guodong Li ·
Muhammad Hussain**

Abstract We demonstrate that waste heat from integrated circuits especially computer microprocessors can be recycled as valuable electricity to power up a portion of the circuitry or other important accessories such as on-chip cooling modules, etc. This gives a positive spin to a negative effect of ever increasing heat dissipation associated with increased power consumption aligned with shrinking down trend of transistor dimension. This concept can also be used as an important vehicle for self-powered systems-on-chip. We provide theoretical analysis supported by simulation data followed by experimental verification of on-chip thermoelectricity generation from dissipated (otherwise wasted) heat of a microprocessor.

Keywords Thermoelectricity · Wasted heat ·
Microprocessor · Self-powered · Systems-on-chip

To meet the consumer demand for high performance computation, scaling of transistors (the basic building block of any integrated chip) is continuing at a fast pace. This trend results in higher integration density of around 850 million transistors in a latest microprocessor of few square centimeters size. But as a negative consequence increased power dissipation specifically from leakage current is rising at a level which causes alarming power densities, increased heat dissipation and higher chip temperatures which will obstruct reliable operation of the

H. Fahad · Md. Hasan · G. Li · M. Hussain (✉)
Integrated Nanotechnology Lab, Electrical Engineering,
Physical Science and Engineering, King Abdullah University
of Science and Technology, Thuwal, Mecca 23955-6900,
Saudi Arabia
e-mail: Muhammad.hussain@kaust.edu.sa

chips. When the circuit densities are projected to reach the gigascale as the smallest transistor size approaches 10 nm, chip-level power densities are currently on the order of 100 W/cm^2. This trend is certain to continue which will quickly drain batteries in portable devices and may render many electronic systems unusable without significant advances in cooling technology, or without fundamental shifts in design (Pop et al. 2006). The situation is compounded by millimeter-scale hot spots on the chip, i.e., localized regions of higher heat generation rate per unit area and hence higher temperatures (e.g., near the clock) (Borkar 2001). Thermoelectric devices can address these limitations by on-chip cooling, and significant progress has been made in the development of nano-structured thermoelectric materials with enhanced figures-of-merit (Majumdar 2004; Venkatasubramanian et al. 2001). However, the integration of nano-structured thermoelectric materials with micro-scale devices at a mega scale packaging imposes a significant challenge (Chowdhury et al. 2009). While on-chip cooling is considered as a potential solution, based on the microprocessor surface temperature of at least 65 °C and computer usage at a room temperature (approximately 25 °C) results in a significant temperature difference which can be leveraged by integrating thermoelectric generators in the back plane of a microprocessor to generate considerable amount of electricity to run a portion of the circuitry. Here in this letter, we report theoretical analysis supplemented by simulation results followed by experimental demonstration to support this novel concept.

In a typical thermoelectric device, a junction is formed from two different conducting materials, one containing positive charge carriers (holes) and the other negative charge carriers (electrons). A heat source at the junction causes carriers to move away from the junction, making an electrical generator. Such devices have the advantage of

containing no moving parts, but low efficiencies have limited their use (DiSalvo 1999). Hudak and Amatucci 2008 provide a comparative study of performance in different thermoelectric materials where Bismuth Telluride (BiTe) based thermoelectric devices reportedly have very high conversion efficiency and figure-of-merit (ZT). This material can be fabricated either by two wafer process or in single Si substrate (Rowe 2006). Because of its excellent thermoelectric properties we have used a Bi_2Te_3 based TEG system in our analysis as well as experiment.

To show its feasibility, a p–n thermocouple (Fig. 1) with dimensions comparable to single transistors, is simulated using COMSOL Multi-Physics (Jaegle 2008). The theory on thermoelectric materials is given in (Antonova and Looman 2005).

The heat flow equation and charge continuity equation in thermoelectric materials are given by:

$$\rho C \frac{\partial T}{\partial T} + \nabla . \mathbf{q} = \dot{q} \tag{1}$$

(a)

Top Copper Electrode (5)

n-BiTe (2)

p-BiTe (1)

Si Substrate (3)

Bottom Copper Electrode (4)

Max: 65.0

Min: 27.0
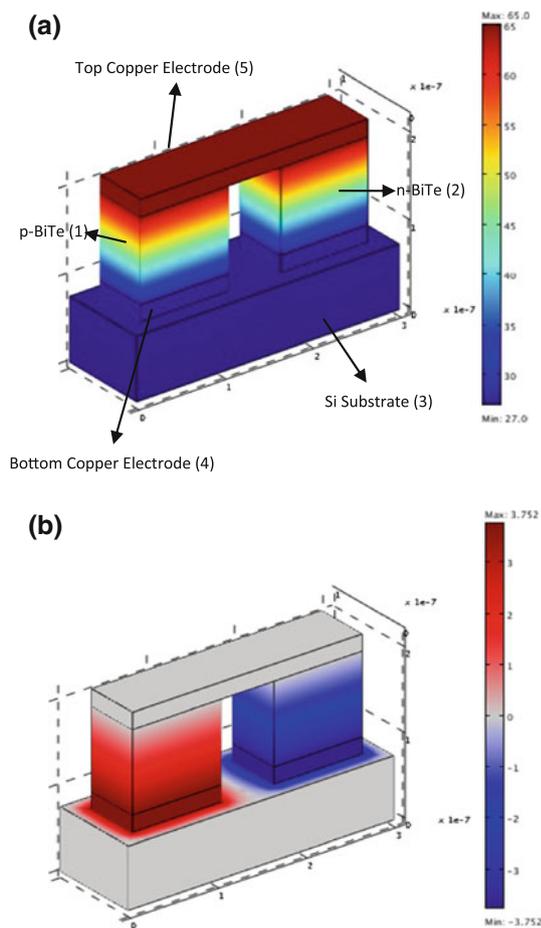
(b)

Max: 3.752

Min: −3.752

Fig. 1 Simulation of TEG system integrated with silicon substrate back plane. **a** Temperature distribution (°C) cold side (bottom of silicon substrate) maintained at 27 °C and hot side (top of copper electrode maintained at 65 °C and **b** Output open circuit voltage (mV)

$$\nabla . \left(\mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \right) = 0 \tag{2}$$

$$\mathbf{E} = -\nabla \varphi \tag{3}$$

These equations are coupled through the following constitutive field equations

$$\mathbf{q} = [\Pi] . \mathbf{J} - [\lambda] . \nabla T \tag{4}$$

$$\mathbf{J} = [\sigma] . (\mathbf{E} - [\sigma] . \nabla T) \tag{5}$$

$$\mathbf{D} = [\varepsilon] . \mathbf{E} \tag{6}$$

The static coupled thermoelectric equations can then be re-written as

$$\nabla . ([\Pi] . \mathbf{J}) - \nabla . ([\lambda] . \nabla T) = \dot{q} \tag{7}$$

$$\nabla . ([\sigma] . [\alpha] . \nabla T) + \nabla . ([\sigma] . \nabla \varphi) = 0 \tag{8}$$

By rearranging (7) and (8) one can solve for the field variables, Temperature (T) and Voltage (V). The rearranged partial differential equations are then given by:

$$-\nabla \left((\sigma \alpha^2 T + \lambda) \nabla T \right) - \nabla \left(\sigma \alpha^2 T \nabla V \right)$$
$$= \sigma \left((\nabla V)^2 + \alpha \nabla T \nabla V \right) \tag{9}$$

$$\nabla (\sigma \alpha \nabla T) + \nabla (\sigma \nabla V) = 0 \tag{10}$$

where,

ρ = density, kg/m^3
C = specific heat capacity, J/(kg K)
T = absolute temperature, K
$\dot{q}$ = heat generation rate per unit volume, W/m^3
$\mathbf{q}$ = heat flux vector, W/m^2
$\mathbf{J}$ = electrical current density vector, A/m^2
$\mathbf{E}$, = electric field intensity vector, V/m
$\mathbf{D}$ = electric flux density vector, C/m^2
$[\lambda]$ = thermal conductivity matrix, W/m K
$[\sigma]$ = electrical conductivity matrix, S/m
$[\alpha]$ = Seebeck coefficient matrix, V/K
$[\Pi] = T[\alpha]$ = Peltier coefficient matrix, V
$[\varepsilon]$ = dielectric permittivity matrix, F/m.

COMSOL allows implementation of (9) and (10) using the partial differential equation (PDE) coefficient form. Using this, a BiTe based p–n thermocouple (Fig. 1) is simulated with the temperature independent material properties listed in Table 1 and dimensions in Table 2 (Jaegle 2008). In Fig. 1, the p and n BiTe legs are contacted at both ends by copper electrodes. The entire structure sits on a silicon substrate, which is electrically grounded except the upper surface in contact with the bottom electrodes. This surface along with all the other surfaces (copper, BiTe) is treated as distributed resistances. The bottom of the Si substrate is maintained at 0 °C while the top copper electrode is subjected to a hot side temperature of 65 °C. The simulated temperature distribution

in the p and n legs is shown in Fig. 1a. The generated open circuit output voltage from this single couple is shown in Fig. 1b, where it can be seen that a maximum voltage of +3.752 mV is at the p-leg bottom copper electrode and a minimum of −3.752 mV is at the n-leg bottom electrode. Keeping the cold side temperature constant at 27 °C, the p–n couple is simulated for hot side temperatures ranging from 65 to 125 °C. These values are typical in CPUs, GPUs at normal to heavy operational loads. The total internal resistance of the device is calculated to be approximately 303 Ω. The output power and the efficiency of the single couple TEG are determined to be 46.53 nW and 0.1152 %, respectively for an input heat flux of 40.4 μW using equations given in (Nextreme thermal solutions 2011).

$$P_{out} = V_{oc}^2/4R \tag{11}$$

$$\eta = P_{out}/Q_{in} \tag{12}$$

where,

P_{out} = Matched output power
V_{oc} = Open circuit output voltage
R = TEG resistance
Q_{in} = Input heat flux.

Figure 2 shows the simulated maximum output power achievable from TEGs containing N number (100–400) of p–n couples at the above specified temperature range.

As an experimental demonstration, we demonstrate that heat dissipated from a Pentium 4 processor operating at 2.4 GHz running on windows XP (Fig. 3a). A commercially available thermoelectric generator with a ZT of 0.72 was used to harvest electricity from the thermal gradient between dissipated heat-induced hot back surface of the processor and the room temperature (Marlow Industries

Inc. 2011). For simplicity and demonstration purposes, this regenerated power was used to drive a circuit consisting of light emitting diodes (LEDs). The maximum output voltage and current that could be harvested has been measured to be 3.729 V and 11.9 mA as seen in Fig. 3b. Up to the best of our knowledge, this is the first demonstration to use wasted heat from a microprocessor using thermoelectric generator (Narasimhan et al. 2009).
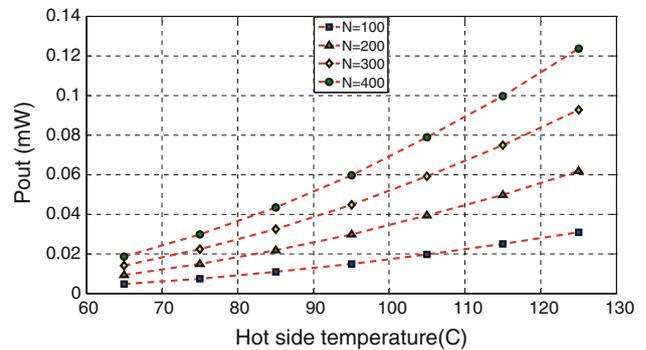

Fig. 2 Calculated maximum output power achievable from TEGs containing N number of p–n couples for different hot side temperatures
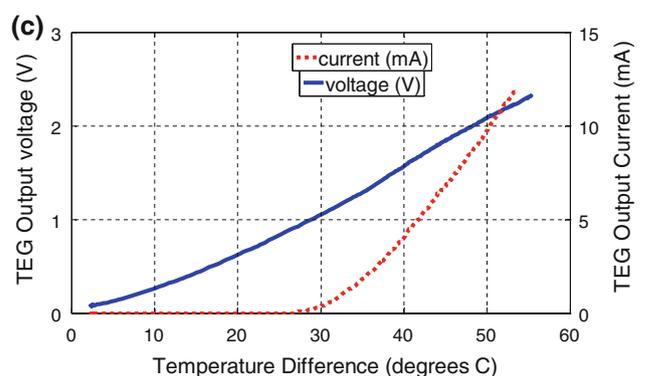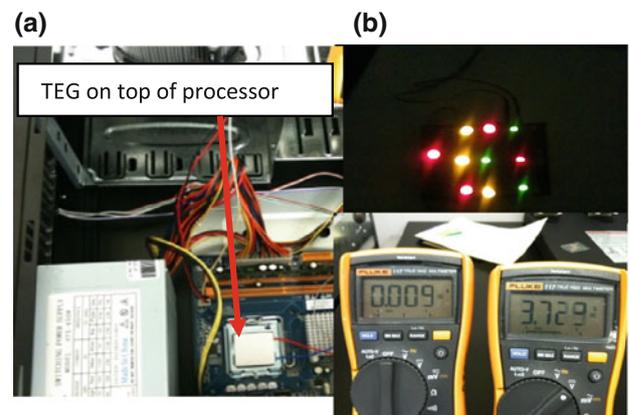

Fig. 3 Experimental setup and I–V plot generated from TEG attached to the back plane of a microprocessor

Table 1 Thermoelectric properties of some known thermoelectric materials

Material	α (V/K)	σ (S/m)	λ (W/m/K)	ρ (kg/m^3)	C (J/kg/K)
n-BiTe	−200e−6	1.1e5	1.6	7,740	154.4
p-BiTe	200e−6	1.1e5	1.6	7,740	154.4
Copper	6.5e−6	5.9e7	400	8,700	385
Silicon	–	1e−12	163	2,330	703

Table 2 Simulated TEG couple dimensions

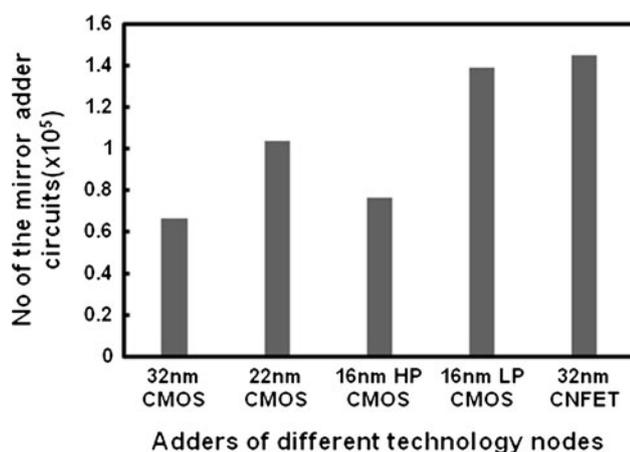| Region	Length (nm)	Width (nm)	Height (nm)
1	100	60	100
2	100	60	100
3	300	100	75
4	100	60	20
5	260	60	20

Fig. 4 Number of mirror adders from various technology nodes that can be run by the electrical power generated from the TEG of different number of cells

In its fullest extent, we envision a portion of the integrated circuit can be run using the generated electricity which will reduce the burden of external power supply. For calculation purpose, we use a full adder which is a very important element in the arithmetic and logic unit of a microprocessor. A conventional mirror full adder is simulated in HSpice for different processes at a clock of 2 GHz. Figure 4 shows the number of mirror adders that can be run by the electrical power generated from the TEG with hot side temperature of 75 °C for different number of cells. Number of adder circuits that can be run from the TEG at specific hot side temperature increases linearly with the number of cells in the TEG. Calculations are carried out for different complementary metal oxide semiconductor (CMOS) and carbon nanotube field effect transistors (CNFET) processes as various technology nodes. As seen from the results, the number of adders which can be operated by waste heat thermoelectricity will be higher for 32 nm CNFET technology and it is also considerably more than the 16 nm low-power standard CMOS process. As the number of adder circuits that can be run from TEG at specific hot side temperature increases linearly with the number of cells in TEG, TEG with large number of cells will be able to run large number of adder circuits. So, as the possible number of TEG that can be accommodated on a microprocessor is large, we can run a large number of adder circuits as well as small microprocessor or microcontroller.

To conclude, we have described here a novel self-powering technique that involves power regeneration from dissipated (wasted) heat in integrated circuits. Based on simulated data and the results from the experimental verification, we have proved the possibility of reusing wasted thermal power from CMOS chips using thermoelectric regeneration. By integrating on-chip thermoelectric generators, we hope to achieve energy independent System-on-Chip (SoC).

References

Antonova E, Looman D (2005) Finite elements for thermoelectric device analysis in ANSYS. IEEE 24th Int Conf Thermoelect 205–208

Borkar S (2001) Low power design challenges for the decade. Proc Asia South Pacific Design Automation Conf 293–296

Chowdhury I, Prasher R, Lofgreen K, Chrysler G, Narasimhan S, Mahajan R, Koester D, Alley R, Venkatasubramanian R (2009) On-chip cooling by superlattice-based thin-film thermoelectrics. Nat Nanotechnol 4(4):235–238

DiSalvo F (1999) Thermoelectric cooling and power generation. Science 285(5428):703–706

Hudak N, Amatucci G (2008) Small-scale energy harvesting through thermoelectric, vibration, and radio frequency power conversion. J Appl Phys 103:101301-1–101301-4

Jaegle M (2008) Proceedings of COMSOL Conference, Hannover

Marlow Industries Inc., TG12-2.5 Thermoelectric Power Generator. http://www.marlow.com/media/marlow/product/downloads/tg12-2-5-01l/TG12-2-5.pdf. Accessed 25 July 2011

Majumdar A (2004) Thermoelectricity in semiconductor nanostructures. Science 303:777–778

Narasimhan S, Chiel H, Bhunia S (2009) A preferential design approach for energy-efficient and robust implantable neural signal processing hardware. Proc IEEE Eng Med Biol Soc 6383–6386

Nextreme thermal solutions, "Thin film thermoelectric power generation". http://www.nextreme.com/media/pdf/whitepapers/Nextreme_Thin_Film.pdf. Accessed 25 July 2011

Pop E, Sinha S, Goodson K (2006) Heat generation and transport in nanometer-scale transistors. Proc IEEE 94(8):1587–1601

Rowe D (2006) Thermoelectrics Handbook: macro to nano. CRC/Taylor and Francis, Boca Raton

Venkatasubramanian R, Siivola E, Colpitts T, O'Quinn B (2001) Thin-film thermoelectric devices with high room-temperature figures of merit. Nature 413(6856):597–602