Movable MEMS Devices on Flexible Silicon

Dissertation/Thesis by

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In Partial Fulfillment of the Requirements

For the Degree of

Master of Science

King Abdullah University of Science and Technology

Thuwal, Kingdom of Saudi Arabia

Insert Approval Date

5th/ May/ 2013
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© Approval Date: 5th May 2013

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ABSTRACT

Movable MEMS Devices on Flexible Silicon

Sally Mamdouh Ahmed

Flexible electronics have gained great attention recently. Applications such as flexible displays, artificial skin and health monitoring devices are a few examples of this technology. Looking closely at the components of these devices, although MEMS actuators and sensors can play critical role to extend the application areas of flexible electronics, fabricating movable MEMS devices on flexible substrates is highly challenging. Therefore, this thesis reports a process for fabricating free standing and movable MEMS devices on flexible silicon substrates; MEMS flexure thermal actuators have been fabricated to illustrate the viability of the process. Flexure thermal actuators consist of two arms: a thin hot arm and a wide cold arm separated by a small air gap; the arms are anchored to the substrate from one end and connected to each other from the other end. The actuator design has been modified by adding etch holes in the anchors to suit the process of releasing a thin layer of silicon from the bulk silicon substrate. Selecting materials that are compatible with the release process was challenging. Moreover, difficulties were faced in the fabrication process development; for example, the structural layer of the devices was partially etched during silicon release although it was protected by aluminum oxide which is not attacked by the releasing gas. Furthermore, the thin arm of the thermal actuator was thinned during the fabrication process but optimizing the patterning and etching steps of the structural layer successfully solved this problem. Simulation
was carried out to compare the performance of the original and the modified designs for the thermal actuators and to study stress and temperature distribution across a device. A fabricated thermal actuator with a 250 µm long hot arm and a 225 µm long cold arm separated by a 3 µm gap produced a deflection of 3 µm before silicon release, however, the fabrication process must be optimized to obtain fully functioning devices on flexible silicon.
Acknowledgment

First, I thank Allah for finishing this work. I also thank my supervisor Dr Muhammad Hussain for giving me the great opportunity to work under his supervision and continuous guidance. I admit that he is the most organized, helpful and inspiring person I have ever met in my life. No words can describe my appreciation and gratitude to Dr Muhammad and all the group members.

I would like also to thank my group members for their continuous unlimited support, especially Jhonathan, Aftab and Galo. This work could not have been completed without their sincere advice and help. My appreciation goes also to the nanofabrication lab staff, especially to Mr. Ahad Syed for his continuous support.

I would like to expand my thanks to the committee members Dr. Mohamed-Slim Alouini and Dr. Peng Wang for taking out the time to attend my defense and to review my thesis. Last but not least, I would like to thank my parents, family and my husband for their support and motivation throughout my masters.
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LIST OF ABBREVIATIONS

AMLCDs  Active matrix liquid-crystal displays
BHF    Buffered hydrofluoric acid
CPD    Critical point drying
DI water  Deionized water
IPA    Isopropyl alcohol
LPCVD  Low pressure chemical vapor deposition
MEMS   Micro electrical mechanical systems
PECVD  Plasma enhanced chemical vapor deposition
PSG    Phospho silicate glass
RIE    Reactive ion etching
Sc1    Standard cleaning agent 1
SEM    Scanning electron microscopy
Si$_3$N$_4$  Silicon nitride
SiO$_2$  Silicon dioxide
TFT    Thin film transistors
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1) Introduction

Flexible and stretchable electronics, which can conform on non-planer surfaces, have gained increased attention recently. Many applications such as flexible displays, flexible energy storage, health monitoring devices and artificial skin were illustrated on flexible substrates. Energy harvesting devices, such as solar cells, were demonstrated by J. Yoon et. al. in which very thin semi-transparent silicon solar microcells were fabricated on bulk silicon substrates then transferred onto flexible substrates [1]. However, it is not enough to harvest energy but it is also important to store it so that power can be supplied to the devices anytime during the day. Therefore, fabricating energy storage devices such as rechargeable lithium ion batteries and capacitors on flexible substrates such as paper [2] or plastic [3] has been considered by many researchers. For example, J. A. Rogers et. al. demonstrated rechargeable lithium ion batteries on flexible stretchable substrates; furthermore, he integrated a wireless charging system with the battery [3]. Super capacitors can also be used for storing energy such as the flexible graphene-based super capacitors demonstrated by M. F. El-Kady et. al. [4]. Besides energy applications, tremendous progress has been made in the field of flexible displays. For example, active matrix liquid-crystal displays (AMLCDs), in which the active matrix was formed by organic thin film transistors (TFTs), were demonstrated on large flexible plastic substrates [5-8]. T. Sekitani et. al. also demonstrated not only flexible but also stretchable active-matrix organic light-emitting diode displays [9]. Another interesting application that requires mounting devices on flexible substrates is artificial skin which can be used for the treatment of extensive burn injury and for more advanced robotics [10]. T. Someya et. al. demonstrated the integration of rubber pressure sensors and
temperature sensors with organic field effect transistor for artificial skin applications [11, 12]. Bio-related applications on flexible substrates were also demonstrated such as flexible surgical sutures that include temperature sensors and micro-heaters used for wound monitoring and therapy [13]. In addition, mapping brain activity was also demonstrated by J. A. Rogers et. al. using flexible foldable high density electrodes [14].

Most of these applications use organic thin film transistors (TFTs) which have low carrier mobility compared to that of their inorganic counterparts, thereby limiting their applications. Therefore, J. A. Rogers et. al. looked at the different inorganic materials that can be used with flexible plastic substrates to make high performance thin film transistors [15]. In addition, he noted that integrating most of the inorganic semiconductors with plastic substrates usually requires processing temperatures higher than the plastic thermal-degradation temperature [15]. Although silicon is the most commonly used substrate material in industry, it is not preferred as a flexible substrate because it is brittle and inflexible; however, if made thin enough, it can be flexible with an acceptable bending radius. In fact, J. P. Rojas et. al. demonstrated a process which will be discussed later for making *mechanically flexible optically transparent porous mono-crystalline silicon substrate* which will definitely expand the applications on flexible substrates [16].

Demonstrating freestanding and movable MEMS devices on flexible substrates will further expand the market of flexible electronics. For example, micro-robots on flexible substrates can be used in bio-related applications such as microsurgery, delivering or picking up specific materials to or from the body and
fighting cancer cells. An example of free standing MEMS devices are cantilevers which have many applications ranging from energy harvesting [17, 18], to biosensing [19] and logic MEMS switches [20]. Thermal actuators are also examples of free standing MEMS devices that are used for moving micro-motors, assembling the mirrors of corner-cube retro-reflectors and making micro-grippers [21]. None of these applications has been considered before for fabrication on flexible substrates. Therefore, this thesis reports a fabrication process for free standing and movable MEMS devices on flexible silicon substrates. MEMS thermal actuators are chosen as an example of movable MEMS device to be fabricated on flexible silicon. The following is a discussion of some of different thermal actuators found in the literature and a technique used to make thin flexible silicon substrates.

**MEMS Actuators**

MEMS actuators are micro-electrical mechanical devices that are used to generate mechanical movement due to electrostatic forces or thermal expansion. Electrostatic actuators produce small forces; hence, small deflections are achieved. They require high voltages $\geq 30$ V but they consume lower power [22]. On the other hand, thermal actuators produce large forces that can cause deflections up to 20 microns or even more [23]. In addition, they operate in low voltage range (2.5-12 V) which makes them more compatible with IC technology [22] but it comes with the disadvantage of higher power consumption. This literature review focuses on the thermal actuators not the electrostatic ones for their aforementioned advantages. Thermal actuators can be classified based on the direction of motion and the geometric symmetry. They can be designed to have an in-plane or out-of-plane movement. A thermal bimorph is an example of an out-of-plane thermal actuator. It
consists of two layers from two different materials stacked on top of each other. The two layers must have different coefficient of thermal expansion. When subjected to thermal heating due to current passing though the layers, the layer with larger coefficient of thermal expansion will expand more than the other layer which will cause it to deflect towards the layer with smaller coefficient of thermal expansion. It is hard to fabricate a bimorph thermal actuator with in-plane motion as placing two different materials beside each other is not an easy task [22]. Examples of thermal actuators that cause motion in the in-plane direction parallel to the substrate are thermal flexure actuator and chevron thermal actuator. The operating principle of the thermal flexure actuator is similar to the bimorph in the sense that one part expands more than the other, but the difference is that the flexure actuator has one structural layer while the bimorph has two different structural layers [22]. The thermal flexure actuator consists of two arms connected at the tip: hot arm and a cold arm as shown in Figure 1-1. The hot arm has a smaller cross section area compared to the cold arm. When current passes through the arms, the hot arm expands more than the cold arm as it has higher resistance and is heated at a faster rate. Therefore, it deflects towards the cold arm and the amount of the deflection increases as the temperature difference between the two arms increases which depends on the length and width of each arm and the gap between them [24]. The other type of the thermal actuator that produces in-plane motion is the chevron actuator (bent-beam actuator). The chevron actuator consists of a v-shaped arm anchored from both ends and deflected at a certain angle as shown in Figure 1-2. As the current flows through the arm, the tip is heated and moves parallel to the
substrate, the main advantage of this thermal actuator is that it produces linear motion unlike the aforementioned actuators which produce rectilinear motion [22].

In general, the deflection and the force produced by the thermal actuator can be increased by arranging many of them in an array.

This work focuses on the thermal flexure actuators. N. K. S. Lee et al. have done the modeling and the fabrication of poly-silicon thermal flexure actuator [24]. They used silicon oxide (SiO$_2$) and silicon nitride (Si$_3$N$_4$) as thermal and electrical insulation, Phosphorus-doped glass (PSG) as the sacrificial layer and heavily phosphorus-doped poly-silicon as the structural material for the actuator, all of which were deposited using low pressure chemical vapor deposition (LPCVD). The corresponding thickness
of each layer is shown in Table 1-1. The sacrificial layer was removed by immersing the wafer in a bath of buffered hydrofluoric acid (BHF) followed by cleaning in deionized (DI) water for half an hour and rinsing the wafer in isopropyl alcohol (IPA) for 10 minutes. The wafer was dried using a standard spin dryer.

<table>
<thead>
<tr>
<th>Material</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>1 µm</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>0.6 µm</td>
</tr>
<tr>
<td>PSG</td>
<td>2 µm</td>
</tr>
</tbody>
</table>

Table 1-1: Thickness of each layer of the thermal actuators fabricated in [24]

A deflection of the thermal actuator tip up to 12 µm was achieved by an actuator with a 3 µm wide, a 240 µm long hot arm and a 12 µm wide, a 180 µm long cold arm separated by a gap of 3 µm using 5 V. They reported that a greater deflection up to 22 µm can be realized using a longer cold arm (210 µm) as it provides bigger cooling area, thus the temperature difference between the hot and the cold arms increases causing bigger deflection.

**Flexible Si Fabrication Technique:**

The commonly used flexible substrate is plastic because of its inherent flexibility, transparency and low cost. However, as discussed earlier, plastic substrates have two main disadvantages: low carrier mobility and incompatibility with high thermal budget processing [16]. In this work, J.P. Rojas et. al. technique of making flexible silicon is used mainly because of its compatibility with high thermal budget processes. In addition, the processes of fabricating devices on silicon wafers are well-established, allowing fast progress in this area. The fabrication process of releasing
silicon pieces is shown in Figure 1-3. It starts with oxide deposition or growth followed by oxide patterning and reactive ion etching (RIE) till the silicon of the substrate is exposed. Then the silicon is etched using the BOSCH deep RIE process. After that, another layer of SiO$_2$ is grown or deposited to protect the silicon walls so that no lateral etching occurs near the surface. After that, the oxide on the bottom trenches is etched then the piece is placed in XeF$_2$ which etches the silicon starting from the bottom of the holes followed by upward etching and horizontal etching till the created caves are connected and the silicon piece is ready to be peeled off. This process is used in the release of MEMS movable devices which will be discussed in the fabrication chapter.

Figure 1-3: Fabrication process flow for releasing silicon pieces from mono-crystalline silicon wafer [16]
2) Design

The thermal flexure actuator was chosen to be fabricated on flexible Si fabric for the following reasons:

1. Unlike the chevron thermal actuator which is anchored to the substrate from both ends, the thermal flexure actuator is anchored only from one end which reduces the chances of breaking the actuator while bending the substrate.
2. It has only one structural layer which makes it easier in fabrication unlike the bimorph actuator.
3. The actuator deflects in the in-plane direction (parallel to the substrate) which reduces the error in measuring the displacement of the tip if the substrate is bent. If the displacement is vertical, then it should be taken into consideration that the displacement of the tip of the actuator from the substrate will change according to the bending radius of the Si fabric without supplying current to the actuator.

The design of a thermal flexure actuator is shown in Figure 2-1. It consists of two arms that have different widths. One arm, called the hot arm, has a smaller width compared to the other arm which has a bigger width and is called the cold arm. Both arms are anchored to the substrate from one end and are joined together at the other end. When current passes through the actuator, the temperature of the arms increases due to heat dissipation. Since the hot arm is thinner than the cold arm, its temperature rises faster than the cold arm causing it to expand more than the cold arm and deflects towards it. The cold arm has some dimples to prevent stiction of the actuator to the substrate. The pads have some etch holes which are required for
releasing a thin sheet of silicon as described later on. In addition, a built-in scale was fabricated beside each actuator to measure the deflection of the tip.

![Figure 2-1: Thermal flexure actuator design](image)

The performance of the actuator depends on the geometry and the resistivity of the structural layer and the driving current.

The following points are important in the design of the actuators:

1. Longer hot arms cause larger deflections than shorter hot arms. However, they have a higher probability of sticking to the substrate. In addition, the magnitude of the force they deliver is lower due to bowing.

2. Thinner and wider hot arm and cold arm respectively increase the deflection of the actuator.

3. A longer cold arms will be cooled faster (more area is exposed to air) which increases the temperature difference between it and the hot arm, causing larger deflections.

4. The deflection increases as the ratio between the length of cold and hot arm increases.
5. Smaller gap between the two arms causes a larger deflection. However, if the gap is too small, then heat transferred from the hot arm to the cold arm increases which makes the temperature difference between the two arms smaller causing less deflection of the actuator tip.

**Limitations on the design:**

There are two kinds of limitations in our design: channel width and separation required for silicon release and the minimum feature that can be achieved with the photolithography tool.

1. Channel width and separation:

   According to J.P. Rojas et. al., the width of the etch holes (the channel width) and the separation between them affect the release time and the final thickness of the released silicon piece. As will be discussed in the fabrication section, releasing a piece of silicon requires making channels by etching through the silicon wafer and covering the silicon side walls. After that, silicon is etched using XeF₂ gas which enters through the holes and starts to etch the bottom of each channel as shown in Figure 2-2. The etching is isotropic with a slower etch rate in the horizontal direction than the vertical direction. The thickness of the released silicon piece is the difference between the depth of the channel and the amount of upward etching of silicon which depends on the release time. Increasing the distance between the channels to increase the device area will result in longer release time till the caves formed by etching the silicon from each channel connect together, releasing the silicon piece. Moreover, the vertical upward etching of silicon
will increase, leading to a thinner silicon piece. Another important point that needs to be taken into consideration is that the etch rate of the silicon at the edges is faster than that in the middle which could lead to the complete removal of the silicon layer at the edges if the release time is long. Since larger separations increases the release time, the width of the channels can be increased to reduce the release time as shown in Figure 2-3. However, that will lead to bigger loss of the device area [16]. In this work, the channel width is 10 microns and the separation between the holes is 20 microns which results in acceptable release time of 2 hours. Therefore, the maximum width of the whole actuator - which includes hot arm width, the gap between the arms and the cold arm width - should be less than 20 microns.

Figure 2-2: Released silicon piece [16]
2. Minimum Feature Size:

The other design limiting factor is the minimum feature size achievable by the available photolithography tool. Features less than 2 microns did not survive during the development of the photoresist. Therefore, the air gap between the two arms was kept at 3 µm in all actuators as smaller gaps increase the deflection of the actuator. In addition, the width of the hot arm was also kept as small as possible (3 µm) to increase its heating rate. Since the total width of the actuator should be less than 20 microns (which is the separation between two rows of etch holes), then the cold arm width should be less than 14 microns. The width of the cold arm was designed to be 10 microns because a margin of at least 2 microns beside each arm had to be
kept to account for alignment errors. The design of the thermal flexure actuator is shown in Figure 2-4.

The following dimensions were varied in order to study their effect on the performance of the thermal actuator: the length of the hot arm, the length of the cold arm, the width of the flexure and the width of the joint that connects the two arms together. Table 2-1 contains the fixed dimensions of the thermal actuator design while Table 2-2 shows the different hot arm and cold arm lengths that were used and the ratio between them as well. In order to study the effect of having wider flexure or wider join, their widths were varied as shown in Table 2-1 for a 240 µm long hot arm, a 180 µm long cold arm and a 3 µm air gap between them.
Table 2-1: Fixed Dimensions in the thermal actuator design

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Air Gap between the hot and cold arms</td>
<td>3 µm</td>
</tr>
<tr>
<td>Hot arm width</td>
<td>3 µm</td>
</tr>
<tr>
<td>Cold arm width</td>
<td>10 µm</td>
</tr>
<tr>
<td>Flexure width</td>
<td>3 µm</td>
</tr>
<tr>
<td>Joint width</td>
<td>3 µm</td>
</tr>
</tbody>
</table>

Table 2-2: Hot arm and cold arm lengths and ratios

<table>
<thead>
<tr>
<th>Ratio</th>
<th>( L_h (\mu m) )</th>
<th>( L_{c1}(\mu m) )</th>
<th>( L_{c2}(\mu m) )</th>
<th>( L_{c3}(\mu m) )</th>
<th>( L_{c4}(\mu m) )</th>
<th>( L_{c5}(\mu m) )</th>
<th>( L_{c6}(\mu m) )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>230</td>
<td>160</td>
<td>165</td>
<td>170</td>
<td>175</td>
<td>180</td>
<td>190</td>
</tr>
<tr>
<td>( L_c/L_h )</td>
<td>0.70</td>
<td>0.72</td>
<td>0.74</td>
<td>0.76</td>
<td>0.78</td>
<td>0.83</td>
<td></td>
</tr>
<tr>
<td></td>
<td>240</td>
<td>170</td>
<td>175</td>
<td>180</td>
<td>185</td>
<td>190</td>
<td>200</td>
</tr>
<tr>
<td>( L_c/L_h )</td>
<td>0.71</td>
<td>0.73</td>
<td>0.75</td>
<td>0.77</td>
<td>0.79</td>
<td>0.83</td>
<td></td>
</tr>
<tr>
<td></td>
<td>250</td>
<td>180</td>
<td>185</td>
<td>190</td>
<td>195</td>
<td>200</td>
<td>225</td>
</tr>
<tr>
<td>( L_c/L_h )</td>
<td>0.72</td>
<td>0.74</td>
<td>0.76</td>
<td>0.78</td>
<td>0.8</td>
<td>0.9</td>
<td></td>
</tr>
</tbody>
</table>

Table 2-3: Flexure and Joint dimension variations for \( L_h = 240 \) microns, \( L_c = 180 \) microns and Air gap = 3 microns

<table>
<thead>
<tr>
<th>Flexure Width (µm)</th>
<th>Joint Width (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>3, 4</td>
</tr>
<tr>
<td>5</td>
<td>3, 4</td>
</tr>
<tr>
<td>6</td>
<td>3, 4</td>
</tr>
</tbody>
</table>

The fabrication of the thermal flexure actuator on flexible silicon fabric includes four lithographic steps (i.e. four masks were required). The first mask, shown in Figure 2-5, is for anchor patterning. The size of the anchor on each pad is 70 µm X 70 µm. The next mask is for dimple patterning which is shown in Figure 2-6 as the green
squares. Each wide arm has an array of 3 µm x 3 µm square dimples separated by a distance of 5 µm.

Figure 2-5: Firstmask for anchor patterning (in blue)

Figure 2-6: Second mask for dimple patterning (in green)

After patterning sacrificial layer with the anchor and dimple masks, the structural layer is then patterned with a bright field mask, shown in Figure 2-7. The pads contain some etch holes because etching the structural layer in the channel at this
step of the fabrication process facilitates the formation of the channels. In other words, making the etch holes involves etching through the sacrificial layer, oxide and silicon substrate. However, on the pads there is an extra material for the structural layer; so removing it at an earlier step makes the material stack, which needs to be etched later to make the holes, the same everywhere on the wafer except for the anchor which will have oxide exposed instead of the sacrificial layer. On the right side of Figure 2-7, a built-in scale is fabricated to measure the deflection of the tip of the thermal actuator. Each rectangle on the scale bar has a length of 2 µm and a width of 4 µm separated by a distance of 2 µm.

![Figure 2-7: Third mask for patterning the structural layer](image)

The last lithography step is for making the etch hole patterns; part of the mask is shown in Figure 2-8. It is clear that some holes, which are on the location of the pads of the actuators, are bigger than the rest of the holes to account for the alignment errors.
A thermal actuator with all mask layers is shown in Figure 2-9.

The whole set of masks are shown in Figure 2-10. The wafer is divided into two parts: devices on flexible silicon and devices on bulk silicon. There are three identical pieces.
of flexible silicon in the middle of the wafer while the devices on the bulk silicon substrate are located on the right and the left parts of the wafer. The reason for making devices on bulk silicon is that this is the only way of testing the thermal actuators before releasing the silicon pieces as the sacrificial layer is removed after silicon release, which means the same device cannot be tested before and after silicon release.

![Figure 2-10: The whole four masks](image-url)
3) Material Selection

1. Electric Insulation:

Silicon dioxide and silicon nitride are chosen for thermal and electric insulation. However, SiO₂ only can be used for both thermal and electrical isolation as the nitride produced by the PECVD tool in is highly stressed.

2. Sacrificial layer:

The choice of the sacrificial layer is a bit challenging. In the PolyMUMPs process where poly-silicon is used as the structural layer, phosphosilicate glass (PSG) is used as the sacrificial layer and is removed at the end using HF [25]. Amorphous silicon is also used as the sacrificial layer in a process where SU-8 acts as the structural layer [26]. In the current work, using silicon dioxide or PSG as the sacrificial layer is incompatible with silicon release process because silicon dioxide is used as the thermal and electric insulating layer. If used as the sacrificial layer, the whole SiO₂ layer would be removed including the insulating layer and the devices will be floating since they were initially anchored on SiO₂. A good solution to this problem is to cover the SiO₂ layer with silicon nitride (Si₃N₄); however, the main concern regarding Si₃N₄ deposited using plasma-enhanced chemical vapor deposition (PECVD) is that it is highly stressed. Hence, it can curl and break the thin silicon piece. Therefore, Si₃N₄ was avoided in the developed process. In addition, Si₃N₄ can also be etched using HF but with a slower etch rate. Moreover, after silicon release, the oxide, used for channel side wall protection, will be etched followed by the removal of the oxide sacrificial layer which will be attacked not only from the top, but from the sides as well because of the holes. That will speed the oxide etch which could end up with having a floating Si₃N₄ layer. The other choice of using amorphous silicon as the
sacrificial layer is impossible since the used structural layer is poly-silicon which is etched with the same chemistry as amorphous silicon. Therefore, the required properties of the sacrificial layer is summarized in Table 3-1.

<table>
<thead>
<tr>
<th>Property</th>
<th>Example</th>
<th>Restriction</th>
<th>Conclusion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Can be dry etched using a vapor phase etchant</td>
<td>1- SiO₂, Si₃N₄</td>
<td>- SiO₂ is used as the insulating layer;</td>
<td>1- For HF: use a sacrificial material</td>
</tr>
<tr>
<td></td>
<td>2- Amorphous Si</td>
<td>therefore it cannot be used as the sacrificial layer.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hence, HF cannot be used.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>- The structural layer of the thermal actuators is poly-silicon and can be etched using XeF₂. Therefore, XeF₂ cannot be used.</td>
<td>2- For XeF₂: use a sacrificial material that has a much faster etch rate than poly-silicon etch rate or use a different structural layer that is not etched by XeF₂</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3- Use wet etchant</td>
</tr>
<tr>
<td>- Can be etched with wet chemicals that does not attack SiO₂ or poly-silicon</td>
<td>Metals such as Al or W</td>
<td>- Can be dry etched using reactive ion etching tools</td>
<td></td>
</tr>
</tbody>
</table>

Table 3-1: Sacrificial layer properties
Since silicon dioxide and amorphous silicon cannot be used as sacrificial layers for the thermal actuator, a metal sacrificial layer could be tried. The etching chemistry of some metals such as tungsten and aluminum were investigated as shown in Table 3-2. Tungsten can be dry etched using SF$_6$ or CH$_4$+O$_2$ gases in reactive ion etching chamber while Aluminum needs plasma of chlorine containing gas. Since XeF$_2$ will be used to release the silicon piece, it was important to check if it will attack the other used materials or not. In fact, XeF$_2$ attacks tungsten rapidly while it does not etch aluminum. That gives an advantage for the aluminum to be used as the sacrificial layer. However, a protection layer of Al$_2$O$_3$ will be covering everything, therefore no need to worry about XeF$_2$ effect. By looking at the wet etchants for aluminum in Table 3-2, the first etchant is not an option since it attacks Si$_3$N$_4$. Although the second etchant does not attack SiO$_2$ nor, the Si$_3$N$_4$, it is very poisonous and better to be avoided. To etch tungsten, SC1 can be used since it is available and can be easily prepared. Therefore, tungsten was chosen as the sacrificial layer.

<table>
<thead>
<tr>
<th></th>
<th>Tungsten (W)</th>
<th>Aluminum (Al)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RIE</td>
<td>SF$_6$ +O$_2$ [27]</td>
<td>BCl$_3$/Cl$_2$, SiCl$_4$/Cl$_2$, HBr/Cl$_2$ [28]</td>
</tr>
<tr>
<td>Gases: CF$_4$/O$_2$</td>
<td>Aluminum can be etched in a plasma of any gas contains chlorine such as BCl$_3$, CCl$_4$, SiCl$_4$, HCl or Cl$_2$ with an etch rate in the range of 0.1-1 microns/min. - Cannot be etched in fluorine plasma [29].</td>
<td></td>
</tr>
</tbody>
</table>
mTorr.
The total gas flow was 100 sccm

<table>
<thead>
<tr>
<th>Pressure: 25 mTorr</th>
<th>Pressure: 250 mTorr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max etch rate</td>
<td>Max etch rate</td>
</tr>
<tr>
<td>100nm/min @30% O₂</td>
<td>170nm/min @35% O₂</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Xef₂</strong></th>
<th>Etches W very rapidly [31]</th>
<th>Does not etch Al [31]</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th><strong>Wet Etching</strong></th>
<th><strong>Etchants:</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>HF : HNO₃ [32]</td>
<td>1- 19 H₃PO₄ : 1 HAc : 1 HNO₃ : 2 H₂O</td>
</tr>
<tr>
<td>SC1 (H₂O: H₂O₂: NH₄OH) [27]</td>
<td>Etch rate : 40 Å/s</td>
</tr>
<tr>
<td></td>
<td>Also Etches: Si₃N₄, M</td>
</tr>
<tr>
<td></td>
<td>Does NOT etch: SiO₂, Si, PR</td>
</tr>
<tr>
<td>2- 10% K₃Fe(CN)₆</td>
<td>Etch rate : 100 Å/s</td>
</tr>
<tr>
<td></td>
<td>Does NOT etch: ZnO, SiO₂, Si₃N₄, Si, M, PR [33]</td>
</tr>
</tbody>
</table>

Table 3-2: Tungsten Vs Aluminum dry and wet etching chemistry

3. Structural layer:

   Heavily doped poly-silicon is used as the structural layer material in most
MEMS actuators. It is also common to use metals but heavily doped poly-silicon is preferred for the following reasons:

1- Poly-silicon has higher resistivity than metals. Therefore, the amount of voltage and current required to move a poly-silicon actuator is less than those required for metal actuators to move.

2- Voltages and currents required to move poly-silicon actuators are compatible with IC technology. For example, J.H Comtois et. al. reported that 2.94 V and 3.68 mA were required to move the tip of a 220 µm long, 2 µm thick poly-silicon actuator with a 2.5 µm hot arm a distance of 16 µm [21].

For these reasons, heavily doped poly-silicon is used as the structural layer of thermal actuators.
4) Fabrication process

A process has been developed to fabricate free standing and movable devices on flexible silicon substrates. Thermal actuators were chosen to demonstrate the viability of the developed process. The process is illustrated below.

**Step 1: Oxide Growth**

A 300 nm thick thermal oxide was grown on heavily doped p-type wafers. Any type of wafer can be used since it acts as a support for the devices (it could be an n-type, a p-type, a lightly doped or a heavily doped wafer). A thick silicon dioxide layer results in better thermal actuator performance due to less heat loss to the substrate.

![Figure 4-1: Oxide Growth](image)

**Step 2: Silicon Nitride Deposition**

The silicon nitride layer provides more electric insulation but it is optional since the dioxide acts as both an electric and thermal insulator. For some wafers, a 100 nm low stressed Si$_3$N$_4$ layer was deposited using plasma enhanced chemical vapor deposition (PECVD) as shown in Figure 4-2. Although the nitride is supposed to be low stressed, it came out to be highly stressed. Therefore, it was avoided in order not to break the silicon fabric once released.
Step 3: Sacrificial Layer Deposition

After the deposition of the electric and thermal insulation layer(s), a 600 nm-900 nm thick tungsten layer is deposited. As mentioned before, tungsten was chosen as the sacrificial layer as it is more compatible with silicon release process. It was deposited by sputtering a tungsten target; the deposition parameters are shown in Table 4-1.

<table>
<thead>
<tr>
<th><strong>Table 4-1: Tungsten deposition parameters</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DC power</strong></td>
</tr>
<tr>
<td><strong>Ar gas flow</strong></td>
</tr>
<tr>
<td><strong>Pressure</strong></td>
</tr>
<tr>
<td><strong>Time</strong></td>
</tr>
</tbody>
</table>

Step 4: Anchor Patterning

After tungsten deposition, a layer of AZ ECI 3027 positive photoresist is spun on the wafer followed by baking at 100°C for 60 seconds to drive off the solvents in the photoresist. A 4 µm thick photoresist layer was formed. The photoresist is then exposed and patterned with the anchor dark field mask using the contact aligner
available in the clean room followed by photoresist development in AZ 627 MIF developer for 60 seconds. The wafer is then cleaned with DI water to remove the developed photoresist. After that, the wafer is placed in a reactive ion etching (RIE) tool to etch the tungsten (W) and form the anchors. The recipe for etching W is shown in Table 4-2. The etch rate of tungsten under the mentioned conditions is around 130-150 nm/min. Over etching for anchor formation was required to make sure that all the tungsten was removed from the anchor area. After etching the tungsten, the photoresist is removed using acetone followed by cleaning the wafer with IPA and DI water.

<table>
<thead>
<tr>
<th>RF power</th>
<th>75 Watt</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICP power</td>
<td>1200 Watt</td>
</tr>
<tr>
<td>Pressure</td>
<td>10 mTorr</td>
</tr>
<tr>
<td>SF6 flow</td>
<td>20 sccm</td>
</tr>
<tr>
<td>Ar flow</td>
<td>5 sccm</td>
</tr>
</tbody>
</table>

Table 4-2: Tungsten RIE conditions

Figure 4-4: Sacrificial layer patterning

**Step 5: Dimple Patterning**

The dimple is then formed in similar way. Since the dimple dimensions are small (3 µm x 3 µm), a thinner photoresist was required. A layer of AZ 1512 HS positive
photoresist was spun on the wafer with 3000 rpm speed which produces a 1.4 µm thick photoresist layer. The photoresist is then baked at 100 °C for 60 seconds and exposed with an exposure dose of 40 mJ/cm². The photoresist is then developed using MIF 726 developer for 20 seconds and the wafer is cleaned with DI water and dried. Using the same tool and recipe for tungsten etching in the anchor patterning step, half the thickness of the sacrificial layer is etched to form the dimples. In the previous step, 850 nm of W were etched in 6 minutes. Therefore, the tungsten is etched for 3 minutes only to form the dimple area. Over etching in this step was not preferred.

![Figure 4-5: Dimple patterning](image)

**Step 6: Structural Layer Deposition**

After anchor and dimple patterning, a 2 µm thick heavily doped n-type poly-silicon layer is deposited using PECVD tool. A phosphorous containing gas is flown inside the chamber at 20 sccm flow rate which is the maximum rate that results in the maximum doping level that can be achieved using this tool. The poly-silicon is then annealed for dopant activation at 950°C for 30 seconds. This step is important as it leads to reduction of the resistance of poly-silicon by 3 orders of magnitude. The measured resistivity of heavily doped poly-silicon was 2 m ohm cm.
Step 7: Structural Layer Patterning

After annealing poly-silicon and before spinning the photoresist, the wafer is covered with a layer of HDMS to provide better adhesion of the photoresist to the poly-silicon layer. A layer of AZ 1512 HS positive photoresist is spun on the wafer to form a 1.4 µm thick photoresist. The photoresist is then baked for 60 seconds and patterned using the third mask. The reason for using a thin photoresist is that the hot arm of the actuator is 3 µm wide. The recipe for etching poly-silicon is listed in Table 4-3.

<table>
<thead>
<tr>
<th>RF Power</th>
<th>50 watt</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICP Power</td>
<td>800 watt</td>
</tr>
<tr>
<td>Pressure</td>
<td>6 mTorr</td>
</tr>
<tr>
<td>SF₆ Flow</td>
<td>15 sccm</td>
</tr>
<tr>
<td>O₂ Flow</td>
<td>4 sccm</td>
</tr>
</tbody>
</table>

Table 4-3: Polysilicon RIE recipe
Normally, the sacrificial layer is removed after this step to release the devices. Since there are still more steps to release the silicon that involves RIE and deep RIE, the sacrificial layer is kept as a mechanical support for the actuators. In addition, since there is one lithography step left, DI water will be used after developing and stripping the photoresist. The actuators will stick to the substrate unless critical point drying is used for drying. This is time consuming and can be avoided by etching the tungsten at the very end after releasing the silicon piece.

**Step 8: Protection Layer Deposition**

Since XeF$_2$ is used to etch the silicon substrate to make it flexible, the poly-silicon structures and the tungsten layer must be protected as they are also attached by XeF$_2$. Therefore, a 40 nm protection layer of Al$_2$O$_3$ is deposited using ALD to protect the poly-silicon structures as the Al$_2$O$_3$ is not etched in XeF$_2$. 

*Figure 4-8: Aluminum oxide deposition*
Step 9: Holes Patterning

The next step is to make the holes by etching though \( \text{Al}_2\text{O}_3 \), W, Si$_3$N$_4$ and SiO$_2$ layers.

To make the whole patterns, a layer of AZ ECI 3027 photoresist is spun on the wafer at a spinning speed of 1750 rpm to result in a thickness of 4 µm. The photoresist is then baked at 100°C for 60 seconds. The photoresist has to be thick to protect the wafer surface as the wafer will go through several RIE steps and one deep RIE step. The photoresist is then patterned with the holes dark field mask with an exposure does of 200 mJ/cm$^2$. Next, the photoresist is developed in MIF 726 developer for 60 seconds followed by rinsing the wafer with DI water and drying it with a nitrogen gun. The first layer that should be etched to form the holes is the \( \text{Al}_2\text{O}_3 \) layer. The recipe, shown in Table 4-4, etches \( \text{Al}_2\text{O}_3 \) in a reactive ion etching tool with an etch rate of 40 nm/min.

<table>
<thead>
<tr>
<th>RF Power</th>
<th>100 watt</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICP Power</td>
<td>1000 watt</td>
</tr>
<tr>
<td>Pressure</td>
<td>5 mTorr</td>
</tr>
<tr>
<td>CH$_3$ Flow</td>
<td>20 sccm</td>
</tr>
<tr>
<td>Ar Flow</td>
<td>5 sccm</td>
</tr>
</tbody>
</table>

Table 4-4: \( \text{Al}_2\text{O}_3 \) etchign recipe
Al$_2$O$_3$ is etched using CH$_3$ gas while tungsten, silicon dioxide and silicon nitride are etched with a different gas (SF$_6$). Therefore, etching these three layers was done in one step using the same recipe for etching tungsten that was previously mentioned in Table 4-2 using longer time.

**Step 10: Silicon Deep RIE**

Deep channels have to be opened in the Si wafer so that XeF$_2$ can go through them and release a thin layer of the silicon wafer. The depth of the channel is determined...
by the separation between the holes and the desired thickness of the flexible piece. In the actuator design, the holes were separated by a distance of 20 µm and they had a diameter of 10 µm. Around 50 µm deep channels were formed using the Bosch process. The Bosch process consists of several deposition and etching steps and is mainly used to create high aspect structures with straight side walls. The Bosch process has many advantages:

- High aspect ratio structures can be created with vertical side walls because it uses high density plasma with low pressure which decreases the collisions between the ions, hence they do not scatter.
- It can create deep trenches using low pressure as it allows the gases to reach and etch the bottom of the trenches.
- High selectivity between the masking layer and the silicon gives it a great advantage (Si: Photoresist, 1: 75).

The Bosch process includes cycles of depositions of a passivation layer using C₄F₈ gas followed by etching the bottom of the trenches using SF₆. Then the process of surface passivation and bottom trench etching is repeated a certain number of cycles to get the desired depth.

Figure 4-11: Silicon deep reactive ion etching (RIE)
Step 11: Spacer Formation

After forming the deep trenches, the side walls have to be protected from XeF$_2$, otherwise the silicon will be etched from the top as well. A 40 nm layer of ALD Al$_2$O$_3$ is deposited on the wafer. The total thickness of the Al$_2$O$_3$ layer on the surface of the wafer is 80 nm while the channels have only 40nm thick Al$_2$O$_3$ on the bottom and the sidewalls. The wafer is then placed in the RIE tool to form the spacers by etching 40 nm of Al$_2$O$_3$ form everywhere. Low pressure of 3 mTorr is used to make sure that CH$_3$ gas reaches the bottom of the trench and etches the Al$_2$O$_3$ from there to open a path for XeF$_2$ to etch the silicon substrate. A high pressure is used at the beginning to start the plasma (10 mTorr) then the pressure is brought down again to 3 mTorr. The thickness of the Al$_2$O$_3$ on the surface should decrease to 40 nm after the etching step since no masking layer was used.

Figure 4-12: Spacer formation
Step 12: XeF2 Release

The silicon pieces are then placed in XeF2 etching system. An average of two hours was required to release the silicon pieces by connecting the caves formed by etching the silicon at the bottom laterally and vertically. Leaving the silicon piece for longer time in the XeF2 leads to more etching in the upward direction which results in thinner Si piece. Around 120 etching cycles were used (each cycle is 60 seconds) and the pressure of the XeF2 gas was 4.5 mTorr.

![Diagram of XeF2 release](image)

Step 13: Al2O3/ Sacrificial Layer Removal

Al2O3 and tungsten are removed by rinsing the wafers in standard cleaning agent 1 (SC1) with the following ratios: (DI: H2O2: NH4OH , 2: 1: 1) at 60°C for approximately one hour. The silicon pieces are then rinsed with DI water.
Step 14: Critical Point Drying

The silicon pieces are then dried using critical point drying method because the normal drying will probably cause stiction of the thermal actuators to the wafer. The critical point is the point at which the liquid phase is transferred into gas phase without having two different phases at the same time. Having two different densities concurrently is what causes the cantilevers to collapse and stick to the wafer. The critical point drying process works as follows: after the pieces are cleaned with DI water, they are covered with IPA till they are transferred to the critical point drying (CPD) tool. When transferred to the CPD tool, the pieces that needs to be dried are placed inside a chamber and covered either with IPA, Ethanol or Methanol. The chamber is then left to cool down to 8°C. After that, the chamber is filled with liquid carbon dioxide (LCO₂). Then, the liquid is purged out of the chamber to make sure that no IPA is still inside. After that, the chamber is filled again with LCO₂ and the pressure and temperature start to increase till the critical point is reached (critical pressure is 1075 psi and the critical temperature is 31°C). The temperature is raised above 31°C and the pressure stabilizes at 1350 psi. The temperature and the pressure are maintained above the critical point for some time then the pressure
starts to drop and the temperature as well. After the pressure drops to zero psi, the samples are taken out of the tool.

Figure 4-15: Sacrificial layer etching
5) Discussion and Results

In this chapter, the challenges faced during the fabrication process are discussed and how they were overcome.

Fabrication wise:

- Tungsten peeling off:

  One of the challenges faced during the fabrication and testing of the thermal actuators is that they had very high resistance in the mega ohm range. Hence, the applied voltage could not create enough current to heat the thermal actuator and cause them to deflect. In this case, the heavily doped poly-silicon was not annealed after deposition. One way to decrease the resistivity of the heavily doped poly-silicon is to do dopant activation annealing which was performed in a RTP tool at 950°C for 30 seconds. A small piece was annealed and it looked fine with a decrease in the resistance of the actuators by three orders of magnitude. However, when a whole 4” wafer was annealed, the tungsten below started to peel off. This is probably due to the difference in the coefficient of thermal expansion (CTE) of tungsten and silicon. The linear CTE of tungsten is \(4.3 \times 10^{-6}\) m/m K while that of silicon is \(3 \times 10^{-6}\) m/m K. When the temperature increases, each layer starts to expand and needs room for expansion, if there is no room for expansion, then stress starts to accumulate in that layer. In the case of poly-silicon annealing, it was done before patterning the poly-silicon layer for one sample and after patterning the poly for another sample. In the first sample, the tungsten was peeling off after the sample is annealed. A possible reason is
that the tungsten did not have much room to expand because of the poly-silicon layer on top; hence a lot of stress was accumulated in the tungsten layer. When it starts to cool down and shrink, the tungsten curls and peels off. In the other case where poly-silicon was patterned and etched before annealing, the tungsten did not peel off as poly-silicon was covering small parts of it in the device areas only allowing the tungsten to expand without accumulating much stress. However, the poly-silicon arms were deformed. It is more logical to anneal the poly-silicon before patterning it. In order to avoid peeling off the tungsten, a lower annealing temperature was used (600°C) and a 10 nm titanium adhesion layer was used to make sure that the tungsten sticks well to the SiO₂ underneath.

Figure 5-1: Tungsten peeling off the substrate after annealing the poly-silicon at 950°C for 30 seconds
• Poly-silicon patterns becoming thinner:

Another challenge that was faced during the fabrication process is related to the dimensions of the designed thermal actuator. The actuator was designed to have a 3 µm wide hot arm, 10 µm wide cold arms and a 3 µm separation between them. Small features require thin photoresist layer so that the patterns are transformed to the layer with good accuracy. At the same time, if the layer needed to be etched is thick, then a thick photoresist is required to provide enough protection to the covered areas as the photoresist is also etched and thinned during the RIE process. A 2.5 µm thick photoresist was used to pattern the poly using RIE. However, the arms of the thermal actuators had wavy side walls and the thin arm was becoming even thinner with a width of 1 µm instead of 3 µm as shown in Figure 5-2. In the following run, a thinner photoresist was used (1.4 µm) to get more vertical side walls and hopefully to keep the thin arm width as designed. However, the sidewalls were also wavy and the thin arms also became thinner. The problem of obtaining thinner hot arms was solved by making sure that the photoresist was not over developed even by few seconds and by immersing the wafer in DI water to clean it and remove the developed photoresist without using the DI water gun. However, the wavy sidewalls were still there. This problem was solved by using deep RIE (the Bosch process) to etch the silicon instead of using RIE. The advantage of the deep RIE is that it creates vertical sidewalls and etches the 2 µm thick poly in much less time than the time required by RIE. The best looking thermal actuator resulted from using 4 µm thick photoresist to pattern the poly-silicon and deep RIE to etch it.
Figure 5-2: SEM image of a thin arm becoming thinner after RIE

Figure 5-3: Microscope Image of a thermal actuator patterned using deep RIE and 1.4 μm thick photoresist
Figure 5-4: SEM image of thermal actuator patterned using deep RIE and 4 µm thick photoresist

- XeF$_2$ release challenges

  1. Holes mask alignment:

     Aligning the hole mask to the poly-silicon layer was the most critical step because any misalignment greater than 2 µm will result in making the hole patterns on top one of the actuator arms. It becomes more problematic if the holes are overlapping with the thin arm because it can make it discontinuous. Two different diameters of the holes in the pad areas were tried. The first diameter was exactly the same as the diameter of the holes in the poly-silicon pads. In this case, any misalignment error would decrease the holes’ opening causing problems in XeF$_2$ release.

     Figure 5-5 shows an SEM cross sectional image of an unreleased silicon piece. Due to holes misalignment with the poly-silicon layer, some
channels were not etched which made it difficult for all the silicon caves etched by XeF$_2$ to connect leading to non-uniform XeF$_2$ release as shown in Figure 5-6. This non-uniform release was only in the pads' area but the areas where there were no devices were perfectly released as shown in Figure 5-7. The thickness of the released piece is 18.5 µm with channel depth of 34.2 µm and an upward etching of 16 µm. Bigger holes in the holes mask were also tried to have some room for the inevitable alignment errors. However, they even grew bigger during XeF$_2$ to the extent that the thin arm was disconnected from its pad as shown in Figure 5-9.
Figure 5-5: SEM image of unreleased Si piece after channel formation.

Figure 5-6: SEM image of a released Si piece with defects in the pads area
2. $\text{Al}_2\text{O}_3$ not fully protecting the poly-silicon structures:

Another problem noticed after $\text{XeF}_2$ release is that the poly-silicon layer was being etched which means that the $\text{Al}_2\text{O}_3$ was not protecting it very well as shown in Figure 5-9 and Figure 5-10. The edges of the arms in these two figures are the $\text{Al}_2\text{O}_3$ layer that was protecting the side walls of the poly-silicon structures. One reason that could have led to etching the poly is that the thin arm in most of the devices
contained some unwanted holes as shown in Figure 5-11. Al$_2$O$_3$ probably was not able to cover these holes neither from the top nor from the sidewalls, thus allowing the XeF$_2$ to go through them and attack the poly-silicon layer.

Figure 5-9: SEM image of the flexure of a thermal actuator after XeF$_2$

Figure 5-10: SEM images of a thermal actuator after XeF$_2$
Moreover, part of the silicon was etched not only from the bottom as expected but also from the top as shown in Figure 5-12. In addition, part of the tungsten was also etched leaving the Al₂O₃ layer hanging as shown in Figure 5-13 and Figure 5-14.
Figure 5-13: Tungsten etched during XeF release

Figure 5-14: Tungsten partially etched during XeF leaving the AlO layer hanging.
Simulation Results:

Simulation was done by COMSOI software to predict the deflection amount of the thermal actuators with holes and without holes. The flexure thermal actuator models are shown in Figure 5-15 and the dimensions are listed in Table 5-1. The simulation was done to study the temperature and stress distribution across the thermal actuator devices. The deflection of the tip of the thermal actuator was also studied versus the applied current.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Hot arm width</td>
<td>3 µm</td>
</tr>
<tr>
<td>Cold arm width</td>
<td>12 µm</td>
</tr>
<tr>
<td>Hole diameter</td>
<td>10 µm</td>
</tr>
<tr>
<td>Hole separation</td>
<td>20 µm</td>
</tr>
<tr>
<td>Poly-silicon thickness</td>
<td>2 µm</td>
</tr>
<tr>
<td>Air gap between the hot and cold arms</td>
<td>3 µm</td>
</tr>
<tr>
<td>SiO₂ thickness</td>
<td>1 µm</td>
</tr>
<tr>
<td>Si₃N₄ thickness</td>
<td>1 µm</td>
</tr>
<tr>
<td>Air gap between the thermal actuator and the substrate</td>
<td>2 µm</td>
</tr>
<tr>
<td>Resistivity of heavily doped poly-silicon</td>
<td>1 m ohm cm</td>
</tr>
<tr>
<td>Young’s modulus of poly-silicon</td>
<td>150 x 10⁹ Pascal</td>
</tr>
<tr>
<td>Thermal expansion coefficient of poly-silicon</td>
<td>2.7 x 10⁻⁶ C⁻¹</td>
</tr>
<tr>
<td>Thermal conductivity of poly-silicon</td>
<td>30 W m⁻¹ C⁻¹</td>
</tr>
<tr>
<td>Thermal conductivity of air</td>
<td>0.026 W m⁻¹ C⁻¹</td>
</tr>
<tr>
<td>Thermal conductivity of SiO₂</td>
<td>2.25 W m⁻¹ C⁻¹</td>
</tr>
<tr>
<td>Thermal conductivity of Si₃N₄</td>
<td>1.4 W m⁻¹ C⁻¹</td>
</tr>
</tbody>
</table>

Table 5-1: Dimensions and parameters used in the simulation
Stress Analysis:

The distribution of the stress across the thermal actuator due to an applied current of 2.5 mA is shown in Figure 5-16 where the maximum stress is experienced at the connection between the flexure and the pad at the cold arm side (Figure 5-17). That is expected since the hot arm elongates as current passes through it and deflects towards the cold arm forcing it to move in the same direction which results in a huge stress at the fixed part connecting the cold arm with left pad.
Temperature distribution:

The temperature distribution across the thermal actuator with an applied current of 2.5 mA is shown in Figure 5-18. The thin arm experiences the maximum temperature because it has the largest resistance (smallest cross sectional area). The cold arm temperature is also high but the deflection increases with increasing the difference between the two arms' temperatures. You can notice that the temperature of the pads and the flexure is much lower because the pads are physically connected to the substrate which allows heat loss through it.
Displacement results:

It was also important to check whether the holes in the anchor will affect the deflection of the thermal actuator or not. Figure 5-18 shows the tip displacement versus the applied current for both a thermal actuator with no holes in the anchor and a thermal actuator with holes in the anchor. The deflection, of course, increases by increasing the current as the arms get heated more. In addition, a slight increase in the tip displacement was noticed in case of the thermal actuator with holes in the pads. That is logical since the existence of the holes decreases the contact area between the pads and the substrate leading to less thermal conduction through the substrate.
Experimental Results:

Basically, it was planned to have two sets of devices: some on flexible silicon and others on bulk silicon. The same device cannot be tested before and after release because the sacrificial material cannot be removed before releasing the silicon with XeF$_2$. Some of the fabricated thermal actuators on bulk silicon were tested. Error! Reference source not found. shows an image of a 2 µm thick thermal actuator with a 225 µm long cold arm and a 250 µm long hot arm separated by 3 µm wide air gap. As the used poly-silicon is heavily doped, it was expected that a current in the mA range can be obtained by a voltage < 10 V as reported in the literature[24]. However, the resistance of the actuators was too high that even large voltages such as 90 V gave only 0.07 mA which means that the poly-silicon was not really conductive. Figure 5-22 shows the voltage and current relationship of the tested thermal actuator. At voltages >90 volt, the thermal actuator was burnt as shown in Figure 5-21 (b). The maximum tip displacement that was obtained is 3 µm. These results do not match the simulation due to the high resistivity of poly-silicon.
Unfortunately, there were no fully surviving devices on the flexible silicon as the poly-silicon structures were etched during XeF$_2$ release. Optimizations in the fabrication process are required to obtain better results as discussed in the next chapter.

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**Figure 5-22:** Voltage and current curve for a 225 µm cold arm and 250 µm hot arm
6) Future work

Since most of the poly-silicon thermal actuators did not survive during XeF$_2$ release step, several options can be tried as discussed below.

A. Deposit thicker Al$_2$O$_3$ protecting layer in Step 8: Protection Layer Deposition in the fabrication process to make sure that the poly-silicon is well protected.

B. Use a different protection layer.

C. Choose a different conductive structural layer other than poly-silicon that is not etched by XeF$_2$.

D. Try to replace critical point drying step by using a vapor phase etchant such as HF. SiO$_2$ can be used as the sacrificial layer if a thick layer of Si$_3$N$_4$ is deposited on top of a very thick layer of SiO$_2$. The SiO$_2$ insulating layer must be much thicker than the SiO$_2$ sacrificial layer so that when the sacrificial layer is etched, only a small part of the insulating layer is etched away.

E. Make bigger holes and larger separation between them to have more flexibility in the thermal actuator design.
7) Conclusion

The fabrication process of free standing and movable MEMS devices on flexible silicon substrates has been illustrated. The most frequently used sacrificial materials in fabricating free standing MEMS devices could not be used to make these devices on flexible silicon because of their incompatibility with the silicon release process. Therefore, a new material, tungsten, was selected for the sacrificial layer. Thermal flexure actuators were designed and fabricated to illustrate the developed process; devices were designed with etch holes required for releasing the silicon. Several challenges were faced during the fabrication process, some of which have been tackled. However, some steps must be optimized to obtain fully functioning devices on flexible silicon substrates. The devices were tested before releasing the silicon piece and a deflection of 3 μm was achieved by a thermal actuator with a 250 μm long hot arm and a 225 μm long cold arm. Simulation was also carried out to check the functionality of the actuators with holes in the anchors compared to those without holes and to study the stress and temperature distribution across the devices. A slight increase in the deflection of the actuator tip in the anchor with holes was noticed due to less thermal conduction between the anchors and the substrate. Some solutions to the faced problems were suggested for future work such as trying different materials for the structural and sacrificial layer, using a thicker poly-silicon protection layer or choosing a different protection layer.
References


[31] *Xenon Difluoride Etching System* [Lab Manual]. Available: [http://nanolab.berkeley.edu/labmanual/chap7/7.5etch.pdf](http://nanolab.berkeley.edu/labmanual/chap7/7.5etch.pdf)
