

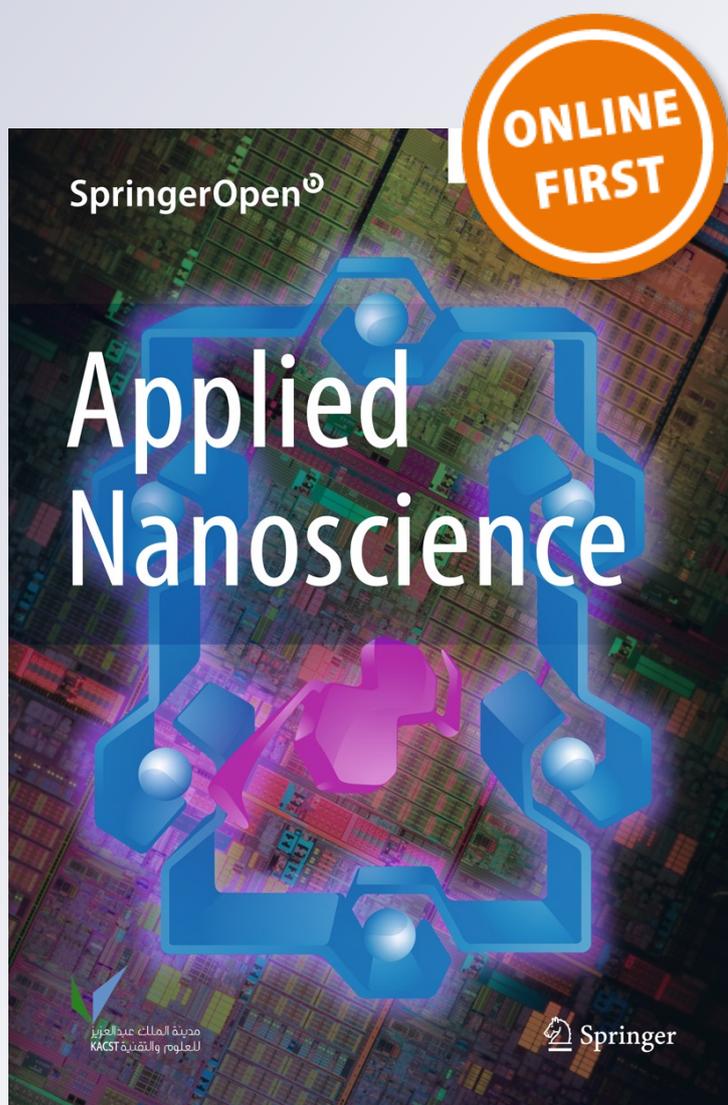
# *Achieving nanoscale horizontal separations in the standard 2 $\mu\text{m}$ PolyMUMPS process*

**A. M. Elshurafa & K. N. Salama**

**Applied Nanoscience**

ISSN 2190-5509

Appl Nanosci  
DOI 10.1007/s13204-013-0195-z



**Your article is published under the Creative Commons Attribution license which allows users to read, copy, distribute and make derivative works, as long as the author of the original work is cited. You may self-archive this article on your own website, an institutional repository or funder's repository and make it publicly available immediately.**

# Achieving nanoscale horizontal separations in the standard 2 $\mu\text{m}$ PolyMUMPS process

A. M. Elshurafa · K. N. Salama

Received: 2 December 2012 / Accepted: 7 January 2013  
© The Author(s) 2013. This article is published with open access at Springerlink.com

**Abstract** This paper shares with the research community how to achieve, effectively and easily, lateral submicron separations in the standard 2  $\mu\text{m}$  PolyMUMPS process without any fabrication intervention or post-processing, based on the oxide sidewall spacer technique. Thousands of nanoseparations were created and successfully tested by visual inspection and by a simple capacitance measurement. The lateral separations attained were less than 440 nm and reached as low as 280 nm. To corroborate the findings, measurements were performed on different capacitors fabricated in different fabrication runs with consistent results. This is the first time that submicron lateral distances are reported in PolyMUMPS using the oxide spacer technique.

**Keywords** Capacitor · Fabrication · MEMS · PolyMUMPS · Sacrificial oxide spacer technique

## Introduction

In MEMS, achieving features and/or horizontal separations in the nanorange is very beneficial and, depending on the application considered, provides enhanced performance on different fronts. For example, lateral nanogaps increase the capacitance density of comb drive (variable) capacitors, whereas they increase power handling and reduce phase noise in capacitively transduced resonators (Lin et al.

2005). Many other examples can be easily found in the literature.

Processes with horizontal nanoseparations may use electron beam lithography (EBL) (Henini 1999) or nano-injection lithography (NIL) (Rowland et al. 2005), for example to attain the required resolution. However, both techniques require equipment that may not always be available in academic institutions or small companies. As an alternative, a research group or a company may choose to pay a certain provider for nanoresolution printing, which is surely more expensive than microresolution printing.

To circumvent the financial and technical challenges of attaining lateral separations in the nanoscale, researchers have sought alternative routes that are cheaper and less complex. Shao et al. (2007) for example introduced a method that depends on electrostatic actuation: briefly explained, if two structures are one or two microns away from each other and a DC potential difference is created between them, an attractive electrostatic force causes the structures to move towards each other reducing the gap length, and a carefully placed stopper ensures that both structures do not touch. Although effective, this method requires a constant DC supply, which cannot always be possible for all applications.

On the other hand, Hsu et al. (2001) proposed an intelligent method that requires no advanced lithography, no advanced etching technologies, and no DC biasing. The backbone of this technique is to simply deposit oxide conformally along the top and the sidewalls of an existing structural polysilicon layer. This oxide will play the role of the sacrificial layer that governs ultimately the lateral gap spacing between the already existing polysilicon and the subsequent polysilicon layer that will be deposited.

After its advent, the aforementioned technique, which is usually referred to as the oxide sidewall spacer technique

---

A. M. Elshurafa (✉) · K. N. Salama  
Electrical Engineering Program, Computer, Electrical,  
and Mathematical Sciences and Engineering Division,  
King Abdullah University of Science and Technology (KAUST),  
Thuwal 23955-6900, Saudi Arabia  
e-mail: amro.elshurafa@kaust.edu.sa; elshurafa@ieee.org

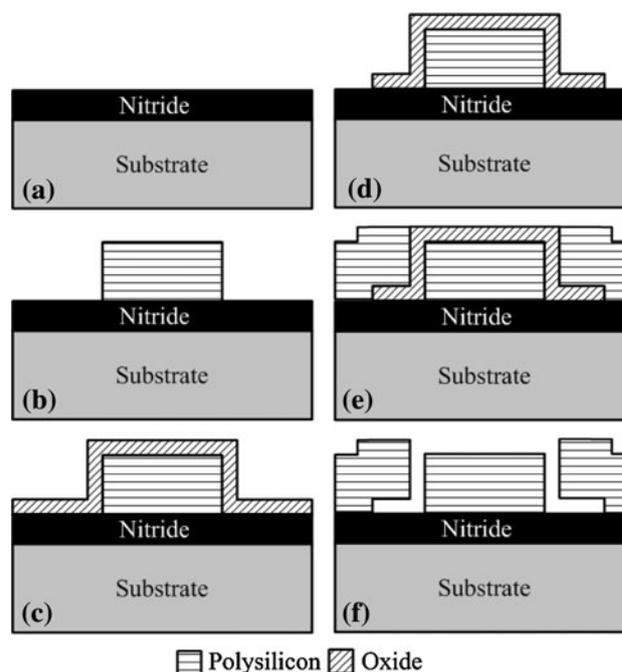
(OSST), has been used in many applications (Clark et al. 2003; Lin et al. 2008; Rocheleau et al. 2012) and was successfully used in attaining lateral dimensions as low as 100 nm. Additionally, this technique has been further enhanced using atomic layer deposition and the lateral spacing was brought down to 10 nm (Cheng and Bhawe 2010). Nonetheless, all the previously reported devices and/or circuits were fabricated in specially developed processes.

From a commercialization standpoint, using specially developed processes poses the usual concerns of repeatability. Hence, in this paper, we study the repeatability of achieving submicron lateral separations in the standard and commercially available PolyMUMPS process (Cowen et al. 2011) provided by MEMSCAP (<http://www.memscap.com>) using the OSST, since this information is lacking in the literature.

The PolyMUMPS process is a standard commercial surface micromachining process that has been under demand since 1992. PolyMUMPS is a very mature and reliable process, and has been used by hundreds of groups in academia, industry, and government institutions worldwide. Explicitly, PolyMUMPS has been used in the development of thermal actuators (Arthur et al. 2011), micromotors (Arthur et al. 2011), cell segregators (Bligh et al. 2008), resonators (Motiee et al. 2006), radio frequency capacitors (Elshurafa et al. 2012c; Elshurafa and Salama 2012; Elshurafa and El-Masry 2010a, b; Motiee et al. 2006), scratch drive actuators (Li et al. 2002), and many other applications. However, the PolyMUMPS design handbook does not provide any information about the OSST. Hence, it is still premature to design any devices using this method because the method itself has not been typically used in the PolyMUMPS process. It would be prudent to focus first on how repeatable the OSST is and provide some reliable information before using this technique in designing any specific device. The latter is the objective of this paper.

#### The oxide spacer technique: overview

The main advantage of the OSST is to easily achieve submicron horizontal gaps without the need for time-consuming and costly lithography. We explain this technique with the aid of Fig. 1, in which we provide a conceptual schematic for a generic process, and ignore processing intricacies such as passivation layers, seed layers, photoresist spinning, baking, etc. Starting with a typical insulator layer (silicon nitride for example) atop a silicon substrate as shown in step 'a', a polysilicon layer is deposited and patterned (step 'b'). Then, a sacrificial oxide layer is deposited (step 'c') and patterned (step 'd'), before the following polysilicon layer is deposited and patterned (step



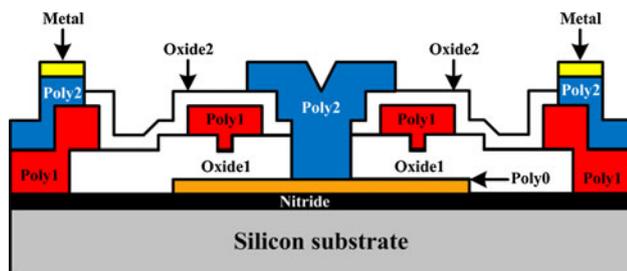
**Fig. 1** Brief illustration of the oxide sidewall spacer technique. Step 'a': start the explanatory process with a typical substrate and an insulating nitride layer; step 'b': deposit and pattern polysilicon; step 'c': conformally deposit oxide; step 'd': pattern oxide; step 'e': deposit and pattern second polysilicon layer; step 'f': wet-etch the sacrificial oxide and end up with the desired geometry

'e'). Finally, the oxide layer is wet-etched and we are left with the desired separation (step 'f'). Note that it is easily possible to have a sacrificial layer deposited right after the nitride to serve as a sacrificial layer for the first polysilicon layer, and for this sacrificial layer to be patterned so that the first structural layer is anchored to the nitride as previously done (Akgul et al. 2009; Hsu et al. 2001; Wang et al. 2003).

With the process shown in Fig. 1, we can infer that the only factor that governs the gap dimension is the ability to control the deposition of the oxide layer, and this surmounts the limitations of lithography and dry etching. Note also that it is desired that the oxide deposition be conformal for better control of its thickness on the sidewalls of the polysilicon (step 'c' in Fig. 1). Nevertheless, conformal deposition is not mandatory and more details will follow shortly.

#### PolyMUMPS overview

Given the relatively detailed explanation of the previous section, we would like to implement this methodology onto the standard, commercially available, PolyMUMPS process. Before that, a brief description of PolyMUMPS is essential. Figure 2 summarizes the layers in PolyMUMPS and most of the possible structural connections and/or



**Fig. 2** The layers of PolyMUMPS right before release with most of the possible connections shown (not drawn to scale)

combinations of layers, in which Poly0, Poly1, and Poly2 are polysilicon structural layers with thicknesses of 0.5, 2, and 1.5  $\mu\text{m}$ , respectively, whereas Oxide1 and Oxide2 are oxide sacrificial layers with thicknesses of 2 and 0.75  $\mu\text{m}$ , respectively.

It is clear how PolyMUMPS allows for flexibility in connecting the layers of PolyMUMPS to each other with anchors, vias, etc. It is for this freedom and flexibility in connecting different layers to each other that there is a plethora of PolyMUMPS papers that have been published in the literature, for a variety of applications as mentioned earlier, with some being complex.

By taking a close look at Fig. 2, we opt to restrict our study on the second oxide layer only for the following reasons: (1) the first oxide layer is 2- $\mu\text{m}$  thick. As such, achieving lateral nano-separations will be extremely difficult if at all possible; (2) the Poly0 layer is only 0.5- $\mu\text{m}$  thick which makes creating a practical device while interacting with Poly0 a difficult task due to its low thickness; (3) the Poly0 is fixed to the substrate, which means that creating moving or vibrating structures will not be possible. On the other hand, and with respect to the second oxide layer, we note that it is already 750-nm thick. Hence, whether the deposition of Oxide2 takes place conformally, the sidewall thickness of this Oxide2 layer created adjacent to the Poly1 layer will be 750-nm thick at most. Further, it is very easy to create structures like fixed-fixed beams, fixed-free beams, disks, etc., and ensure that these structures are capable of being actuated and/or moved.

## Design

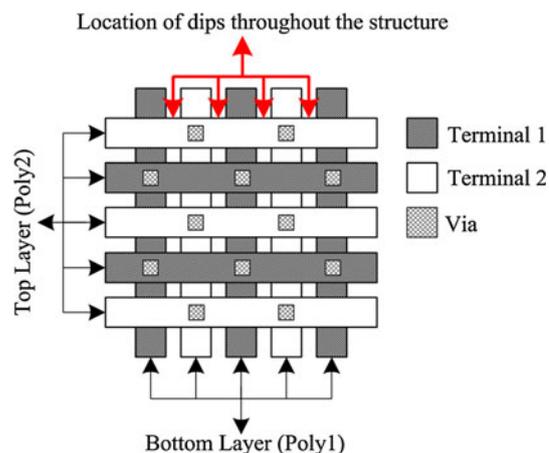
### Structure of choice

The purpose of this paper, as explained in the introduction, is to study the possibility of obtaining submicron lateral separations in PolyMUMPS reliably and repeatably. In order to achieve these goals, a structure that will enable easy visualization of these nanoscale horizontal distances is

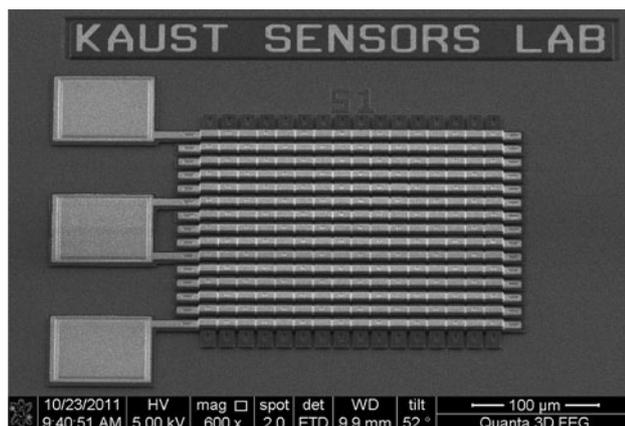
required. Note also that studying these nanoscale separations is being performed without any specific device in mind. It is still early at this stage to think about the possible devices that can benefit from this OSST in PolyMUMPS simply because we are not sure whether this technique will work. Even in the event if it works, we cannot confirm whether this technique is reliable and repeatable. Once the concept is proven, then more application-specific structures with design-of-experiment efforts in mind directed towards a specific device would take place.

In order to test reliability, it is important to create hundreds of these separations. Moreover, it is equally important to verify that these separations exist (i.e., Poly1 does not touch Poly2), such that this verification is not visual because the time required to visually inspect hundreds of separations would be prohibitive. Thus, the capacitor presents itself as an appropriate candidate for the purposes of this paper, since measuring a capacitance value from a capacitor immediately confirms that no shorts exist between the terminals of the capacitor. Creating a capacitor structure that serves the purpose of this paper becomes, now, the challenge.

Starting by some crude and basic designs, searching the literature for capacitor structures, and after some optimization by trial-and-error, we arrive at the woven structure depicted in Fig. 3. As can be seen, the top layer will be created using Poly2/Metal, whereas the bottom layer will be created using Poly1. In order to test the OSST at the extreme case, the horizontal separation between all adjacent Poly1 segments will be 2  $\mu\text{m}$ , which is the minimum allowable separation in PolyMUMPS. At this minimum separation, and after the second oxide layer is deposited, we allow the oxide to create the minimum possible divot (if any). Then, the subsequent Poly2 layer will fill in the void with a dip, and this dip will ideally be, at most, 750 nm



**Fig. 3** A conceptual schematic of the woven structure that will be used to verify the OSST in PolyMUMPS



**Fig. 4** An SEM of one of the fabricated woven capacitors

away from Poly1 at both sides (i.e., left and right). In other words, we test the divot at the extreme case.

#### Acquired results

A scanning electron microscope (SEM) photograph of one of the fabricated woven capacitors is shown in Fig. 4. As can be seen, the capacitor has horizontal segments that are made of Poly2/Metal and these horizontal segments conceal the vertical Poly1 segments under them. Three pads are also clearly visible to the left of the figure and are required for measurement purposes.

In Figs. 5 and 6, sample SEM photographs are provided for two woven capacitors. The first capacitor shown in Fig. 5 possesses horizontal separations between any two adjacent Poly1 segments of 2  $\mu\text{m}$  and possesses horizontal separations between any two adjacent Poly2 segments of 2  $\mu\text{m}$  as well; for convenience, we call this capacitor  $C_1$ . On the other hand, the horizontal separation between any two adjacent Poly1 segments in the capacitor shown in

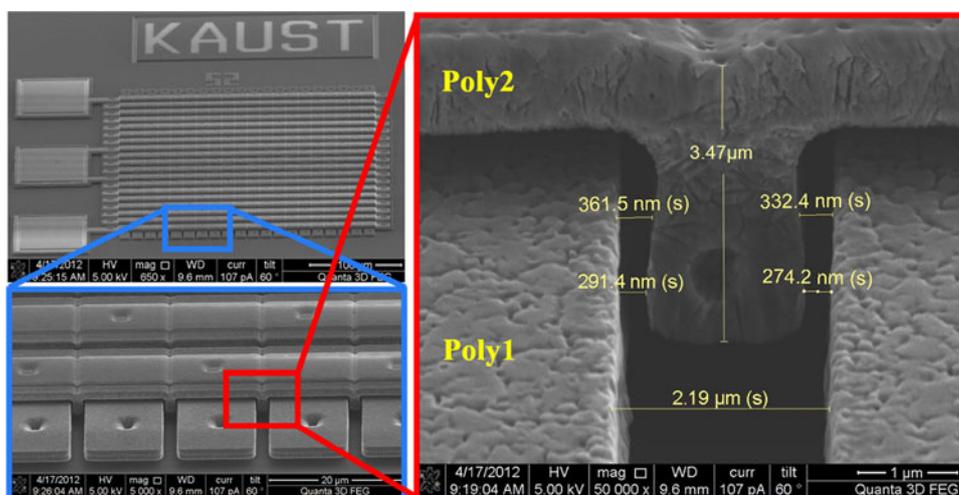
Fig. 6 is 3  $\mu\text{m}$ , and the horizontal separation between any two adjacent Poly2 segments is also 3  $\mu\text{m}$ . We call this capacitor  $C_2$ .

By taking a close look at Figs. 5 and 6, it is concluded that the lateral separations achieved in both cases between Poly1 and Poly2 are less than 500 nm, and this was confirmed by testing tens of other separations visible. Further, we notice that the deposition of the oxide is not fully conformal. The horizontal nanoscale separations in Fig. 5 are in the range of 300 nm, while the separations in Fig. 6 are in the range of 400 nm, and these results are logical and conform to the theory of step coverage (Sze 2008) given that the arrival angle available for the reactants in Fig. 5 is smaller than that of Fig. 6. For  $C_1$ , and after performing tens of measurements, it was concluded that the maximum separation at the top of the dip was 380 nm while the maximum separation at the bottom of the dip was 305 nm. As for  $C_2$ , the maximum top separation was 436 nm, while the maximum bottom separation was 380 nm. Moreover, we can also see that the heights of the dips are 3.47 and 2.71  $\mu\text{m}$  for  $C_1$  and  $C_2$ , respectively and these results are logical, because the separation between two adjacent Poly1 segments is 2 and 3  $\mu\text{m}$  for  $C_1$  and  $C_2$ , respectively, the oxide creates a larger divot in  $C_2$ , and hence, a shorter dip. Further, these dips suggest that the Poly2 layer almost fully faces the Poly1 layer. For completeness, we also include Fig. 7 to show that the nanopacings are also present at the outer edges, and are in the range of 430 nm.

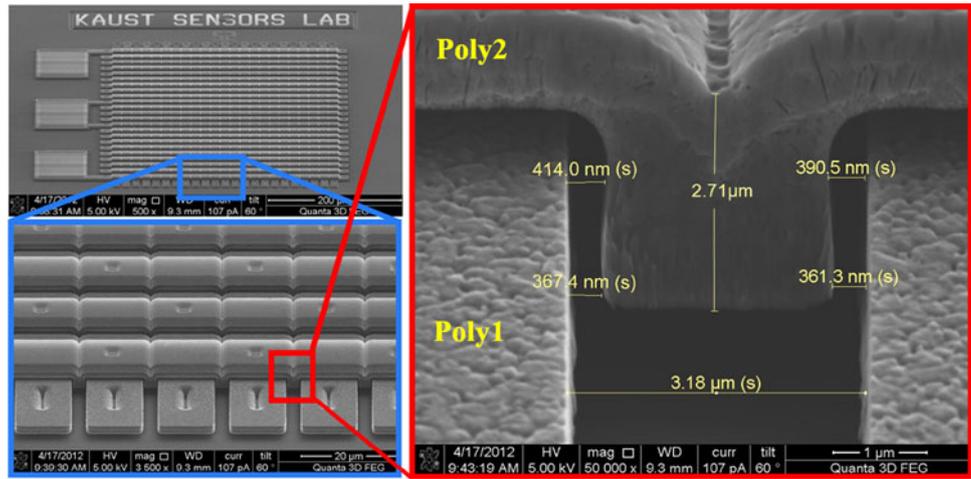
#### Repeatability

Now that we have confirmed that nanoseparations are indeed achievable, we test for repeatability. To begin with, and because we utilized a woven structure, we have already tested hundreds of separations in a single capacitor. Explicitly, the number of divots in  $C_1$  and  $C_2$  is 361 and

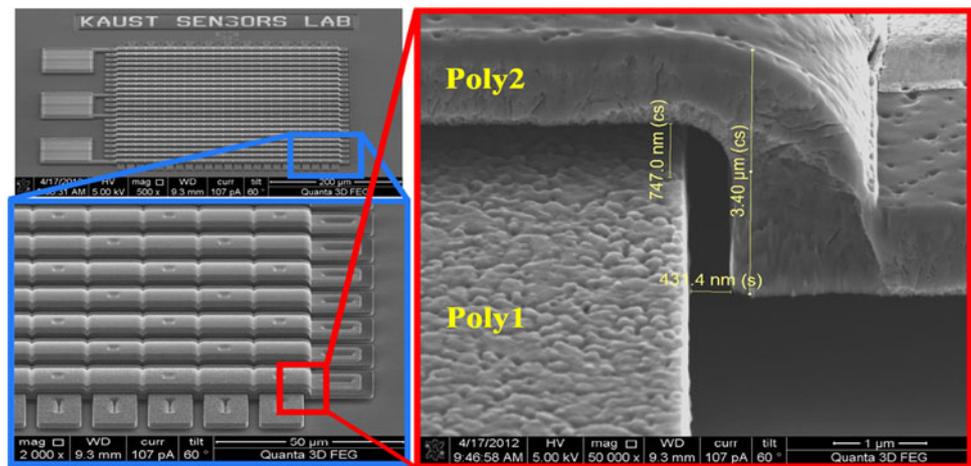
**Fig. 5** One of the fabricated woven capacitors ( $C_1$ ) in which the horizontal distance between any two adjacent Poly1 segments, and between any two adjacent Poly2 segments, is 2  $\mu\text{m}$ . It is clear how the separation between Poly1 and Poly2 is in the 300-nm range



**Fig. 6** Another fabricated woven capacitor ( $C_2$ ) in which the horizontal distance any two adjacent Poly1 segments, and between any two adjacent Poly2 segments, is  $3 \mu\text{m}$ . It is clear how the separation between Poly1 and Poly2 is in the 400-nm range



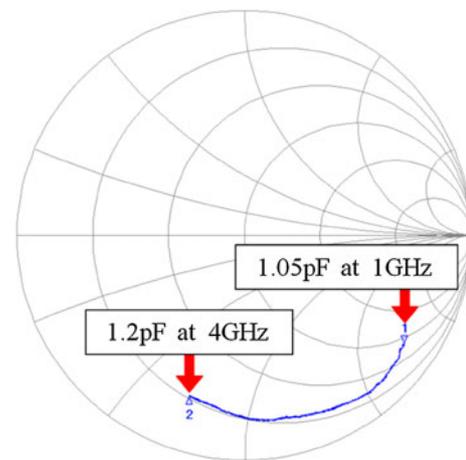
**Fig. 7** Nanospacings present also at the sides of the capacitors



506, respectively, which translates to 722 and 1,012 nanospacings in each capacitor, respectively (each Poly2 dip is separated from Poly1 by a left and right spacings). Because it is not possible to visually test all the divots, we simply measure the capacitance and look out for a short. As a sample measurement, the capacitor shown in Fig. 4 was measured and measurement results, as shown in Fig. 8 via the Smith chart, indicate a capacitance of 1.05 pF at 1 GHz which is on par with other reported PolyMUMPS capacitors (Elshurafa et al. 2012c; Elshurafa and Salama 2012; Elshurafa and El-Masry 2010b; Elshurafa et al. 2012a, b). Since a capacitance is measured, then no shorts exist. Secondly, we fabricated different sizes of the capacitor on the same die. All the capacitors that were tested, with no exception, measured a capacitance, and no shorts were witnessed anywhere.

Finally, and to further corroborate the previous findings, the same capacitors were fabricated on two different PolyMUMPS fabrication runs (i.e., run 95 in April 2011 and run 96 in July 2011). We have witnessed no shorts in all the capacitors that were tested in both runs.

Collectively, there was a total of approximately 21,000 nanospacings tested. We also emphasize that we were unaware of the location of the lots that were assigned to us



**Fig. 8** Smith chart measurement of the woven capacitor to extract capacitance

from MEMSCAP on the wafer during both fabrication runs. Hence, the location of our designs in both runs on the wafer was random. Yet, the results were consistent (the location of the lots is important for residual stress considerations).

As mentioned earlier, the woven capacitor was chosen to demonstrate the reliability and feasibility of obtaining the nanospacings. In other words, the woven capacitor structure was not optimized from a device perspective, but from both a process perspective and an easy-to-test perspective (the capacitance value itself is not of primary interest).

Despite being able to surely obtain submicron separations, this technique in PolyMUMPS lacks accurate control over the separation length, as opposed to previous papers, which performed conformal oxide deposition with some optimization to control the oxide sidewall thickness. In PolyMUMPS, however, the oxide is deposited with a  $\pm 12.5$  tolerance. As such, it is only possible to work with a range rather than a specific value of separation.

## Conclusion

We have shown that achieving lateral nanospacings in the commercially available and standard PolyMUMPS process is indeed achievable and in fact facile. We believe that the results included herein will be of interest to the community especially that PolyMUMPS is a very mature, reliable, and reasonably priced process. The lateral separations attainable ranged from 280 to 440 nm.

**Acknowledgments** The authors thank Dr. Ali Behzad, Mr. Xiang Yu, Dr. Dongku Cha at the Advanced Nanofabrication and Imaging Laboratories in King Abdullah University of Science & Technology (KAUST) for measurement and imaging assistance. The authors also thank Dr. Ian Foulds for fruitful technical discussions.

**Open Access** This article is distributed under the terms of the Creative Commons Attribution License which permits any use, distribution, and reproduction in any medium, provided the original author(s) and the source are credited.

## References

- Akgul M, Kim B, Hung LW, Lin Y, Li WC, Huang WL, Gurin I, Borna A, Nguyen CTC (2009) Oscillator far-from-carrier phase noise reduction via nano-scale gap tuning of micromechanical resonators. In: IEEE Transducers, 2009. IEEE, pp 798–801
- Arthur C, Ellerington N, Hubbard T, Kujath M (2011) MEMS earthworm: a thermally actuated peristaltic linear micromotor. J Micromech Microeng 21:035022
- Bligh M, Stanley KG, Hubbard T, Kujath M (2008) Sorting microparticles into lateral streams using a two-phase rectangular electrokinetic array. J Micromech Microeng 18:045002
- Cheng TJ, Bhawe SA (2010) High-Q, low impedance polysilicon resonators with 10 nm air gaps. In: IEEE MEMS, 2010. IEEE, pp 695–698
- Clark JR, Abdelmoneum MA, Nguyen CC (2003) UHF high-order radial-contour-mode disk resonators. In: IEEE frequency control symposium, 2003. IEEE, pp 802–809
- Cowen A, Hardy B, Mahadevan R, Wilcenski S (2011) PolyMUMPS design handbook—Rev. 13. MEMSCAP Inc., Bernin
- Elshurafa AM, El-Masry EI (2010a) MEMS variable capacitance devices utilizing the substrate: I. Novel devices with a customizable tuning range. J Micromech Microeng 20:045027
- Elshurafa AM, El-Masry EI (2010b) MEMS variable capacitance devices utilizing the substrate: II. Zipping varactors. J Micromech Microeng 20:045028
- Elshurafa A, Salama K (2012) Two-layer radio frequency MEMS fractal capacitors in PolyMUMPS for S-band applications. Micro Nano Lett (IET) 7(5):419–421
- Elshurafa A, Ho P, Radwan A, Ouda M, Salama K (2012a) Low-voltage puzzle-like fractal microelectromechanical system variable capacitor suppressing pull-in. Micro Nano Lett (IET) 7(9): 965–969
- Elshurafa A, Ho P, Salama K (2012b) Low voltage RF MEMS variable capacitor with linear CV response. Electron Lett 48(7): 392–393
- Elshurafa A, Radwan A, Emira A, Salama K (2012c) RF MEMS fractal capacitors with high self-resonant frequencies. Microelectromech Syst J 21(1):10–12
- Henini M (1999) EBL opening up the nano-world. III-Vs Rev 12(6): 18–23
- Hsu WT, Clark JR, Nguyen CTC (2001) A sub-micron capacitive gap process for multiple-metal-electrode lateral micromechanical resonators. In: IEEE MEMS, 2001. IEEE, pp 349–352
- Li L, Brown JG, Uttamchandani D (2002) Study of scratch drive actuator force characteristics. J Micromech Microeng 12:736
- Lin YW, Li SS, Ren Z, Nguyen CTC (2005) Low phase noise array-composite micromechanical wine-glass disk oscillator. In: IEEE electron device meeting, 2005. IEEE, pp 281–284
- Lin Y, Li WC, Ren Z, Nguyen CTC (2008) A resonance dynamical approach to faster, more reliable micromechanical switches. In: IEEE frequency control symposium, 2008. IEEE, pp 640–645
- Motiee M, Mansour RR, Khajepour A (2006) Novel MEMS filters for on-chip transceiver architecture, modeling and experiments. J Micromech Microeng 16:407
- Rocheleau TO, Naing TL, Ren Z, Nguyen CTC (2012) Acoustic whispering gallery mode resonator with  $Q > 109,000$  at 515 MHz. In: IEEE MEMS, 2012. IEEE, pp 672–675
- Rowland HD, Sun AC, Schunk PR, King WP (2005) Impact of polymer film thickness and cavity size on polymer flow during embossing: toward process design rules for nanoimprint lithography. J Micromech Microeng 15:2414
- Shao L, Palaniapan M, Khine L, Tan W (2007) Micromechanical resonators with submicron capacitive gaps in 2 CE<sup>m</sup> process. Electron Lett 43(25):1427–1428
- Sze SM (2008) Semiconductor devices: physics and technology. Wiley, USA
- Wang J, Ren Z, Nguyen CTC (2003) Self-aligned 1.14-GHz vibrating radial-mode disk resonators. In: IEEE Transducers, 2003. IEEE, vol 942, pp 947–950