Ultrafast and Ultralow-Power Voltage-Dominated Magnetic Logic

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To solve the von Neumann performance bottleneck, many kinds of magnetic logic devices are proposed. However, the operation speed, power consumption, and error rate of these devices are incompatible with complementary metal–oxide–semiconductor (CMOS) logic, and moreover, cascading of the devices is difficult. Herein, instead, a new voltage-dominated magnetic logic-memory device is proposed, with switching time of 300 ps and power consumption of 150 fJ, representing ≈ 10 times improvement compared with CMOS logic on the same scale. The device has a reliable output ratio of $>3000\%$, a low working magnetic field of <10 mT, and a low error rate of $\approx 10^{-7}$. Moreover, complex logic operations, such as XOR gates and a full adder, can be realized using this device via cascading. As a result of these advantages, the magnetic logic-memory device is well suited for practical applications.

1. Introduction

Conventional computers are built on devices combining a volatile silicon-based complementary metal–oxide–semiconductor (CMOS) logic processor with external nonvolatile memory. Frequent communication between the logic processor and the memory results in low speed and high power consumption^[1] (the von Neumann performance bottleneck). A promising approach to address this issue is combining reconfigurable logic and built-in nonvolatile memory through the use of magnetic logic^[2], such as magnetic field-controlled logic,^[3] electric field-controlled magnetic logic,^[4–7] magnetic domain-wall (DW) logic,^[8–11] magnetic logic based on magnetic tunnel junctions (MTJs),^[12,13] or the anomalous Hall effect

(AHE).^[14,15] All of these approaches, however, suffer from certain limitations.

Diode-assisted geometry-enhanced low-magnetic-field magnetoresistance in silicon can be used to perform basic Boolean logic operations. The large required magnetic field (0.15 T) limits, however, application of this approach. Magnetic switching can also be controlled using a ferromagnetic/ferroelectric structure^[5] or electrical gating of the oxygen level,^[7] forming electric field-controlled magnetic logic. However, the long times and limited suitability for cascading also make this approach unsuitable for practical applications.^[6,16]

Magnetic DW logic-encoded data and processed logic or memristive operations

with DWs propagating through complex networks of nanowires under the action of an externally applied magnetic field or current have also been investigated.^[8,10] For magnetic logic based on MTJs and Schottky diode-enhanced MTJs, basic logic and arithmetic operations have also been implemented.^[3,12,13]

However, the power demand for magnetic DW logic and MTJ-based logic is determined by the critical current for magnetic switching, as the current in the logic operation is used to drive directly magnetic switching. A DW logic of 1 μm in size has switching time of 6.25 ns and power consumption of 20.4 pJ,^[10] while magnetic logic based on a 40 nm MTJ has a switching time of 1.31 ns and power consumption of 49.6 pJ.^[17]

Luo et al. proposed a form of magnetic logic by coupling the AHE and current-controlled negative differential resistance, thereby realizing in-memory computing.^[15] This device has a long switching time of ≈ 100 ns, arising from the internal turn-on properties of current-controlled negative differential resistance. To address this problem, Pu et al. replaced the current-controlled negative differential resistance with insulator-to-metal transition materials, thereby achieving a reduction in switching time to 7.5 ns.^[14] However, in these devices, the logic output is in the form of the current, and as such it is difficult to perform complex logic operations via cascading. In addition, as the turn-on resistance of current-controlled negative resistance components is large, and the current required for logic operations is large, the switching time is still relatively long, and the power consumption of these devices is high.

To reduce both the switching time and power consumption, the logic operations and magnetic switching should be electrically separated, and the turn-on resistance should be reduced. Moreover, to improve the suitability for cascading, voltage should be used as the output signal instead of current. Accordingly, we

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have investigated the use of voltage-controlled n-type negative differential resistance (NDR), due to its small turn-on resistance and switching time, and the use of Hall voltage, instead of current imbalance, so that the logic operations and magnetic switching can be electrically separated and the required power consumption for the magnetic logic can be dramatically reduced. Based on this approach, we propose in this work an ultrafast and ultralow-power voltage-dominated magnetic logic device. Its switching time and power consumption can achieve values of 300 ps and 150 fJ, representing a ten times improvement compared with CMOS logic devices of the same size.

2. The Switching Time and Power Consumption of Voltage-Dominated Magnetic Logic

We prepared magnetic multilayer films with a structure of Ta (3.5 nm)/CoFeB (1 nm)/MgO (1.3 nm) and patterned these films using photolithography and Ar-ion milling (details given in the Experimental section). The three-terminal magnetic component can be regarded as a Δ -type resistor network (Figure 1a). Because of the AHE, the voltage between the left electrode and the top electrode (V_L) and the voltage between the right electrode and the top electrode (V_R) is unbalanced and magnetism controlled. With magnetization up, V_R is larger than V_L , equivalent to $R_{\text{Right}}^{\text{eff}} > R_{\text{Left}}^{\text{eff}}$. With magnetization down, V_R is smaller than V_L , equivalent to $R_{\text{Right}}^{\text{eff}} < R_{\text{Left}}^{\text{eff}}$. However, the voltage imbalance is extremely small (0.4%, see Section 1, Supporting Information). In our proof-of-concept experiment, we used resonant tunneling diodes and complementary junction field transistors^[18] to enhance this voltage imbalance. We observed magnetism-controlled voltage bifurcation and

accordingly propose a magnetic logic device with reconfigurable logic operations (Section 2, Supporting Information). We experimentally investigated the switching time and power consumption of our magnetic logic device with the electrical method^[19] (Figure 1c, details in Section 3, Supporting Information). Although logic outputs are simultaneously written into the storage bits at the same time as carrying out logic operations, our magnetic logic device can nevertheless be divided into two parts, the logic part and the storage part. The measured switching time of the logic part was 298 ps, which is ≈ 10 times less than that of a CMOS logic device of the same size ($\approx 1 \mu\text{m}$).^[20] The measured switching time of the storage part was < 1 ns. As the logic part and the storage part are connected via a metal-oxide-semiconductor field-effect transistor (MOSFET), the current in the logic operations is isolated from magnetic switching, leading to ultra-low current for logic operations. The power consumption of the device is just 152 fJ (Figure 1c), which is ≈ 6 times less than that of a CMOS logic device of the same size. Our magnetic logic device is therefore able to overcome the problem, whereby power consumption of DW logic and other current-driven magnetic logic are limited by the critical current for magnetic switching. The logic operation error rate of our magnetic logic device was also estimated as 10^{-7} , comparable with that of conventional CMOS logic^[16] (all comparisons of magnetic logic devices and CMOS logic are for devices of similar size of $1 \mu\text{m}$; for further details see Section 5.2 of the Supplementary materials).

The turn-on resistance of n-type NDR is $10\text{--}100 \Omega$, so the turn-on time caused by the junction capacitor and the NDR turn-on resistance in our device is low. In addition, the working frequency resonant tunneling diodes used in our device can achieve values of up to ≈ 1 THz. The logic operations in our device are performed based on Hall voltage instead of magnetic switching or DW

Figure 1. The structure and high-frequency properties of voltage-dominated magnetic logic. a) Schematic of our magnetic device structure. The current–voltage curve of n-type NDR is indicated in the inset. b) Schematic of magnetic logic device with three magnetic bits. The magnetization of each magnetic bit can be switched by a magnetic needle. c) Comparison of the switching time and power consumption of current-driven magnetic logic devices,^[14] CMOS logic circuits,^[17] magnetic DW logic devices,^[9] and our magnetic voltage-type magnetic logic device. All data are collected from devices of $1 \mu\text{m}$ in size.

propagation, so the current used for logic operations is not limited by the critical current for magnetic switching. Therefore, our voltage-dominated magnetic logic can achieve both ultrafast switching speed, while at the same time operating at ultralow power.

3. Logic Operations

3.1. Basic Logic Operations

In our magnetic film, the bottom layer of Ta offers a built-in spin-Hall effect with a spin-orbit torque in the top magnetic layer, making our device capable of electric memory writing.^[21] Two magnetic components (bits a and b) are considered as logic input bits, and one magnetic component, bit c, is considered as a control bit. They are connected in parallel, with a magnetic component, bit d, connected via a MOSFET in the output channel to integrate information writing into our magnetic device (Figure 2a). For the magnetic components' magnetization, directions of down and up are defined as logic inputs of "1" and "0," respectively; for the output voltage level, high and low values are defined as logic outputs of "1" and "0," respectively.

The magnetization of three magnetic components (namely bits a, b, and c) determines the relationship between the effective resistance on the left side ($R_{\text{Left}}^{\text{eff}}$) and the right side ($R_{\text{Right}}^{\text{eff}}$) (Figure S6a, Supporting Information). When $c = "0"$ and bits (a, b) both have logic inputs of "1," then $R_{\text{Left}}^{\text{eff}} < R_{\text{Right}}^{\text{eff}}$, meaning that the left voltage V_{O1} is at a high output voltage level (logic output of "1"). When $c = "0"$ and at least one of the bits (a, b) have a logic input of "0," then $R_{\text{Left}}^{\text{eff}} > R_{\text{Right}}^{\text{eff}}$, meaning that left voltage V_{O1} is at a low output voltage level (logic output "0"). The left

voltage V_{O1} and right voltage V_{O2} satisfy, therefore, the logic operations of AND and NAND, respectively. Moreover, when $c = "1"$ and bits (a, b) both have a logic input of 0, then $R_{\text{Left}}^{\text{eff}} < R_{\text{Right}}^{\text{eff}}$. When $c = "1"$ and at least one of bit a, b is of logic input "1," then $R_{\text{Left}}^{\text{eff}} > R_{\text{Right}}^{\text{eff}}$. Under these conditions, the left voltage V_{O1} and right voltage V_{O2} satisfy the logic operations of OR and NOR, respectively. Therefore, its reconfigurable logic operations with high output ratio $> 3 \times 10^3\%$ can be programmed by manipulation of magnetic bit c (Figure 2c).

In our tests, the output of magnetic bit d was preset as a logic value of "0," simply by a negative current of 1 mA. Using an applied voltage of 0.4 V, the output voltage for a logic output of "1" was > 0.38 V, which is greater than the threshold voltage $V_{\text{GS(th)}}$ of the connected MOSFET, such that the MOSFET was in an "on"-state, with the output current through the magnetic bit d of ≈ 0.9 mA (Figure 2b). Moreover, this output current is larger than the switching current of the magnetic component (≈ 0.7 mA at a magnetic field of 10 mT, Figure 2d). In contrast for a logic output "0," the output voltage was < 0.02 V, which is much smaller than the threshold voltage $V_{\text{GS(th)}}$ of the connected MOSFET, so that the MOSFET remained in the "off"-state. The output current through the magnetic bit d under this condition is ≈ 0 . Therefore, the output voltage for logic output "1" switches the magnetization from up to down (writes a logic "1"), and the output voltage for logic output "0" leaves the magnetization as up (writes a logic "0"). In this process, logic outputs are simultaneously written into the magnetic bits at the same time of the logic operation. This demonstrates that logic and non-volatile memory are closely integrated in our device, making our device a nonvolatile logic-memory device.

Figure 2. Demonstration of magnetism-controlled reconfigurable magnetic logic combined with memory writing. a) Schematic of the magnetic logic device with a magnetic output logic bit d. A fixed magnetic field of 10 mT was applied on the magnetic output logic bits, and V_{DD} was 1 V. b) Current I_O through the magnetic output bit d with the gate voltage V_O of the MOSFET controlled by magnetic output. c) Truth table of reconfigurable magnetic logic. d) Transverse resistance changes with applied current, indicating the spin-orbit switching effect in our device at applied current of ≈ 0.7 mA.

3.2. Complex Logic Operations

In addition to forming the basic logic operations as described earlier, complex logic operations can be also performed by our magnetic logic device. Three parallel-connected magnetic components (Figure 1b) can be considered as a magnetic logic gate controlled by bit c . An XOR gate can be realized by combining two NOR gates with additional MOSFETs (Section 4, Supporting Information), enabling us to construct a full adder by cascading together two XOR gates (Figure 3a). As the logic inputs are the magnetization of the magnetic components and the logic outputs are voltage signals, the XOR gate can be cascaded through two intermediate magnetic bits (bit I_i and bit $\bar{I}_i$ in Figure 3) instead of being cascaded directly. To demonstrate this possibility, a XOR operation of bit A_i and bit B_i was performed and the results were

written into intermediate bit I_i and bit $\bar{I}_i$ as a first step. The XOR operation of bit C_{i-1} and bit I_i was then performed and the result was written into bit S_i in a second step, representing the “sum” operation of a full adder (see inset in Figure 3a). Moreover, the “carry” operation of a full adder can also be achieved by a magnetic logic gate (Figure 3b). To further demonstrate the potential of this magnetic logic device, a control circuit was applied to the full adder, thus allowing the operations mentioned earlier to be processed automatically, controlled by a clock pulse generator (Section 4, Supporting Information). It can be seen, therefore, that the full adder operation was realized (Figure 3c), and that the circuit demonstrates the possibility for cascading complex logic devices by use of our magnetic logic device.

The magnetic component of our magnetic logic device could be scaled down to ≈ 20 nm in size with stable perpendicular

Figure 3. Scheme of the magnetic full adder circuit. a) Sum operation and b) carry operation. Where two lines with different color intersect, the two lines are not connected (except for connection to the MOSFET); where two lines with the same color intersect, the two lines are connected. c) Truth table for the magnetic full adder.

magnetic anisotropy^[22] and work at a high frequency in the GHz range.^[23] Resonant tunneling diodes can also be minimized and their working frequency can achieve THz values.^[24] Furthermore, instead of “fixed” n-type NDRs and magnetic components, shared n-type NDR and target magnetic components can be utilized and connected by the control unit in the circuits, reducing the number of n-type NDRs and magnetic components used for computation (Section 5.3, Supporting Information).

4. Conclusion

In summary, to overcome the disadvantages of existing magnetic logic devices, we combined n-type NDR components with Ta/CoFeB/MgO multilayers to realize a magnetic logic memory device with reliable output ratio >3000%, low error rate ($\approx 10^{-7}$), a low working magnetic field (<10 mT), excellent high-frequency performance (switching time = ≈ 298 ps), and low power consumption (150 fJ). These performance values are comparable with those for CMOS logic devices of the same size.^[17] Furthermore, the logic operation and magnetic switching in our device can be performed simultaneously, while remaining electrically isolated, so that the current required for logic operations is not limited by magnetic switching. Moreover, complex logic operations, such as XOR and a full adder, can be achieved by cascading our magnetic logic gates. The features make our magnetic logic-memory device suitable for practical applications. If we can improve the structure of our device and realize field-free spin-orbit torque switching through symmetry breaking,^[25] the 10 mT magnetic field can also be eliminated.

5. Experimental Section

Thermally oxidized Si wafers with SiO₂ layer of 300 nm in thickness were used as substrates for magnetic thin films. Magnetic multilayer films with a structure consisting of Ta (3.5 nm)/CoFeB (1 nm)/MgO (1.3 nm) were prepared using a sputter system (Rotaris, Singulus). The samples were deposited at room temperature with base pressure lower than 8.0×10^{-9} mbar. Deposition of SiO₂ with 5 nm thickness was used as a top layer for each sample. During deposition, the gas atmosphere was argon, with flow rate of 55 sccm, and the process pressure was 3×10^{-3} mbar. All samples were annealed at 300 °C for 1 h in vacuum ($< 5 \times 10^{-7}$ mbar). To fabricate the large magnetic component (10 μ m width), magnetic multilayer films were patterned using photolithography followed by Ar-ion milling. To fabricate the small magnetic component (1 μ m width), electron beam lithography was used instead of photolithography. Before deposition of Ti (10 nm)/Au (50 nm) electrodes, slight plasma cleaning was used. For the n-type NDR component, commercially available junction field transistors or resonant tunneling diodes were connected in the printed circuit board.^[15] The magnetic components and the N-type NDR component were connected using ultrasonic wire bonding. Voltage pulses with a width of 100 ms were used for magnetic transport measurements. An external magnetic field was supplied by a self-designed electromagnet. All measurements were conducted at room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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