Tunable, Asynchronous, and Nanopower Baseband Receiver for Charging and Wake-up of IoT Devices

Ahmed Abed Benbuk, *Student Member, IEEE*, Nour Kouzayha, *Member, IEEE*, Joseph Costantine, *Senior Member, IEEE*, and Zaher Dawy, *Senior Member, IEEE*

Abstract—This paper proposes a novel ultra-low power, tunable, and asynchronous baseband architecture for joint radio frequency (RF) wake-up and charging receivers. The designed system switches between the wake-up and charging operations based on the type of the received RF signal. To our knowledge, the proposed system is the first of a kind that introduces multiple power states to reduce the energy consumption by sequentially activating minimal components required for RF wake-up or charging. The fabricated prototype, using off-the-shelf components, features a sensitivity of -40 dBm, a bit rate of 500 bps, and a current consumption of 225 nA at a bias voltage of 2.6 V in the listening state. Current consumption is estimated at 3.225 μ A and 13.725 μ A while processing the preamble and bit sequence, respectively. The address detector is powered OFF during charging to reduce the system's current consumption to 150 nA. Our experimental results show that shutting down the address detector during charging reduces charging time and allows charging from received power levels that are as low as -6 dBm. We demonstrate that, operating the detector with multiple power modes reduces its current consumption and enhances its noise immunity when compared to conventional address detectors with two power modes of operation.

Index Terms—RF wake-up, ultra-low-power, multi-power-mode, address detector.

I. INTRODUCTION AND BACKGROUND

THE swift adoption of Internet of Things (IoT) is enabling new applications in health, agriculture, and industry by transforming ordinary objects into autonomous devices capable of exchanging information [1]. Deploying IoT devices in hard-to-reach and hazardous locations poses formidable challenges. A particular concern is maintaining a reliable source of energy and minimizing power consumption [2]. Radio Frequency (RF) energy harvesting has emerged as a solution to satisfy energy requirements, thanks to the prevalence of ambient wireless signals [3]. Still, the energy extracted from ambient RF sources is limited and requires careful management to eliminate unnecessary drain [4].

A common approach to reduce the power consumption of IoT devices is operating them for a short time in pre-defined,

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The authors are with the Department of Electrical and Computer Engineering, American University of Beirut, Beirut 1107 2020, Lebanon. Nour Kouzayha is also with King Abdullah University of Science and Technology (KAUST), Saudi Arabia. (email: {ajb09, nhk16}@mail.aub.edu, {jc14, zd03}@aub.edu.lb).

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Fig. 1. Generic structure of wake-up receiver designs in the literature.

reoccurring schedules, i.e., by relying on duty cycling [5], [6]. This method significantly decreases the power consumption outside of the scheduled operating windows. However, it suffers from the drawbacks of idle listening and high latency [7]. Wake-up receivers (WuRx) [8] [9] have been proposed to address these issues by allowing power-hungry components to remain inactive during idle times [10]. The design of wake-up receivers presents many challenges and trade-offs. Strict power constraints limit their ability to listen to and process coded messages [7]. Furthermore, ambient noise poses a problem as it leads to false wake-ups and increased power consumption.

The available RF wake-up methods follow diverse techniques that target different components in the receiver chain, seen in Fig. 1. Nevertheless, all efforts converge to the single goal of offering enhanced performance at a reduced power consumption. For example, the power consumption of the WuRx in [11] is reduced by 29% by lowering the Low-Noise Amplifier (LNA) gain during the listening. On the other hand, the work in [12] uses a passive, high-Q transformer/filter to achieve a passive gain of 25 dB.

Multiple efforts target power savings in the baseband. A conventional WuRx baseband architecture is shown in Fig. 2.a. The received signal is demodulated by an envelope detector and a data slicer, and a correlator examines the serial bit sequence. The correlator is either permanently powered ON [12]–[20], duty-cycled [6], or placed in a low power mode [21]–[26]. Additionally, a local oscillator generates the clock required for synchronization [6], [12]–[16], [18], [20], [21]. A common baseband implementation is presented in [22], where a microcontroller is used as a bit correlator. The design has a power consumption of 152 nW and 63 μ W in the listening and active states, respectively. A preamble detector is used for interference rejection and to avoid false trigger of the microcontroller. In [23], a combined RF energy harvester and WuRx uses the harvester as a demodulator, allowing the transmitter to encode a wake-up signal while charging the receiver's battery. The circuit in [25] is similar to [22] and [23] by implementing a noise-filtering preamble detector. The

Fig. 2. (a) A conventional wake-up baseband architecture. (b) Proposed architecture offering combined wake-up/harvesting, coded preamble detector, clock extraction, and ON/OFF switching of baseband components.

bit sequence is decoded by a Serial Peripheral Interface (SPI) driver that communicates with a microcontroller at low power mode 3 (LPM3), consuming only 2.7 μ W.

Combining the WuRx with an energy harvester offers the advantage of using a single antenna and rectifier for both tasks [27]. However, it adversely impacts performance due to loading the receiver [10]. The authors in [10] suggest isolating a 2.4 GHz transceiver from harvesting by relying on the difference between the receive and harvesting power levels. Nonetheless, it is challenging to use this approach when harvesting from low power levels [9]. Moreover, the combined structure complicates the task of interference avoidance since the rectifier's output voltage represents added noise for the baseband [25]. The added noise activates the bit correlator [22], [25] or causes a false wake-up of the IoT device [22], [23], [25]. The available solutions implement a preamble detector for interference avoidance [21], [25] or synchronization [6], [11], [16], [21], [28], but do not consider the preamble's potential for carrying instructions. The coded preamble concept has been suggested to enhance the wake-up signal's data delivery efficiency and improve noise immunity [29]. Additionally, some designs implement external clock extraction to reduce the power consumption [5], [30], [31].

This paper proposes a novel baseband architecture for wake-up receivers that share a rectifier with a harvesting system. The architecture of the suggested approach is shown in Fig. 2.b. The rectifier's output is harvested to charge the energy storage, and the stored energy is used to power an IoT device. The receiver baseband is powered by an independent battery to ensure a stable, continuous power source. It can also be configured to share the energy storage element with the IoT device. In addition, baseband threshold detection is used for harvesting/receiver switching. We implement multiple power states to reduce the average current consumption by activating the minimal components required for processing the wake-up signal. The system supports clock extraction, and contains a coded preamble detector for an enhanced noise immunity and addressing capability.

The paper's contributions are as follows:

- Design, implement, and test a novel address detector for IoT devices that leverage a combined RF harvesting and wake-up ability. The circuit achieves a -40 dBm sensitivity without an active RF amplification stage and features a bit rate of 500 bps and a current consumption that is as low as 225 nA in the listening state.
- Design and implement a coded preamble detector that enhances the address detector's data delivery efficiency and immunity against interference. The coded preamble precedes the bit sequence and can be used to extend the addressing range or implement advanced techniques, such as multicast addressing capability [32].
- Propose multiple power states to reduce the average current consumption. The detector sequentially activates the minimum components required to process the wake-up signal, consuming only 225 nA during listening. To the best of our knowledge, this work presents the first of a kind design that maintains the bit correlator powered OFF while processing a coded preamble.
- Realize an asynchronous solution by extracting the bit correlator's clock from the PWM-modulated bit sequence, removing the need for a local oscillator and bit oversampling that is implemented in most other solutions.
- Provide an analytical assessment of the designed circuit's operation. The results indicate that introducing multiple power states reduces the detector's average current for any application scenario involving wake-up and charging. It has also been shown that operating in multiple power states enhances the detector's noise immunity when compared to traditional designs in the literature.

The rest of this paper is organized as follows: Section II presents an overview of the system components and describes the address detector's power modes. In Section III, we provide a detailed description of the system at the circuit level. Section IV describes the fabrication, testing, and experimental verification of a prototype using off-the-shelf components. Section V provides an analytical study to determine the average current consumption under noiseless and noisy environments. In Section VI, we provide a comparison with similar designs in the literature. Finally, conclusions are drawn in Section VII.

II. SYSTEM DESCRIPTION

A. System block diagram

1) *Transmitter operation:* A block diagram of the overall system is shown in Fig. 3. The transmitter is composed of an RF signal generator and an antenna. It operates by switching between continuous charging signals and modulated wake-up signals, as seen in Fig. 4. The figure shows an example of a wake-up signal (WuS) composed of a coded preamble followed by a bit pattern of (1011). The WuS is composed of the following elements:

- A coded preamble generated by a signal burst at f_0 GHz that lasts for a specific duration. The preamble is demodulated at the receiver into a pulse with a specific width that determines its unique value.

Fig. 3. System block diagram [33].

Fig. 4. Charging and wake-up signals transmitted by the WuTx. The WuTx can switch between the two operating modes by transmitting continuous and modulated signals [33].

- The preamble is followed by a guard time with a period of g_1 [seconds].
- An 8-bit sequence composed of PWM-modulated bursts at f_0 GHz with two distinct periods representing the bit 0 and bit 1.
- The bit bursts are separated by a guard time with a period of g_2 [seconds].

The address is designed such that the preamble is large when compared to the bit sequence.

2) *Receiver operation:* A wake-up receiver (WuRx) is implemented at the receiver side to process the WuS. An address detector examines the demodulated WuS to wake-up the IoT device. The detector generates a trigger only if the following two conditions are satisfied:

- The width of the demodulated preamble matches the value configured in the WuRx's hardware.
- The bit pattern following the preamble matches the value tuned in the WuRx's hardware.

The receiver uses the same antenna for harvesting and wake-up functions. The antenna is followed by an impedance matching network and a rectifier that converts the input signal to DC voltage to power the IoT device. The rectifier functions as a demodulator that converts the received WuS into digital pulses, as shown in Fig. 4. Furthermore, it converts the input power to a voltage accumulated in an energy storage element via a passive power management unit (PMU) that we designed and tested in [9]. The PMU is always operating and it charges the energy storage whenever the input power level exceeds a minimum threshold. An address detector is implemented at

TABLE I
ADDRESS DETECTOR POWER STATES.

State	Active Components
Listening	Data slicer; Auto-power off; RX/harvesting switch
Processing Preamble	+ PWD
Processing Bit Sequence	+ Bit correlator
Charging	RX/harvesting switch; Data slicer

Fig. 5. Address detector block diagram.

the receiver to trigger the IoT device when it receives a wake-up signal with the correct address. The antenna, rectifier, and address detector form a wake-up receiver (WuRx). Unlike the power management unit, the address detector is an active component with an independent power source, and therefore must be kept in a low-power mode to reduce its power consumption. The address detector receives demodulated wake-up signals, continuous charging signals, and noise signals. It must operate with minimal power to process wake-up signals, switch OFF when receiving continuous charging signals, and demonstrate high noise immunity.

B. Address detector block diagram and power states

The address detector is composed of several units to process the WuS and control power delivery to active components. Fig. 5 shows the architecture of the address detector. Two units are responsible for examining the WuS: A pulse width detector (PWD) that we designed and tested in [34] and [9] processes the width of every incoming pulse from the data slicer, and a bit correlator examines the received bit sequence. The circuit remains in the *listening* state when no signal is received from the rectifier and reduces its current consumption to the nano-amp range. The data slicer, auto-power off unit, and the threshold detector remain powered ON in this state, as shown in Table I.

The data slicer converts the rectifier's output into digital pulses when the input power level exceeds its minimum threshold. Furthermore, the auto-power off unit constantly monitors the output of the data slicer. It generates a positive control signal to connect power to the PWD through power

Fig. 6. Address detector power consumption states. The circuit constantly spins in a power state machine to reduce the average current consumption.

switch S_1 when a signal exceeding the data slicer's minimum sensitivity is detected. The circuit moves to the *processing preamble* state as shown in Fig. 6 to determine if the width of the pulse generated by the data slicer matches the configured preamble width. The PWD generates a positive control signal to connect power to the bit correlator through power switch S_2 if the received pulse width matches the configured value. The circuit moves to the *processing bit sequence* state when the bit correlator is powered ON, as demonstrated in Fig. 6. Conversely, the circuit returns to the listening state if the received pulse is not matched.

In the processing bit sequence state, the bit correlator inspects the bit sequence to determine if it matches the tuned sequence. The current consumption of the address detector reaches its peak value at this state because all components are active, as seen in Table I. The bit correlator generates a trigger to the IoT device when the bit sequence is matched. The PWD and bit correlator are powered OFF after the detector generates the trigger because the auto-power off timer is configured to automatically disconnect power from the PWD after a configurable period, as will be shown in Section III.

The voltage threshold detector operates as an RX/harvesting switch by constantly monitoring the output of the data slicer to determine if the address detector must be shutdown during charging operations. It generates a negative control signal to disconnect power from the auto-power off circuit through the power switch S_3 when its threshold is exceeded. The circuit moves to the *charging* state and remains in this state if the voltage sampled from the data slicer remains above the threshold detector's configurable threshold. By shutting down the auto-power off timer, the address detector is effectively disabled, and the detector reduces its current consumption to the nano-amp range. The threshold detector's sample voltage decreases after the continuous signal is removed and the circuit returns to the listening state after charging.

The circuit keeps switching its power mode between the states shown in Fig. 6 for any signal generated by the data slicer. Nevertheless, it is configured to always return to the listening state and remain in this state if the data slicer does not generate any pulse for a configured period. The circuit implementation is described in details in Section III.

III. CIRCUIT DESCRIPTION

A. Operation in the listening state

The circuit diagram of the address detector, highlighting its different units, is shown in Fig. 7. In addition, the figure shows the status of the three power switches ($S_1 - S_3$) in each power state. The address detector operates in the listening state while the input signal level is below the data slicer's minimum threshold. The data slicer converts the rectifier's output voltage at point (1) in Fig. 7 into digital pulses. The data slicer and the RX/harvesting switch remain powered ON in all states. The data slicer is implemented using a nanopower comparator C_1 [35]. Its negative input is configured with a threshold using the voltage divider of R_9 and R_{10} which determines the address detector's sensitivity. The threshold is set to the minimum offset voltage to maximize the detector's sensitivity, while remaining above the comparator's hysteresis voltage. The data slicer's sensitivity is also impacted by temperature variations. At 25° C the comparator's minimum input offset is ± 3 mV which increases to ± 22 mV when the temperature is above 100° C. In our previous work [34], we found that operating the circuit in a noisy environment leads to a higher average current consumption and false wake-up probability. Therefore, the data slicer can be configured with an adaptive threshold to enhance the noise immunity of the circuit when implemented in noisy environments [28].

B. Operation in the processing preamble state

The circuit moves to the processing preamble state when a pulse appears at the output of the data slicer. The R_7C_1 circuit (see Fig. 7) charges on the output of the data slicer, and power is connected to the PWD through power switch S_1 when the accumulated voltage exceeds the auto-power off timer's threshold (see Fig. 8, at time t_2). The auto-power off timer's threshold is configured to a value that is below the D-latch threshold of 1.2 V to connect the source power to the D-latches when the preamble is received. Fig. 8 exhibits a logic diagram of the PWD operation during the processing preamble state. The voltage at R_7C_1 exceeds the threshold of D-latch D_1 and the voltage at $R_{11}C_4$ remains below the threshold of D-latch D_2 only when the tuned pulse width is received. D-latches D_1 and D_2 [36] generate a value of 1 and 0 at their respective output Q-pins at time t_3 . The 1 and 0 values appear at the XoR gate [37] at time t_4 and the PWD outputs a control signal that activates power switch S_2 . The PWD can be tuned to detect different widths by varying the values of the R_7C_1 and $R_{11}C_4$ circuits [9] [34] [38].

The process shown in Fig. 8 is repeated for every pulse received by the PWD. The PWD's output controls the power delivery to the bit correlator through S_2 . Therefore, it must remain high when processing the bit sequence. To avoid switching the PWD output from high to low when the first bit is received, an RC circuit is connected to the EN pins of D_1 and D_2 . The D-latches are only enabled if the voltage at R_8C_3 exceeds the threshold (see Fig. 8, at time t_2). The value of R_8C_3 must be large enough to avoid enabling the D-latches when the bit sequence is received after the preamble. On the other hand, it should remain small enough to enable

Fig. 7. Address detector circuit schematic. The detector is powered by an LiR2032 battery. The harvested energy can be used to power an IoT device.

Fig. 8. Logic diagram of PWD detection of coded preamble showing the input pulse and states of the EN pins of D-latches D1-4 and their outputs Q1-4. A control signal is generated at the output of the XoR when the pulse width is matched.

the D-latch when the preamble is received. The bit sequence is composed of pulses with a shorter period than the shaded area (between time t_1 and t_2).

C. Operation in the processing bit sequence state

In the processing bit sequence state, all units in the address detector are powered ON. The bit correlator demodulates the PWM-modulated 1- and 0-bits and their values are recorded in parallel in a shift register [39] that can store up to 8 bits. A demodulator composed of the $R_{15}C_5$ circuit and one active component, inverter N_2 , is connected to the serial port

Fig. 9. Demodulator operation. The received bit sequence (Signal (1), Fig.7) is demodulated into a voltage level on the $R_{15}C_5$ circuit. The clock is generated by inverting the input signal using inverter N_2 .

of the shift register. Clocking is extracted from the PWM-demodulated bit sequence by inverting the signal using inverter N_2 , as shown in Fig. 9. The value recorded on $R_{15}C_5$ is pushed to the serial port after the bit is removed, i.e. at the start of the guard time g_2 , and the value of g_2 is selected such that the $R_{15}C_5$ fully discharges before the following bit is received. The $R_{15}C_5$ voltage remains below the threshold of the shift register's serial port when a 0-bit is received, but it exceeds the threshold when a 1-bit is received. Logic gates are connected to the shift register's parallel output to generate a trigger when the bit sequence is matched. The R_7C_1 circuit discharges after generating a trigger, and the detector returns to the listening state. The charging constant of R_7C_1 must be large enough to avoid switching OFF the receiver during WuS detection, and the discharging constant must be small enough to reconnect the receiver after the charging task is completed.

D. Operation in the charging state

The address detector is configured to shut down the PWD and the bit correlator during charging operations. Upon charging, the voltage on R_2C_2 exceeds the threshold of the RX/harvesting switch configured on the negative input of comparator C_3 . The switch is a threshold detector configured

Fig. 10. Fabricated Prototype including a) Pulse width detector [9]. b) Bit correlator and c) Power management unit [9].

with negative logic. It disconnects power from the auto-power off circuit when the threshold is exceeded. Therefore, the address detector maintains minimal active components, the data slicer and the RX/harvesting switch during charging. The threshold of RX/harvesting switch is configured such that the switch does not disconnect during WuS reception. The R_2C_2 circuit discharges after the transmitter completes the charging operation, allowing the address detector to return to the listening state.

IV. EXPERIMENTAL RESULTS

The harvester must maintain passive operation, while the power consumption of the wake-up circuitry must be a few orders less than the IoT device. In addition, the stored energy should be adequate to power the IoT device during one operation cycle. In [40], it was shown that a 100 μ F capacitor can be used to power an ultra-low-power microcontroller.

A. Rectifier and Power Management Unit (PMU)

The fabricated rectifier is characterized by an efficiency of 58% at an input power of 0 dBm and maintains flat efficiency around 50% for a frequency range of 2.3-2.5 GHz [41]. The PMU is realized in a BQ25570 from Texas Instruments [42] which supports Maximum Power Point Tracking (MPPT) and can initiate charging from an input voltage level as low as 700 mV. The PMU circuit is described in detail and experimental results are provided in [9]. The rectifier and PMU do not require an active biasing source to operate, thus keeping the harvesting part entirely passive.

B. Current consumption, sensitivity, and data rate

The address detector is fabricated on an FR4 substrate, and it is shown in Fig. 10. The prototype operates at a bias voltage of 2.6 V and is powered through a single LIR2032 battery. Our previous work [9] demonstrated that the address detector circuit is characterized by a sensitivity of -40 dBm when combined with the rectifier designed and implemented in

Fig. 11. Allocation of the total current consumption between various components.

TABLE II
COMPONENT VALUES OF FABRICATED PROTOTYPE.

Component	Value
Data slicer	
R_9	1 k Ω
R_{10}	120 Ω
Auto-power off	
R_5	10 k Ω
R_6	8.2 k Ω
PWD	
R_7	13.8 k Ω
R_{11}	2.24 k Ω
R_8	45 k Ω
$C_1; C_3; C_4$	15 μF
$R_{12}; R_{13}; R_{14}$	100 k Ω
RX/harvesting switch	
R_2	45 k Ω
C_2	15 μF
R_4	100 k Ω
R_1	15 k Ω
R_3	10 k Ω
Demodulator	
R_{15}	1 k Ω
C_5	1.5 μF
R_{16}	15 k Ω

[41]. In [9], we show that the combination achieves a wake-up distance of 27.5 meters at a transmit power of 15.4 dBm. In this work, we extend the addressing range by adding a PWM demodulator and introduce multiple power operating modes. In addition, we introduce the ability to shutdown the address detector during charging.

The designed multi power state system leads to a significant reduction in the circuit's current consumption. Fig. 11 demonstrates the distribution of the maximum current consumption of $I_{max} = 13.725 \mu A$ realized during the processing bit sequence state where all units are activated. The bit correlator contributes to 76.3% of I_{max} . Therefore, shutting down the bit correlator offers major power savings. The current consumption is reduced to 225 nA during the listening state. This value amounts to a decrease of 98% from the processing bit sequence state. Furthermore, implementing a coded preamble enhances noise immunity by avoiding the activation of the bit correlator component whenever the input signal level exceeds the circuit's minimum threshold. The circuit switches to the processing preamble state with a moderate current

consumption, amounting to less than 25% of I_{max} to detect the input pulse width instead of immediately activating the bit correlator. All reported current consumption values are taken at room temperature, which was almost constant, as the variation of temperature can significantly impact the overall current consumption. Because our design relies on a passive RF front end, the baseband contributes the most to overall current consumption. The baseband's current consumption can be significantly reduced in a fully integrated CMOS implementation [12] [18], which is beyond the scope and objectives of this work.

The data slicer introduces a limit on the address detector's maximum data rate due to the slow response time of the comparator [35] to the input signal's rise and fall. The slow response negatively affects the integrity of the demodulated preamble pulse width and bit sequence. Specifically, the slow response time causes a widening of the data slicer's output for input pulses with fast rise and fall time. The minimum detectable input pulse width is experimentally found to be 200 μ sec so the 0- and 1- bits can be modulated as a 250 μ sec and 500 μ sec pulses, respectively. In addition, a minimum guard time of $g_2 = 3t_{bit} = 1.5$ msec is required to fully discharge the $R_{15}C_5$ circuit, where t_{bit} represents the duration of the 1-bit. Therefore, the system can achieve a maximum data rate of $\frac{1}{(0.5+1.5) \text{ ms}} = 500$ bps.

C. Pulse width detection and PWM demodulation

Fig. 12. PWD Operation. The pulse width detection is performed by varying the values of R_7C_1 and $R_{11}C_4$. The D-latches have a threshold of 1.2 V at a bias voltage of 2.6 V.

The PWD shown in Fig. 10.a can be configured to detect any desired pulse width by tuning the values of $\tau_1 = R_7C_1$ and $\tau_2 = R_{11}C_4$. For example, we tune the PWD to detect a preamble with a width of 100 μ sec by setting the values as seen in Fig. 12. When the preamble is received, the EN pins are activated and 1- and 0- bits are stored in D_1 and D_2 , respectively. The stored bit values are delivered to the XoR gate and the PWD generates a high edge.

Fig. 13. PWM bit demodulation. The bit value is determined by the voltage value recorded on $R_{15}C_5$. The RC value is selected such that the recorded voltage exceeds the shift register's threshold when a 1-bit is received, and remains below it when a 0-bit is received.

TABLE III
WAKE-UP SIGNAL TUNING OF THE FABRICATED PROTOTYPE

Component	Value
Preamble	300 ms
Guard time g_1	300 ms
Guard time g_2	40 ms
1-bit	10 ms
0-bit	3 ms

Fig. 13 demonstrates passive demodulation of the PWM-modulated bits using the $R_{15}C_5$ circuit and clock extraction from the received input signal. The input signal is received at a frequency of 20 kbps. The demodulated bit values are stored serially in a shift register as shown in Fig. 7 at the clock's rising edge. The parallel output of the shift register is connected to re-configurable digital gates to generate a high edge when the correct bit pattern is received. The value of g_2 is large to fully discharge the voltage recorded on $R_{15}C_5$ before demodulating a subsequent bit.

D. Multi-power state operation

Multi power state operation is demonstrated by tuning the address detector to the WuS with the specifications provided in Table III. the circuit is configured with the values shown in Table II to generate a trigger when that WuS is received.

Fig. 14 exhibits the detection of the WuS and the generation of a trigger when the preamble and the bit pattern are matched. The bit sequence is terminated with a 0-bit because the bit correlator unit [39] contains a storage register that lags one clock cycle behind the shift register. Signal (1) in Fig. 14 shows the detector operating in the listening state before receiving a WuS with the specifications in Table III. The auto-power off circuit connects power to the PWD as seen in Signal (2) and the detector moves to the processing preamble state. Signal (3) shows connecting power to the bit correlator after the preamble is fully received, at the start of g_1 . In the processing bit sequence state, the bit pattern is correlated and

Fig. 14. Address detector operation: Tuned wake-up signal. Signals are measured in positions (1)-(5) in Fig. 7

Fig. 16. Address detector operation: Erroneous bit sequence. Signals are measured in positions (1)-(5) in Fig. 7

Fig. 15. Address detector operation: Erroneous preamble. Signals are measured in positions (1)-(5) in Fig. 7

Fig. 17. Address detector operation: Continuous charging signal. Signals are measured in positions (1)-(5) in Fig. 7

a trigger is generated when this bit sequence is matched, as seen in Signal (4). The detector returns to the listening state after generating a trigger. The R_7C_1 circuit discharges and power is disconnected from the PWD and the bit correlator. Signal (5) shows the output of the RX/harvesting switch. It can be seen that the output remains high, indicating that the auto-power off circuit is powered.

The address detector moves to the processing preamble state then goes back to listening state if the preamble is not matched. This is shown in Fig. 15 where a preamble with a larger width (400 msec) is received. The address detector switches to the processing preamble state as the previous case in Fig. 14. However, since the preamble width is not matched, no control signal is generated by the PWD to power the bit correlator, and the address detector moves back to the listening state. On the other hand, Fig. 16 exhibits receiving a WuS that begins with the correct preamble followed by an erroneous bit sequence (1111). The address detector switches from listening to processing preamble, then to processing bit sequence, but no trigger is generated because the bit sequence is not matched.

The case of receiving a charging signal is shown in Fig. 17. When the WuTx is conducting a charging task, the address detector receives a continuous signal from the rectifier. The figure shows receiving a continuous charging signal for a period of 6 seconds. The charging signal is first treated by the address detector as a WuS, in the same way as the previous figures. When the voltage exceeds the threshold of the RX/harvesting switch, its output turns low and disconnects power from the auto-power off timer. The detector moves to the charging state and remains in that state as long as the R_2C_2 voltage remains above the threshold.

E. Combined address detector and harvester

In this section, the baseband receiver is configured to share the energy harvesting storage energy element with the IoT device. We demonstrate that powering OFF the address detector while charging allows the system to charge the energy storage element faster and from lower power levels at the rectifier's input. In the experimental setup, the address detector

Fig. 18. Charging times for different address detector configurations loading the storage capacitor. The detector powers the minimal components (data slicer and RX/harvesting switch) and achieves faster charging at lower levels.

is configured to draw current from an energy storage capacitor connected to the output of a passive harvesting system that we designed and tested in [9] and [41]. Additionally, the harvesting system receives a continuous signal with a frequency of 2.42 GHz from a dedicated transmitter.

Fig. 18 shows the duration required to charge a Chip Monolithic Ceramic Capacitor from Murata with a measured capacitance of 120 μF to a voltage level of 4.5 V at different input power levels (P_{in}). Each subfigure exhibits three attempts to charge the capacitor at different configurations of the address detector's circuit: 1) Default configuration with only the data slicer and RX/harvesting switch powered ON during charging. 2) PWD powered ON during charging. 3) Bit correlator powered ON during charging.

At the highest input power level ($P_{in} = 0$ dBm) the three configurations achieve similar charging times, with the default configuration narrowly leading the other two configurations. However, the difference in charging times increases for lower input power levels. For example, at $P_{in} = -4$ dBm, the capacitor can be charged in 55 seconds for the default configuration, but requires 62 seconds and 95 seconds to reach the same level for the other two configurations. When P_{in} is decreased to -6 dBm, the capacitor's voltage does not reach the maximum value if the bit correlator is powered ON. Furthermore, the capacitor charges to the highest voltage at $P_{in} = -8$ dBm in the default configuration. Its voltage reaches 2.7 V after 100 seconds of charging, when compared to 2.3 V and 1.5 V

Fig. 19. Average active current consumption of the proposed detector for different wake-up signal characteristics composed of a) 8-bits and b) 16-bits.

Fig. 20. Address detector's combined current consumption in operation scenarios involving wake-up and charging. Different plots are shown for a variety of WuS and charging signal characteristics. a) proposed architecture b) No RX/harvesting switching (PWD remains ON during charging).

for the second and third configurations, respectively.

The capacitor's measured load-free, self-discharge rate is 48 seconds for discharging from 4.5 V to 3.5 V after the input power is removed. The capacitor self-discharge can be minimized by eliminating fabrication imperfections. In addition, the capacitor discharges into the measurement equipment that is used to record the voltage.

V. ANALYSIS AND DISCUSSION

A. Average current consumption in a noise-free environment

In this section, we show that the introduction of multiple power states reduces the detector's current consumption when compared to conventional detectors. We consider the detector to operate in the active state during the period of processing a wake-up signal, i.e. when the detector is operating either in the processing preamble or processing bit sequence state. To highlight the power savings achieved by the proposed design, we consider operation in a wake-up scenario and a combined scenario composed of wake-up followed by charging and compare the active state current consumption with a conventional receiver.

1) *Current consumption in the wake-up scenario:* We define the active state current consumption as the current consumed during the processing of one WuS using Equation 1:

$$I_{\text{active}} = \frac{t_p}{t_{\text{WuS}}} \cdot I_p + \frac{t_s}{t_{\text{WuS}}} \cdot I_s \quad (1)$$

where t_p and t_s represent the time spent in the processing preamble and processing bit sequence states, respectively. In

addition, t_p is equal to the preamble width and t_{WuS} is the period of the WuS. t_{WuS} can be calculated as:

$$\begin{aligned} t_{\text{WuS}} &= t_p + t_s \\ &= t_p + g_1 + (n \cdot t_{\text{bit}}) + ((n-1) \cdot g_2) \end{aligned} \quad (2)$$

where g_1 and g_2 are the guard times, t_{bit} is the period of one PWM-modulated bit (assuming the case of an all-one address), and n is the number of bits in the bit sequence.

Introducing two operating states within the period of the WuS reduces the value of I_{active} when compared to a two-state detector with a constant active state current $I_{\text{active}} = I_s$, as shown in Fig. 19.a and Fig. 19.b. For a constant bit rate, the current is smaller for larger preamble sizes because the detector spends a larger fraction of t_{WuS} in the processing preamble state. On the other hand, the current increases with slower bit rates with a constant preamble width.

2) *Current consumption in the combined scenario:* We consider a scenario where the system receives one WuS followed by one charging signal. We define I_{combined} as the address detector's average current during a period of one WuS followed by one charging operation. The combined current consumption can be found by considering the fraction of time spent in the charging state (t_c) and the combined charging and wake-up wake-up signal period $t_{\text{active}} = t_{\text{WuS}} + t_c = t_p + t_s + t_c$ in Equation 1. We compare the system's combined current consumption with that of a circuit configuration where the PWD remains powered ON during charging operations. This scenario occurs if the RX/harvesting switch is removed from the proposed system (see Fig. 6).

The combined current decreases for longer charging periods because the detector spends most of the time in the charging state, as shown in Fig. 20.a. The proposed architecture significantly reduces the circuit's combined average consumption. For example, I_{combined} remains under 0.5 μA for a WuS preamble width of 200 ms followed by a charging signal that lasts for 30 seconds.

B. Average current consumption in a noisy environment

To highlight the enhanced noise immunity, we consider the average current consumption of the proposed architecture in a noisy environment and compare it to that of a two-state detector configuration operating under the same noise conditions. The average current consumption in a noisy environment can be found using Equation 3 and 4 for the two-state and multi-state configurations, respectively:

$$I_{\text{noise}} = D_l \cdot I_l \cdot (1 - PF_{\text{threshold}}) + D_s \cdot I_s + D_l \cdot I_s \cdot PF_{\text{threshold}} \quad (3)$$

$$\begin{aligned} I_{\text{noise}} &= D_l \cdot I_l \cdot (1 - PF_{\text{threshold}}) + \\ &D_l \cdot I_l \cdot (1 - PF_{\text{threshold}} \cdot PF_{\text{preamble}}) + \\ &D_p \cdot I_p \cdot (1 - PF_{\text{preamble}}) + D_s \cdot I_s + \\ &D_l \cdot I_p \cdot PF_{\text{threshold}} \cdot (1 - PF_{\text{preamble}}) + \\ &D_l \cdot I_s \cdot PF_{\text{threshold}} \cdot PF_{\text{preamble}} + D_p \cdot I_s \cdot PF_{\text{preamble}} \end{aligned} \quad (4)$$

where D_l , D_p , and D_s represent the fraction of time spent in the listening, processing preamble, and processing bit

Fig. 21. Current consumption of the proposed architecture versus a two-state configuration in a noisy environment.

sequence states, respectively. I_l , I_p , and I_s are the current consumption in each state. $PF_{\text{threshold}}$ is the probability of noise level exceeding the system's threshold and PF_{preamble} is the probability of false detection of noise as a preamble.

Figure 21 shows a comparison between the consumption of the two configurations when operating under noisy conditions. The time separating two wake-ups is set to 24 hours, and the wake-up signal is received at 500 bps with a preamble of 200 ms. At the maximum noise level ($PF_{\text{threshold}} = 1$), the two-state address detector operates at the maximum current of I_s , while the multi-power address detector remains in the processing preamble state. Its current reaches I_s only if the preamble is falsely detected. Based on the experimental results and analytical discussion, we conclude that the coded preamble scheme leads to three benefits: 1) Preamble can be used for addressing. 2) Reduced active state current consumption per WuS. 3) Enhanced noise immunity.

VI. COMPARISON WITH EXISTING WORKS

In this section, we provide a comparison between this work and similar efforts reported in the literature as shown in Table IV. Examples of hardware realized through discrete components are found in [22]–[24]. A microcontroller is used as a bit correlator in [22] and [23]. The design in [22] implements a passive noise rejection preamble, and a preamble composed of one Return-to-Zero (RZ) encoded 1-bit is used in [23]. On the other hand, the AS3933 [43] correlator used in [24] offers a low active current consumption of 8 μA , a sensitivity of -52 dBm, and a bit rate of 1 kbps.

Several reported designs combine a wake-up receiver with energy harvesting. For example, the authors in [48] integrate an RFID module with an RF energy harvester operating at the 900 MHz ISM band. The RFID chip is powered through the harvested energy, and it wakes up from the listening state when the accumulated voltage exceeds a minimum threshold. An external battery can be used to extend the system's sensitivity from -17 dBm to -24 dBm. Alternatively, an energy harvester is used in [49] to power an OOK wake-up receiver operating at the 900 MHz and 2.4 GHz ISM bands. OOK signal demodulation can occur when the harvester's output exceeds 1.8 V. Therefore, the system has a sensitivity of 500 mV and can be powered at a maximum distance of 1.5 m. In [50],

TABLE IV
STATE-OF-THE-ART COMPARISON

Design	Tech.	Combined Harvest /Wake-up	Freq.	Modulation Scheme	Sensitivity [dBm]	Clocking Source	Bias [V]	Bit Rate [kbps]	Preamble Function	Current Con-sump. (listen-ing) [μ A]	Current Con-sump. (active) [μ A]	Current Con-sump. (Charg-ing) [μ A]
This Work	Discrete-Component	Yes	2.42 GHz	PWM	-40	Extracted From Input	2.6	0.5	Addressing	0.225	3.225; 13.725¹	0.15
[22]	Discrete-Component	No	868 MHz	OOK	-32	μ C	1.8	10	Noise Filtering	0.106	35	NA
[23]	Discrete-Component	Yes	915 MHz	OOK	SEE NOTE ²	μ C	2.2	33.3	Noise Filtering	0.13	270 @ 1 MHz	0.13
[24]	Discrete-Component	No	2.4 GHz	OOK ³	-52	AS3933 [43]	3	1	Sync.	3.6	8	NA
[11]	CMOS	No	902-928 MHz	OOK	-78.5; -75 ⁴	Local Osc.	Variable	10; 200 ⁵	Sync.	16.4 ⁶	22.9 ⁶	NA
[25]	CMOS	No	433.9 MHz	PWM	-30 ⁷	Extracted From Input	1.5	80	Noise Filtering	0.28 ⁸	1.8	NA
[13]	CMOS	No	45 MHz	FSK	-62.7	Local Osc.	0.7	200	NA	53.5	53.5	NA
[44]	CMOS	No	780-950 MHz	OOK	-86	Extracted From Input	1	10	NA	123	123	NA
[45]	CMOS	No	80 MHz	FSK	-62	Local Osc.	0.7	312	NA	64.2	64.2	NA
[31]	CMOS	No	2.45 GHz	OOK	-47	Extracted From Input	1	200	Sync.	2.3	2.3	NA
[21]	CMOS	No	2.4 GHz	OFDM ⁹	-72	Local Osc.	0.95	62.5	Sync.	121	182	NA
[12]	CMOS	No	113.5 MHz	OOK	-69	Local Osc.	0.4	0.3	NA	0.01125	0.01125	NA
[46]	Discrete-Component	No	28 MHz	PWM	-97	Local Osc.	1.5	1.25	NA	26.66	26.66	NA
[47]	CMOS	No	2.4 GHz	OOK	-51.5	Injection-lock	1	200	NA	50	50	NA
[48]	Discrete-Component	Yes	900 MHz	NA	-17; -24 ¹⁰	NA	1.8	NA	NA	15	100	Passive
[49]	CMOS	Yes	0.9/2.4 GHz	OOK	500 mV ¹¹	Local Osc.	1.8	40/80/160 kbps	NA	Passive	20	Passive
[50]	CMOS	Yes	902-928 MHz	FSK; OOK ¹²	-78; -53 ¹²	Injection-lock	1.2	8000; 100 ¹²	NA	532.5	532.5	Passive

¹ Processing preamble state; processing bit sequence. ² Sensitivity is not reported in dBm. The wake-up range is 1.16 m with 13 dBm transmit power. ³ Subcarrier modulation of 2.4 GHz signal emulating an OOK signal. ⁴ Listening mode; detection mode. ⁵ Listening mode; active mode. ⁶ Value in μ W. ⁷ At a bit rate of 80 kbps. ⁸ 180 nA for the address detector + 100 nA for the microcontroller. ⁹ OOK emulating OFDM. ¹⁰ Fully-passive mode; battery-assisted mode. ¹¹ Sensitivity is not reported in dBm. The maximum wake-up distance = 1.5 m. ¹² Main receiver; wake-up receiver.

a rectifier is integrated with an FSK receiver and used as a passive OOK demodulator, generating a wake-up message to activate baseband signal processing. The FSK receiver remains permanently powered ON and has a current consumption of 532.5 μ A.

Various designs are realized using CMOS technology to achieve a compact size and enhanced performance. Higher sensitivity is achieved by implementing an RF amplification stage at the expense of higher current consumption [13] [21] [11] [44] [45]. The method in [44] achieves the highest sensitivity in this comparison. It is obtained at a constant

current consumption of 123 μ A and a data rate of 10 kbps. While some CMOS designs achieve a higher sensitivity, it is important to note that our approach does not include an active RF amplification stage [13] [21] [11] [44] [45].

A current consumption in the few- or sub-microamp range is reported in [12] [31] [25]. The design in [25] features PWM modulation and clock extraction. The design in [31] offers clock extraction using Manchester Coding. The authors in [12] achieve a current consumption of 11.25 nA and a bit rate of 0.3 kbps. The design includes a passive RF amplification stage and has a sensitivity of -69 dBm.

To conclude, the current consumption is proportional to sensitivity and bit rate. The CMOS fabrication process offers the advantages of high sensitivity and low current consumption, while the discrete component approach is inexpensive and less complex to implement. When compared to alternative designs that combine wake-up and harvesting, the method proposed herein is unique because it incorporates addressing into the preamble. Furthermore, it avoids activating the receiver during or after charging, and reduces current consumption by shutting down the unnecessary components during the listening and processing preamble states.

VII. CONCLUSION

In this paper, we introduced an address detector for systems employing combined RF wake-up and charging. To minimize our architecture's current consumption, we offer multi-power operation where the circuit continuously spins between different states, consuming a varying current. The circuit senses the input received from the rectifier and determines the next action to take (switch ON a complex bit correlator, return to listening, or turn off the main circuitry while the device is charging). We suggest extending the preamble's role beyond simple noise filtering by encoding a message in its varying width. The hardware shows flexibility in detecting the coded preamble and the following PWM-modulated bit pattern. It can be tuned to identify pulses with a width ranging from a few hundred microseconds to a few milliseconds by adjusting a variable resistor and delivers a maximum data rate of 500 bps. The proposed detector offers a minimal current consumption of 0.225 nA by shutting down its main components. In addition, the multi-power approach leads to reduced current consumption, ability to charge at lower input power levels, faster charging times, and enhanced noise immunity. These improvements make our approach suitable for applications that rely on harvesting and wake-up to minimize power consumption and extend battery life.

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