Ultralow contact resistance between semimetal and monolayer semiconductors

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Advanced beyond-silicon electronic technology requires discoveries of both new channel materials and ultralow-resistance contacts^{1,2}. Atomically thin two-dimensional (2D) semiconductors have great potential for realizing high-performance electronic devices^{1,3}. However, because of metal-induced gap states (MIGS)⁴⁻⁷, energy barriers at the metal-semiconductor interface, which fundamentally lead to high contact resistances and poor current-delivery capabilities, have restrained the advancement of 2D semiconductor transistors to date^{2,8,9}. Here, we report a novel ohmic contact technology between semimetallic bismuth and semiconducting monolayer transition metal dichalcogenides (TMDs) where MIGS is sufficiently suppressed and degenerate states in the TMD are spontaneously formed in contact with bismuth. Through this approach, we achieve zero Schottky barrier height, a record-low contact resistance (R_C) of $123 \, \Omega \, \mu\text{m}$, and a record-high on-state current density (I_{ON}) of $1135 \, \mu\text{A} \, \mu\text{m}^{-1}$ on monolayer MoS_2 . We also demonstrate that excellent ohmic contacts can be formed on various monolayer semiconductors, including MoS_2 , WS_2 , and WSe_2 . Our reported R_C values are a significant improvement for 2D semiconductors, and approaching the quantum limit. This technology unveils the full potential of high-performance monolayer transistors that are on par with the state-of-the-art 3D semiconductors, enabling further device down-scaling and extending Moore's Law.

The electrical contact resistance at a metal-semiconductor (M-S) interface has been an increasingly critical, yet unsolved issue for the semiconductor industry, hindering the ultimate

scaling and the performance of electronic devices⁹. The main cause of this resistance is the energy barrier, called Schottky barrier (SB), formed between the metal electrode and semiconductor⁸, due to (I) the energy difference between the metal work function and the semiconductor electron affinity, and (II) metal-induced gap states (MIGS) resulting in Fermi level pinning⁴⁻⁷. When a semiconductor is in close proximity to a metal surface, the extended wavefunction from the metal perturbs the environment of the semiconductor, leading to rehybridizations of semiconductor's original wavefunctions. MIGS is a result of such perturbation, where new states in resonance with the metal states emerge in the band gap (Fig. 1a), as compared to the original density of states (DOS) of MoS₂ before contact (Fig. 1c). Resembling the contours of metal DOS after the band alignment, the density of MIGS is contributed by the valence band (VB) (i.e., donor-like, positively-charged states) and the conduction band (CB) (i.e., acceptor-like, negatively-charged states)¹⁰. It has been theoretically and experimentally demonstrated that the Fermi level of the M-S system is pinned at around the branching point of these two components [referred to as gap-states pinning (GSP) (Fig. 1a)], an energetically favorable state when free of residue charges¹⁰. If Fermi level of the system lies inside the semiconductor bandgap, a SB is unavoidable (Fig. 1d).

Two strategies have been developed to solve this issue: (I) reducing the SB width by heavily doping the semiconductor so that the tunneling current outweighs thermionic emission current at the SB¹¹; (II) decoupling the M-S interaction by introducing a thin dielectric, molecular layer, or van der Waals (vdW) gap at the interface^{6,12-14}. While the first strategy is technologically challenging for 2D materials, the second architecture is dominated by a non-negligible tunneling barrier due to the increased M-S distance^{15,16}. Since these two strategies typically end up with either high SBs in the range of 100 – 400 meV or interface tunneling

barriers with above-1-nm thick in monolayer TMD transistors^{6,13,14,17}, the state-of-the-art contact resistance is around 1 k Ω μ m, at least one order of magnitude larger than metal-Si contact¹.

Here, we propose a new strategy to reduce contact resistance by suppressing MIGS using semimetal-semiconductor contacts to avoid GSP (Fig. 1b). A semimetal has near-zero DOS at the Fermi level where few MIGS can be induced; therefore, if the Fermi level of a semimetal is close to the CB minimum (CBM) of the semiconductor, the CB-contributed MIGS is greatly reduced. As a result, the MIGS are greatly suppressed and are purely contributed by the VB, thus can be filled up and saturated [this is referred to as gap-state saturation (GSS)]. In this way, the semiconductor in contact with semimetal will be in a degenerate state and free of SB at the interface (Fig. 1e).

To prove this hypothesis, we fabricate back-gated field-effect transistors (FETs) with a variety of monolayer TMDs and form low-resistance contacts (“ohmic” contacts) by depositing semimetal bismuth (Bi) onto the contact windows of the 2D channel (Fig. 1f). Figure 2a compares typical transfer curves (I_{DS} - V_{GS}) of Bi-, Ni-, and Ti-contacted transistors made of monolayer MoS₂ synthesized by metal-organic chemical vapor deposition (MOCVD). Among them, the Bi-MoS₂ FET clearly exhibits enhanced n-channel conduction with a high on/off current ratio of $>10^7$. Moreover, the Bi-MoS₂ interface shows linear output characteristics (I_{DS} - V_{DS}) both at room temperature (Fig. 2b) and at low temperatures (Fig. 2g and Extended Data Fig. 1a–c), indicating a good ohmic contact with a negligible SB height. In contrast, the nonlinear output characteristics in both Ni- and Ti-contacted MoS₂ (Extended Data Fig. 1d, e, h) suggest the presence of barriers, which are similar to previous reports using either Schottky or interfacial layer contacts^{13,14,17-21}. The R_C for the Bi contact to monolayer MoS₂ is as low as 123 Ω μ m at a

carrier density (n_{2D}) of $1.5 \times 10^{13} \text{ cm}^{-2}$, as shown in Fig. 2c (more data points shown in Fig. 4h and Extended Data Fig. 2d).

It is observed that the electrical characteristics of Bi-MoS₂ FETs are dominated by the MoS₂ channel. The contact resistance ($2R_C$) in the Bi-MoS₂ FETs contributes to less than 5% of the total resistance (R_{TOT}) in a wide range of n_{2D} (Extended Data Fig. 2d). By lowering down temperature from room temperature to 77 K, the drain current density (I_{DS}) in 2-terminal Bi-MoS₂ FETs increases due to the enhanced electron mobility of MoS₂, while the I_{DS} in both Ni-MoS₂ and Ti-MoS₂ FETs are dramatically suppressed (Fig. 2d and Extended Data Fig. 1g), owing to the reduction of thermionic emission current at contact. The field-effect mobilities from 2-terminal and 4-terminal devices as a function of temperature (Fig. 2e) shows identical characteristics, which suggests that the ultralow R_C makes 2-terminal devices a simple yet powerful platform for characterizing intrinsic temperature-dependent transport properties of 2D semiconductors, whereas 4-terminal devices were always required previously^{14,20}. As a side note, the 2-terminal field-effect electron mobility of the MOCVD-grown monolayer MoS₂ channel reaches $120 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 77 K and $55 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature, outperforming ultrathin silicon ($< 2 \text{ nm}$) and germanium ($< 4 \text{ nm}$) on insulator devices³.

We present three evidences of the absence of SB in Bi-MoS₂ FETs. First, the R_C in the Bi-MoS₂ FETs is nearly independent of n_{2D} (determined by the overdrive voltage, $V_{GS}-V_T$, where V_T is the threshold voltage), suggesting a negligible, if not zero, energy barrier at the Bi-MoS₂ (Fig. 4h^{14,18-20,22}). Second, our temperature-dependent I_{DS} shows that the Bi-MoS₂ FETs operate in the barrier-free transport limit (see Methods). For Schottky contacts, the Arrhenius plots [$\ln(I_{DS}/T^{1.5})$ versus $1000/T$] are linear with negative slopes (Fig. 2f and Extended Data Fig. 2a,b), from which the SB heights (Φ_{SB}) at flatband are extracted to be 100 meV for Ni-MoS₂

and 150 meV for Ti-MoS₂ (Extended Data Fig. 1f, i). However, this analysis becomes invalid for Bi-MoS₂ FETs. Instead, the saturation-like regime at lower temperatures (< 200 K) suggests a zero contact barrier height for electron transport, while the positive slope in the range of 200 – 300 K can be attributed to the negative correlation between mobility and temperature. Finally, the $I_{\text{DS}}-V_{\text{DS}}$ curves of Bi-MoS₂ FETs remain linear at low temperatures (Fig. 2g and Extended Data Fig. 1a–c). We define nonlinearity, N , of the $I_{\text{DS}}-V_{\text{DS}}$ relation as $N = [d^2I_{\text{DS}}/dV_{\text{DS}}^2]/2[dI_{\text{DS}}/dV_{\text{DS}}]$. $N = 0$ corresponds to linear relation, where no barrier exists; larger N means increased nonlinearity, which is associated with a higher SB. As shown in Fig. 2h, although the nonlinearities are close to zero for the Ni and Ti contacts at room temperature, they increase quickly as temperature decreases; in contrast, the nonlinearity for the Bi contact maintains zero throughout different temperatures.

To confirm the GSS of Bi-MoS₂, we carry out first-principles calculation based on the crystal structure identified from TEM, and the theoretical result is further substantiated by the evidence from XPS and Raman. The selected-area electron diffraction (SAED) measured on a freestanding MoS₂/Bi/Au stack (Fig. 3a) shows three sets of hexagonal patterns corresponding to the Bi, MoS₂, and Au crystals, respectively, indicating that Bi (0001) plane is parallel to the plane of MoS₂ (Fig. 3b and Extended Data Fig. 3b–d). The diffraction pattern of MoS₂ proves its 2H semiconducting phase with no metallic-phase transition²³. Among the pseudocubic (metallic) and rhombohedral (semimetal) phases of Bi²⁴, the hexagonal SAED pattern has ruled out the possibility of the former. As a comparison, when Bi is directly deposited onto amorphous carbon, it becomes polycrystalline and partially oxidized into Bi₂O₃ evidenced by the powder-like diffraction rings with an extra set of Bi₂O₃ patterns located at 3.0 nm⁻¹ as shown in Extended Data Fig. 3f. From this, we conclude that no oxidation takes place at the Bi-MoS₂ interface.

We build a supercell (Fig. 3c) based on the above information and perform first-principles calculations using density functional theory (DFT). First, the resistance of the tunneling barrier between Bi and MoS₂ is calculated to be low. The barrier has a width (w_t) of 1.66 Å and a height (Φ_t) of 3.6 eV marked in the electrostatic potential profile. This induces a tunneling resistivity (ρ_t) of $1.81 \times 10^{-9} \Omega \text{ cm}^2$, as shown in the equivalent circuit in Fig. 3d, which is very small compared with those made with thin dielectric gaps^{6,14}. Second, the Fermi level of MoS₂ is shifted into the conduction band (Fig. 3e), yielding a degenerate MoS₂ in contact with Bi with $n_{2D} \sim 2 \times 10^{13} \text{ cm}^{-2}$ and a small sheet resistance $R_{\text{SH,C}} \sim 15.6 \text{ k}\Omega$. The degenerate MoS₂ (I) reduces the overall resistance of the ρ_t - $R_{\text{SH,C}}$ network in Fig. 3d, and (II) more importantly, eliminates the SB between Bi and MoS₂, resulting in a negligible SB resistance. The overall contact resistance is calculated to be $130 \Omega \mu\text{m}$, in very good agreement with our measured values (see Methods for details).

In contrast to other metals (like Ni, Pt, Au, Ag, In)^{25,26}, the MIGS is greatly reduced in the case of Bi (Fig. 3e). The wavefunction of the p_z orbital of Bi is in resonance with the p_z and d_{z^2} orbitals of MoS₂ where the MIGS clearly follows the projected local density of states (PLDOS) of Bi (inset of Fig. 3e). However, unlike the others, the MIGS has been completely saturated with electrons, which leads to GSS. Several other observations include: (I) The charge transfer from Bi to MoS₂ is minimal based on the undistorted potential profile, and the induced electric dipole almost completely falls within the vdW gap (seen from the differential charge distribution of Fig. 3c). (II) The decrease of the VB states has outpaced the increase of MIGS (Fig. 3f), pushing the Fermi level up into the CB. (III) Two factors are strongly correlated to the final contact type: (a) the nature of zero DOS at the Fermi level and saturated bonds on the surface of the semimetal, and (b) the work function of the semimetal compared with the electron

affinity of MoS₂. The DFT results of the contact between V-group semimetals (Bi, Sb, and As) and MoS₂ support this hypothesis: since Fermi levels of Bi and Sb are equal or above the CBM of MoS₂ (Fig. 3g), they are predicted to have negligible SB contacts (Fig. 3e and Extended Data Fig. 4a); whereas the Fermi level of As-MoS₂ is still inside the band gap.

Both Raman and XPS characterization results confirm that the monolayer MoS₂ under the Bi contacts turns to degenerate. First, the A_{1g} Raman vibration mode of Bi-contacted monolayer MoS₂ shows a $\sim 10 \text{ cm}^{-1}$ redshift, corresponding to an electron density of $(2-5) \times 10^{13} \text{ cm}^{-2}$ and a Fermi level position at 40 – 100 meV above CBM (Fig. 3h)^{27,28}. In comparison, neither the A_{1g} peaks for Ni-MoS₂ or Au-MoS₂ samples exhibit such shifts (Extended Data Fig. 5b). We note that all the three metal contacts result in similar shifts of the E_{2g} phonon mode, which is likely due to the strain induced at the MoS₂-metal interface²⁹. Second, the blue shifts of both Mo3d and S2p peaks in XPS spectra shown in Fig. 3i and Extended Data Fig. 5c reveals a 400-meV lifting of the Fermi level³⁰ when MoS₂ is in contact with Bi.

The proposed GSS mechanism at the Bi-MoS₂ interface applies to a variety of 2D semiconductors and enables reliable and significantly improved transistor performance. We benchmark our transistor performance with the on-state current density (I_{ON}), a figure-of-merit in transistor scaling, and R_{C} , a key parameter limiting the scaling of I_{ON} and power supply voltage (V_{DD})⁹. Figures 4a–c show typical output characteristics of monolayer MoS₂, WS₂, and WSe₂ transistors (channel length $L_{\text{CH}} = 120 \text{ nm}$) on 100-nm-thick SiN_x gate dielectrics. The linear relationships of $I_{\text{DS}}-V_{\text{DS}}$ at low-field regime indicate their ohmic contacts, and this leads to high on/off current ratios ($> 10^7$, Extended Data Figs. 6 and 7e) and new records of current-delivery capability (Fig. 4e) among monolayer TMDs at a drain voltage of 1.5 V^{22,31-33}. The highest I_{ON} achieved in our study are $560 \mu\text{A } \mu\text{m}^{-1}$ and $1135 \mu\text{A } \mu\text{m}^{-1}$ for a 120-nm L_{CH} and a 35-nm L_{CH}

monolayer MoS₂ FETs, respectively (Extended Data Fig. 7d and Fig. 4d). Given that W-based TMDs have lower electron affinity than MoS₂, making it more difficult to make good n-type ohmic contacts to these materials¹⁵, we perform first-principles calculation to confirm the formation of the degenerate state of WS₂ when contacted with Bi as shown in Extended Data Fig. 4c. In addition, it is observed that such barrier-free contacts can be formed on TMD crystals prepared by different methods including CVD, MOCVD, and mechanical exfoliation (Fig. 4a-c, Extended Data Figs. 7d-f, 8b-d), while a high-quality crystal is essential to avoid the undesired GSP (see DFT results in Extended Data Fig. 4b, experimental results in Extended Data Fig. 8 and additional discussion in Methods). Last but not least, the Bi contact is formed through a standard CMOS-compatible evaporation process, which promises good reliability and scalability. Figure 4e presents statistics of I_{ON} measured on more than 20 Bi-TMD transistors. Average I_{ON} of 367, 331, and 300 $\mu\text{A } \mu\text{m}^{-1}$ at a V_{DS} of 1.5 V with narrow distributions are achieved for monolayer MoS₂, WS₂, and WSe₂ FETs.

Figures 4g and 4h summarize the state-of-the-art contact methods for both monolayer and thicker MoS₂. The Bi contact to monolayer MoS₂ yields the lowest R_{C} . We expect an even lower R_{C} for Bi contacts with thicker MoS₂ than monolayer^{2,33-36}, and the I_{ON} of our monolayer transistor has already exceeded the previous record for multilayer transistors (Fig. 4e). Furthermore, our measured R_{C} values are comparable to those reported in mainstream 3D semiconductors, approaching the quantum limit^{1,2}.

Finally, we propose that the Bi-TMD FET technology could be readily scaled down to sub-10 nm technology nodes and potentially meet the requirement of the *International Roadmap for Devices and Systems* (IRDS) 2024 targets of logic transistors (pentagons in Fig. 4f)³⁷. Our Bi-TMD transistors establish a new benchmark for monolayer TMD FETs (Fig. 4e), and deliver

comparable performance to modern silicon transistors with similar dimensions (diamonds in Fig. 4f)^{38,39}. With the consideration of critical scaling rules such as the contact length (L_C) scaling and supply voltage (V_{DD}) scaling, we conclude that our low- R_C contact is essential for maximized I_{ON} in aggressively down-scaled transistors. First, as the current transfer length of the contact (L_T) for Bi contact is as small as ~ 7 nm (Extended Data Fig. 9b), the L_C -scaling-associated R_C increase and I_{ON} suppression are mitigated (Fig. 4f). Second, the much lower R_C ensures that the drain voltage is dropped mostly across the channel, which significantly reduces the required minimum V_{DD} , at each technology node for driving the MoS₂ channel to the velocity saturation regime, in order to reach its maximum current (Extended Data Fig. 9c, d). The current saturation for the I_{DS} - V_{DS} characteristics, as well as the constant spacing between the saturated I_{DS} for the same overdrive voltage interval (Fig. 4a-c, Extended Data Fig. 7f) suggest that the Bi-TMD FETs can already work in velocity saturation when $L_{CH} = 120$ -150 nm and $V_{DD} = 1.5$ V. This promises a maximized I_{ON} for FETs with even shorter channels and lower V_{DD} (blue dashed lines and open circles in Fig. 4f). The saturation velocity v_{sat} , which determines the maximum I_{ON} , is extracted to be $\sim 2.5 \times 10^6$ cm/s (see Methods). As I_{ON} of $1135 \mu A \mu m^{-1}$ is achieved experimentally for a 35-nm-channel device, we envision that I_{ON} exceeding $1800 \mu A \mu m^{-1}$ in a 10-nm-channel monolayer TMD FET at a n_{2D} of $4.5 \times 10^{13} \text{ cm}^{-2}$ (Fig. 4f) could be realized in the foreseeable future, reaching the industrial goal of next-generation transistor technologies.

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Competing interests P.-C.S. and J.K. are co-inventors on a patent application (provisional filling number 63/024,141) related to the research presented in this paper.

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Additional information Correspondence and requests for materials should be addressed to J.K., L.-J.L. and P.-C. S.. Reprints and permissions information is available at www.nature.com/reprints.

Fig. 1 | The concept of gap-state saturation (GSS) at semimetal-semiconductor contact. **a**, The density of states (DOS) of normal metal (M) and semiconductor (SC) contact. The conduction band (CB) and valence band (VB) contributed metal-induced gap states (MIGS) are shaded as orange and blue areas. Fermi level is pinned at around the branching point of MIGS, leading to gap-state pinning (GSP). **b**, The DOS of semimetal (SM) and SC contact. Because the Fermi level of SM aligns with the CB of the SC and DOS at Fermi level of SM is near-zero for the SM, CB-contributed MIGS is suppressed and the branching point is elevated into CB. The MIGS, now mostly contributed by VB, is saturated, leading to gap-state saturation (GSS). **c**, The reference DOS of SC before contact. **d**, **e**, The band structure of **(d)** M and SC contact, where Schottky barrier (SB) is formed as a result of GSP, and **(e)** SM and SC contact where ohmic contact is formed as a result of GSS. TB: tunneling barrier. **f**, Schematic of a 2D FET with a monolayer (1L) SC (MoS₂) channel and SM (Bi) contacts. The degenerate part of Bi-contacted MoS₂ due to GSS is marked in orange color.

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Fig. 2 | Comparison of ohmic and Schottky contacts in monolayer MoS₂ FETs. **a**, Comparison of room-temperature transfer characteristics (I_{DS} – V_{GS}) of typical monolayer MoS₂ FETs with Bi, Ni, and Ti contacts on 300-nm-thick SiO₂ dielectrics. The Bi-MoS₂ FET presents an on/off current ratio (I_{ON}/I_{OFF}) of $>10^7$. **b**, Typical output characteristics (I_{DS} – V_{DS}) of Bi-MoS₂ FETs at room temperature. **c**, Contact resistance (R_C) extraction using TLM for Bi-MoS₂ FETs on 100-nm-thick SiN_x dielectrics. Blue squares and black circles are total resistance versus channel length at carrier densities of 5.6×10^{12} and 1.5×10^{13} cm⁻², respectively. Inset: False color SEM image of the TLM structure. Scale bar: 1 μ m. **d**, Typical I_{DS} – V_{GS} of ohmic Bi-MoS₂ (blue) and Schottky Ni-MoS₂ (red) FETs on 300-nm-thick SiO₂ dielectrics at various temperatures. **e**, Two-terminal and four-terminal electron mobilities of the Bi-MoS₂ FET as a function of temperature. The consistency between these two methods suggests negligible R_C . The temperature dependence of the mobility $\mu \sim T^{-1.69}$ indicates the dominant optical phonon scattering⁴⁰. **f**, Arrhenius plots of the ohmic Bi-MoS₂ (blue) and Schottky Ni-MoS₂ (red) FETs at a carrier density (n_{2D}) of 1.5×10^{12} cm⁻² and V_{DS} of 1 V. A 30-meV and negligible barrier for Ni-MoS₂ and Bi-MoS₂ FETs, respectively, are extracted. **g**, Typical I_{DS} – V_{DS} of Bi-MoS₂ and Ni-MoS₂ FETs with $V_{GS} = 60$ V and $n_{2D} \sim 4.3 \times 10^{12}$ cm⁻² at 77 K. The full I_{DS} – V_{DS} characteristics can be found in Extended Data Fig. 1b, e. **h**, Nonlinearity ($\mathcal{N}$) of the I_{DS} – V_{DS} for MoS₂ FETs with Bi, Ni, and Ti contacts at various temperatures. Data are extracted at $V_{DS} = 0.1$ V at $n_{2D} \sim 4.3 \times 10^{12}$ cm⁻². $\mathcal{N} = 0$ of the Bi-MoS₂ FET indicates its linear I_{DS} – V_{DS} characteristics, revealing ohmic contact at the Bi-MoS₂ junction.

Fig. 3 | Crystal structure and mechanism of ohmic contact. **a**, Schematic of freestanding Au/Bi/MoS₂ on a meshed amorphous carbon (a-carbon) TEM grid for SAED. **b**, SAED patterns of MoS₂ (3.6 cm⁻¹), Bi (4.3 cm⁻¹), and Au (6.8 cm⁻¹) circled in yellow, purple, and orange respectively. **c**, The side view of Bi-MoS₂ (upper right panel, with the area marked in the inset 3D render), and the corresponding electrostatic potential profile along the vertical direction (left panel). The electron tunneling barrier is shaded in purple (width $w_t = 1.66$ Å, height $\Phi_t = 3.6$ eV). The distance between Bi and S atomic layers is $d = 3.4$ Å. The differential charge density (CD) inside the region of dashed line calculated by subtracting the pre-contact CD from the post-contact CD is superposed in the atomic structure (red: positive, blue: negative). The bottom right panel shows the band profile of MoS₂. **d**, The equivalent circuit of the Bi-MoS₂ contact area with the space partitioned with respect to their atomic colors. ρ_t : tunneling resistivity; $R_{SH,C}$: sheet resistances of MoS₂ in contact with Bi. **e**, Projected local density of states (PLDOS) of MoS₂ before (upper panel) and after (middle panel) in contact with Bi (lower panel). The valence band (VB) is shaded in light blue and conduction band (CB) in light red. Fermi level (E_F) is shifted from inside the gap (before Bi contact) to above the CB minimum (after Bi contact). Inset of middle panel: the magnified PLDOS in the band gap showing MIGS. **f**, The change of PLDOS of different orbitals in VB and MIGS areas marked in (e). **g**, The band alignment of monolayer MoS₂ with examples of semimetals (Bi, Sb and As). **h**, **i**, The shift of Raman (**h**) and XPS (**i**) spectra comparing standalone MoS₂ and Bi-contact MoS₂.

Fig. 4 | Benchmark of Bi-contacted 2D semiconductor technology. **a-c**, $I_{DS}-V_{DS}$ curves of Bi-monolayer MoS₂ (MOCVD) **(a)**, Bi-monolayer WS₂ (exfoliated) **(b)**, and Bi-monolayer WSe₂ (exfoliated) **(c)** FETs with L_{CH} of 120 nm. **d**, $I_{DS}-V_{DS}$ curves of a 35-nm- L_{CH} Bi-MoS₂ FET, showing a record-high I_{ON} of 1135 $\mu\text{A}/\mu\text{m}$. V_{GS} changes from -10 V to 50 V for (a) and (b), from -10 V to 60 V for (c), and from -10 V to 30 V for (d), all in steps of 10 V. Inset of (d): SEM image of the 35-nm- L_{CH} device. **e**, Statistics of I_{ON} for Bi-contacted monolayer TMD transistors, showing a reliable and improved performance with respect to previously reported monolayer,

thicker, and short-channel ($L_{\text{CH}} < 10\text{nm}$) TMD devices^{18,22,30-33,41-44}. Data are extracted and compared at the same V_{DS} of 1.5 V. Typical device performance metrics can be found in Extended Data Table 1. **f**, I_{ON} projection of monolayer TMD transistors with different contact technologies. The blue stars are the experimental data in this work. The solid lines show the projected I_{ON} as a function of L_{CH} for different metal contacts, including Bi (blue, $\rho_{\text{C}} \sim 8 \times 10^{-9} \Omega \text{cm}^2$), Ag (plum, $\rho_{\text{C}} \sim 3 \times 10^{-7} \Omega \text{cm}^2$), and In, hBN/Co, Ni, or Au (purple, $\rho_{\text{C}} \sim 3 \times 10^{-6} \Omega \text{cm}^2$) at a fixed electron mobility μ of $20 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and $n_{2\text{D}}$ of $1.5 \times 10^{13} \text{ cm}^{-2}$. The projections at $L_{\text{CH}} < 26 \text{ nm}$ (14-nm technology nodes) takes into considerations of both the L_{C} and the V_{DD} scalings. The relation between L_{C} and L_{CH} in this region are defined by the contacted gate pitch (CGP)³⁷. The light and dark blue dashed lines are projections for short-channel Bi-monolayer MoS_2 transistors operating at velocity saturation, with $n_{2\text{D}}$ of $4.5 \times 10^{13} \text{ cm}^{-2}$ and $1.5 \times 10^{13} \text{ cm}^{-2}$, respectively. The orange and green pentagons represent the lower bounds of IRDS 2024 target for low-power (LP, $I_{\text{ON}}/I_{\text{OFF}} > 10^6$) and high performance (HP, $I_{\text{ON}}/I_{\text{OFF}} > 10^4$) logic transistors³⁷, respectively. The turquoise diamonds are I_{ON} for 90-nm technology node strained silicon^{38,39}. The yellow triangle shows a representative I_{ON} for 100-nm AlGaAs/InGaAs transistors⁴⁵. **g**, Scaling of R_{C} with the thickness of MoS_2 and ultra-thin Si fins or films. The ranges of R_{C} for monolayer WS_2 (shaded green) and WSe_2 (shaded orange) are also shown^{2,13,14,18,22,30,32,33,41,44,46,47}. The black solid line indicates the quantum limit at $n_{2\text{D}} = 10^{13} \text{ cm}^{-2}$. **h**, State-of-the-art contact technology for MoS_2 transistors plotted as a function of the 2D sheet carrier density ($n_{2\text{D}}$), showing the respective R_{C} of various semiconductor technologies (Si, III-Vs, and MoS_2)^{1,13,14,17-22,33,46,48-50}. The black line represents the quantum limit of R_{C} , $\pi h/(4q^2 k_{\text{F}}) \sim 0.036(n_{2\text{D}})^{-0.5} \text{ k}\Omega \mu\text{m}$, which is determined by the quantum resistance ($h/2q^2 \approx 12.9 \text{ k}\Omega$) and the number of conducting modes per channel width (k_{F}/π) related to the 2D sheet carrier density ($n_{2\text{D}}$, in units of 10^{13} cm^{-2})².

Methods

Metal organic chemical vapor deposition (MOCVD) of monolayer MoS₂. Monolayer MoS₂ films are grown using low-pressure metal-organic chemical vapor deposition (MOCVD). Molybdenum hexacarbonyl [Mo(CO)₆, 98%, Sigma Aldrich] and diethyl sulfide (C₄H₁₀S, 98%, Sigma Aldrich) are selected as the precursors of molybdenum (Mo) and sulfur (S), respectively. With argon (Ar) as the carrier gas, the precursors are supplied in the vapor form into the chamber using a homemade bubbler system. The monolayer MoS₂ films are deposited on 300 nm-thick SiO₂/Si wafers at 320 °C for 15 hours with the flow rates of 100 sccm for Ar, 0.6 sccm for Mo(CO)₆, and 2.0 sccm for C₄H₁₀S. The typical Raman spectrum for the as-grown MOCVD monolayer MoS₂ is shown in Extended Data Fig. 5a.

Chemical vapor deposition (CVD) of monolayer MoS₂. Perylene-3,4,9,10-tetracarboxylic potassium salt (PTAS) molecules are used as the seeding promoter and are coated onto two clean SiO₂/Si pieces, serving as the seed reservoirs to provide the seeding molecules during the MoS₂ growth. The target substrate of a 300 nm-thick SiO₂/Si wafer is suspended between those two seed reservoirs. All of these three substrates are faced down and placed on a crucible containing molybdenum oxide (MoO₃, 99.98%) powder precursor. This MoO₃ precursor is put in the middle of a quartz tube reaction chamber and another sulfur powder (99.98%) precursor is placed upstream in the quartz tube. Before heating, the CVD system is purged using 1000 sccm of Ar (99.999% purity) for 5 minutes. Next, the flow rate of Ar is switched to 20 sccm as the carrier gas for the MoS₂ growth, and the temperature of the reaction chamber is increased to 625 °C at a rate of 30 °C min⁻¹. The monolayer MoS₂ is synthesized at 625 °C for 3 min under atmospheric pressure.

CVD of monolayer WS₂. A simple method for deposition of monolayer WS₂ crystals at atmospheric pressure is utilized. Tungsten trioxide (WO₃) powder is sprayed onto a piece of SiO₂/Si wafer, acting as a WO₃ reservoir during the deposition. The SiO₂/Si target substrate is positioned face-up and downstream, 1 cm away from the WO₃ reservoir. A crucible containing sulfur powder is placed upstream. Prior to the growth, the reaction chamber is purged using 1000 sccm of Ar for 5 minutes. Then the furnace temperature is ramped to 800 °C at a rate of 39 °C/min and the deposition of monolayer WS₂ crystals is implemented at 800 °C for 5 minutes with 50 sccm of Ar carrier gas.

CVD of monolayer WSe₂. A (NH₄)₂WO₄ aqueous solution (2 mg/mL) is spin-coated (2500 rpm for 1 min) onto a SiO₂/Si substrate, and then placed in the center of the furnace. Se powder (30 mg, 99.5%, Sigma-Aldrich) is loaded upstream about 17 cm away from the center. Before the growth, the tube is flushed with 300 sccm of Ar for 10 minutes to eliminate residual oxygen and moisture. During the growth, the temperature is increased to 900 °C at a rate of 50 °C/min and the growth lasts for 10 minutes with 30 sccm of Ar and 10 sccm of H₂ flow as the carrier gases. After the growth, the furnace is rapidly cooled to room temperature.

Mechanically exfoliation of monolayer WS₂ and WSe₂. Monolayer WS₂ and WSe₂ flakes are mechanically exfoliated onto the 100-nm-thick SiN_x dielectrics by the standard scotch tape technique. Prior to device fabrication, the exfoliated TMD flakes are immersed in acetone for 3 hours to remove the tape residues. Raman spectroscopy are performed on the selected TMD flakes to confirm their monolayer characteristics for further device fabrication as shown in Extended Data Fig. 5a.

Transfer of monolayer transition metal dichalcogenides (TMDs) on dielectric/Si substrates.

The monolayer TMD crystals grown by MOCVD or CVD are transferred onto the dielectric/p⁺⁺-Si substrates for device fabrication using a wet transfer process. First, poly(methyl methacrylate) (PMMA) is spin-coated onto the monolayer TMD samples. Then, the PMMA/TMD stacks are released from the SiO₂/Si growth substrate by etching in a concentrated potassium hydroxide (KOH) aqueous solution at 90 °C. The freestanding PMMA/TMD stacks are picked up, rinsed with deionized water three times for 2 hours, and then attached onto the target substrates. In order to dry the samples and enhance the adhesion, the PMMA/TMD stacks are baked on the hotplate at 70 °C for 20 minutes and 130 °C for another 20 minutes. Finally, the sample is immersed in cold acetone for at least 6 hours to remove the PMMA.

Device fabrication and characterization. Monolayer TMD crystals are confirmed by Raman and PL characterization and then selected for transistor fabrication. Electron-beam (e-beam) lithography is used to define the channel and the source/drain contacts with PMMA e-beam resists (MicroChem). Metallization is implemented by e-beam evaporation of 20-nm bismuth with a well-controlled deposition rate of 0.5 angstrom (Å)/second (s), followed by an Au capping layer (10–100 nm, at 2 Å/s) at $\sim 10^{-6}$ torr. Liftoff process is carried out in hot acetone. No annealing or chemical doping treatment is performed on the devices. The channel widths for the devices in this study are in the range of 2 to 10 μm . All electrical characterization is conducted in a vacuum environment (10^{-5} - 10^{-6} torr) in a Lakeshore probe station using an Keysight B1500A semiconductor parameter analyzer. The electrical resistivity of the evaporated bismuth film on monolayer MoS₂, and on SiN_x are measured to be $9.0 \times 10^{-6} \Omega\cdot\text{m}$ and $9.5 \times 10^{-6} \Omega\cdot\text{m}$, respectively. The gate dielectrics for the monolayer TMD transistors studied in this work include 300-nm-thick SiO₂ (NOVA Electronic Materials) and 100-nm-thick SiN_x (MTI Corporation). To estimate the sheet carrier density and carrier mobility of the devices accurately, the capacitances for the dielectrics are measured at 1 MHz with Keysight B1505A power device analyzer on separate metal-insulator-metal capacitors at room temperature.

Sample preparation for Raman and XPS characterizations. First, a 20-nm of bismuth thin film is deposited on a continuous monolayer MoS₂ film grown on a SiO₂/Si wafer followed by an Au capping layer using e-beam evaporation. Next, the heterostructure of Au-Bi-MoS₂ can be peeled off by a thermal tape due to the relatively weak interaction between the MoS₂ film and the silica substrate. Finally, the sample is inverted to expose the continuous MoS₂ film on top of the bismuth film for characterization. In this way, a pristine Bi-MoS₂ interface can be studied without oxidation of bismuth. This method allows us to directly carry out the Raman and XPS characterizations on the Bi-MoS₂ interface.

Raman spectroscopy. Raman spectroscopy of monolayer MoS₂ flakes is carried out on a confocal Raman system of HR800 (Horiba Scientific) with a laser wavelength of 523 nm at the laser power of 2.5 mW and accumulation time of 0.5 second. The emitted Stokes Raman signal is collected by a 0.9 N.A. of 100X objective of Carl Zeiss Microscopy GmbH with an 1800 lines/mm grating for the measurements. The spectrum is calibrated by the silicon characteristic peak at 520.6 cm^{-1} from an undoped silicon wafer.

X-ray photoelectron spectroscopy (XPS) analysis. The XPS measurement is carried out by using a PHI Versaprobe II XPS instrument with monochromated Al K α source (1486.6 eV) and a spot size of 200 μm . 50 W gun power and 15 kV operation voltage are used during spectrum acquisition. During the measurement, samples are flooded with electron and Ar ion guns to

compensate the surface charging. All the XPS spectra presented in this work are calibrated by the C1s peak at 284.8 eV. The XPS spectra are analyzed and fitted by Gaussian/Lorentzian mix function.

Transmission electron microscope (TEM) analysis. The transmission electron microscope (TEM) is performed using FEI Tecnai (G2 Spirit TWIN) under 120 kV. The selected-area electron diffraction (SAED) images are taken with a 1 μm selected-area aperture. The Bi/MoS₂ freestanding sample is prepared by direct e-beam evaporation of Bi and Au on top of freestanding monolayer MoS₂ sample on Protochips C-Flat TEM grid (2/4) as illustrated in Extended Data Fig. 3a, e. The streaks connecting the diffraction pattern of Bi in SAED originate from the diffusive scattering of grain boundaries of Bi.

Extraction of Schottky barriers. A 2D Schottky FET can be regarded as two Schottky diodes connected back-to-back. Most of the applied drain-to-source voltage (V_{DS}) drops at the reverse-biased contact. Therefore, for an n-channel FET the transistor behavior is dominated by the source side. The drain current density (I_{DS} , in units of $\mu\text{A}/\mu\text{m}$) thermally injected from the metal contact into the 2D channel through a reverse-biased Schottky barrier (SB) can be expressed as:

$$I_{\text{DS}} = A_{2\text{D}}^* T^{1.5} \exp\left(-\frac{\Phi_{\text{B}}}{k_{\text{B}}T}\right) \left[1 - \exp\left(\frac{-V_{\text{DS}}}{k_{\text{B}}T}\right)\right] \quad (1)$$

where $A_{2\text{D}}^* = q(8\pi k_{\text{B}}^3 m^*)^{0.5} / h^2$ is the Richardson constant for a 2D system, T is the temperature, k_{B} is Boltzmann's constant, q is the elementary charge, and Φ_{B} is the effective contact barrier height at a given gate-source voltage (V_{GS}). If $V_{\text{DS}} \gg k_{\text{B}}T$, equation (1) can be simplified to

$$I_{\text{DS}} \approx A_{2\text{D}}^* T^{1.5} \exp\left(-\frac{\Phi_{\text{B}}}{k_{\text{B}}T}\right) \quad (2)$$

In this way, the effective energy barrier at a given V_{GS} can be extracted by finding the slope in the Arrhenius plots, as shown in Extended Data Fig. 2a, using the following equation:

$$\ln(I_{\text{DS}} / T^{1.5}) = \frac{-\Phi_{\text{B}}}{k_{\text{B}}T} + c \quad (3)$$

where c is a constant. Φ_{SB} is then extracted at the flatband condition ($V_{\text{GS}} = V_{\text{FB}}$)², as shown in Extended Data Fig. 1c, f, i.

However, the Arrhenius plots of Bi-contacted MoS₂ FETs display an opposite trend to the thermionic emission model [equation (3)]. As shown in Extended Data Fig. 2b, the Arrhenius plots of the Bi-MoS₂ transistors can be divided into two regimes: (i) a positive slope regime where the mobility increases with a decreasing temperature (150 – 300 K) and (ii) a saturation-like regime where the mobility reaches constant at even lower temperatures (77 – 150 K). For an ideal transistor with a zero contact barrier, the thermionic emission model gives rise to a zero slope in the Arrhenius plot when ignoring the contribution of the channel resistance. However, in our devices the drain current is dominated by the channel resistance, so the temperature dependence of the MoS₂ mobility needs to be considered, which contributes to the increase in drain current density (I_{DS}). Therefore, the positive slopes within the range of 150 – 300 K originate from the enhancement of MoS₂ mobility due to the reduced phonon scattering. Once

the mobility gradually reaches a constant due to scattering of long-range Coulomb impurities or short-range atomic defects in the range of 77 – 150 K, the slopes of the Arrhenius plots tend to saturate, which implies the contact barrier-free nature of the Bi-MoS₂ FETs.

Extraction of contact resistance through transfer length method (TLM). In a 2-terminal device, the major resistance components originate from the contact resistance (R_C) and the channel resistance (R_{CH}). As a result, the total device resistance (R_{TOT} , in units of $k\Omega \mu m$) normalized by channel width (W) can be expressed as $R_{TOT} = 2R_C + R_{CH} = 2R_C + R_{SH}L_{CH}$, where R_{SH} is the sheet resistance of the semiconductor channel (in units of $k\Omega/\square$) and L_{CH} is the channel length. The total device resistance varies linearly with the L_{CH} if the R_C (in units of $k\Omega \mu m$) and R_{SH} are spatially homogeneous in the device. Therefore, by measuring the total resistances of the devices with various L_{CH} , the R_{TOT} can be plotted as a function of L_{CH} . The residual resistance at $L_{CH} = 0$ corresponds to the total contact resistance ($2R_C$) of the device.

Accordingly, we extract the R_C of the Bi-MoS₂ transistors for a given carrier density (n_{2D}) by plotting the R_{TOT} versus L_{CH} as shown in Fig. 2c and Extended Data Fig. 2c, d. The vertical intercept at $L_{CH} = 0$ of a linear fit yields the $2R_C$ for the two-terminal Bi-MoS₂ devices. Also, the R_{SH} of the MoS₂ channel for a certain n_{2D} can be calculated from the slope of the linear fit. The effective mobility is then calculated by $\mu = 1/(qn_{2D}R_{SH})$. The n_{2D} induced by electrostatic gating is estimated by assuming a simple linear charge dependence on the gate voltage overdrive $n_{2D} = C_{ox}(V_{GS} - V_T)/q$, where C_{ox} is the capacitance per unit area of the gate dielectric and is experimentally characterized by standard capacitance-voltage (C - V) measurement ($C_{ox} \sim 6 \times 10^{-8}$ F/cm² for the 100-nm-thick SiN_x dielectrics used in this study), and V_T is the threshold voltage linearly extrapolated from the transfer characteristic curve of the device. As shown in Fig. 2c and Extended Data Fig. 2d, the good linear fits to the R_{TOT} vs L_{CH} indicate uniform channel materials and electrical contacts.

The accuracy of the R_C extraction can be improved by: (I) a more efficient gate with higher gate capacitance (100 nm SiN_x instead of 300 nm SiO₂), so that the carrier density, and thus the sheet resistance (slopes of Fig. 2c and Extended Data Fig. 2d) can be substantially reduced; (II) shorter channel lengths so that the data points are closer to the y-axis intersection ($2R_C$); and (III) samples with minimal variation in terms of V_T and μ . With the consideration of these factors we estimated the mean and the fitting uncertainty of the R_C value of our best Bi-MoS₂ device to be $123 \pm 63 \Omega \mu m$.

Extraction of field-effect mobility from 2-terminal and 4-terminal devices. From the transfer curves (I_{DS} - V_{GS}) of a 2-terminal MoS₂ device, the field-effect mobility is extracted using the expression $\mu = 1/(qn_{2D}R_{SH}) \approx (dI_{DS}/dV_{GS}) \times [L_{CH}/(WC_{ox}V_{DS})]$. Note that this field-effect mobility typically represents the lower limit because of contact resistance in the devices.

In a 4-terminal configuration, a bias current (I_{DS}) is applied between the two outer electrodes (D and S), while the voltages on the two inner electrodes are measured (V_1 and V_2). Ideally, the current path in the material should not be affected by the inner sense electrodes, which allows for an accurate assessment of the channel resistivity and thus the intrinsic mobility. We calculate the channel resistance as $R_{SH} = (V_2 - V_1)/I_{DS} \times (W/L_{21})$, where L_{21} is the length between the inner voltage contacts. The 4-terminal field-effect mobility can be calculated by $\mu = 1/(qn_{2D}R_{SH}) = (dI_{DS}/dV_{GS}) \times [L_{21}/(WC_{ox}V_{21})]$, where V_{21} is the voltage difference between the two inner electrodes.

First-principles calculations. We build a model with three layers of Bi with its (0001) surface in contact with monolayer MoS₂. A vacuum slab of 10 angstroms is used for separating the cells to mimic the 2D system. The layer thickness of Bi is proved to be adequate given that very little electronic structure is changed at the second Bi layer (counting from Bi-MoS₂ interface), and almost no electronic structure is changed on the third layer demonstrated in the differential charge plot in Fig. 3c. The supercell of MoS₂ is a 5×5 replicate of its unit cell, and the supercell of Bi is a 3×3 replicate of its redefined unit cell. The lattice mismatch between these two supercells is only 0.1%, making the structure stable during the ionic relaxation steps in the first-principles calculations.

The first-principles calculations for geometric optimization and the electronic properties of crystal structure are carried out using density functional theory and projector augmented wave (PAW) method implemented in the Vienna Ab-initio Simulation Package (VASP)⁵¹. The semilocal generalized gradient approximation (GGA) in the form of Perdew-Burke-Ernzerhof (PBE), and the PAW pseudopotentials are adopted. During the ionic optimization steps, the Hellman-Feynman forces of single atoms are optimized to be less than 0.02 eV/Å, where the energy cutoff is set to be 400 eV and only gamma point is used for k space sampling. In the density of states (DOS) calculation, k points for the supercell are chosen to be 9×9×1 and an energy cutoff is set to be 400 eV, and the single electronic step is converged to 1×10⁻⁵ eV. Dipole correction along the z axis is implemented in all the DFT calculations, which is especially important for electrostatic potential calculations. The orbital projected local density of states (PLDOS) is a projection of total DOS into each orbital and further into the sphere of atoms natively defined in VASP code. Spin-orbit coupling is not included in generating Fig.3 but has been tested in a smaller Bi-MoS₂ system where Fermi level is proved to be still located at CBM. The one-dimensional electrostatic charge potential along the z axis is calculated from Poisson's equation where the charge density per unit length is acquired by integrating the charge along the xy plane from the DFT calculation. According to Bader charge analysis, there are 0.88 electron/supercell transferred from Bi to MoS₂, which is equivalent to an electron doping of 4×10¹¹ cm⁻².

Analysis of contact resistance with transmission line model. The contact resistance (R_C) measured from the TLM originates from two components: (I) transport through the metal-semiconductor energy barrier, and (II) lateral access resistance under the contact due to the sheet resistance (R_{SH}) of the channel material. We employ the transmission line model for R_C , expressed as^{11,33}:

$$R_C = \sqrt{\rho_C R_{SH}} \cot \left[\left(\frac{L_C}{L_T} \right) \right] \approx \sqrt{\rho_C R_{SH}}, \text{ if } L_C \gg L_T \quad (4)$$

where R_C is normalized by W in units of $\Omega \mu\text{m}$, ρ_C is specific contact resistivity accounting for the vertical interlayer transport under the contact, L_T is the current transfer length, and L_C is the physical contact length (1 μm in this study). The R_{SH} here is extracted from the slopes of the TLM plots.

We estimate that $\rho_C \approx 8.8 \times 10^{-9} \Omega \text{ cm}^2$ at $n_{2D} = 1.5 \times 10^{13} \text{ cm}^{-2}$ for the Bi-MoS₂ FETs on 100-nm-thick SiN_x at room temperature. Based on the definition of current transfer length L_T

$$L_T = \sqrt{\frac{\rho_C}{R_{SH}}} \quad (5)$$

we evaluate the best L_T to be around 7 nm at room temperature, much smaller than the L_C used in our devices, justifying the use of the approximation in equation (4). These results suggest that the dimension of the contacts for the Bi-MoS₂ FETs can be reduced to ~ 7 nm without performance degradation resulting from the current crowding effect.

Extended Data Fig. 9a plots the fractions of the total contact resistance ($2R_C$) and the intrinsic channel resistance (R_{CH}) with respect to the total device resistance (R_{TOT}) as a function of L_{CH} using $R_C = 123 \Omega \mu m$ and mobility $\sim 20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ as extracted from the our Bi-MoS₂ FETs on 100-nm SiN_x (Fig. 2c). Extended Data Fig. 9b shows $2R_C$ versus L_{CH} for different contact technologies. It can be seen that R_C does not dominate the performance of Bi-MoS₂ FETs until the L_{CH} reaches ~ 7 nm, providing a significant improvement in the scaling limit of TMD transistors.

Equivalent circuit model for the contact resistance of Bi-MoS₂ FET. Based on the first-principles calculation and the experimental results, we built an equivalent circuit for the Bi-MoS₂ contact region (Fig. 3d). The contact resistance is composed of a network of the vdW gap tunneling resistors (with the tunneling specific resistivity ρ_t) and the Bi-contacted MoS₂ resistors (with the sheet resistance $R_{SH,C}$). Since the barrier height at the Bi-MoS₂ interface is negligible, we do not consider the contact resistance contribution due to the thermionic emission at the SB. The tunneling current density (J_t) through the vdW barrier can be obtained through Simmon's model^{52,53},

$$J_t = \frac{q}{4\pi^2 \hbar w_t^2} \left\{ \left(\Phi_t - \frac{qV}{2} \right) \exp \left[-2 \frac{(2m_e)^{1/2}}{\hbar} \alpha w_t \left(\Phi_t - \frac{qV}{2} \right)^{1/2} \right] - \left(\Phi_t + \frac{qV}{2} \right) \exp \left[-2 \frac{(2m_e)^{1/2}}{\hbar} \alpha w_t \left(\Phi_t + \frac{qV}{2} \right)^{1/2} \right] \right\} \quad (6)$$

where w_t is the tunneling gap width; Φ_t is the tunneling barrier height; α is an empirical factor that is associated with the shape of the barrier ($\alpha=1$ for an ideal square barrier); V is the bias voltage; q is the electron charge; $\hbar$ is the reduced Planck's constant; and m_e is the free electron mass. At low bias ($qV \ll \Phi_t$), the tunneling specific resistivity is given by

$$\rho_t = \left(\frac{dJ_t}{dV} \right)^{-1} \approx \frac{4\pi^2 \hbar w_t^2}{q^2} \frac{\exp \left(2 \frac{(2m_e)^{1/2}}{\hbar} \alpha w_t \Phi_t^{1/2} \right)}{\frac{(2m_e)^{1/2}}{\hbar} \alpha w_t \Phi_t^{1/2} - 1} \quad (7)$$

According to our DFT calculation results, $w_t \approx 1.66 \text{ \AA}$, and $\Phi_t \approx 3.6 \text{ eV}$. We therefore estimate that $\rho_t \approx 1.81 \times 10^{-9} \Omega \text{ cm}^2$ for our Bi-MoS₂ contact.

In addition $R_{SH,C}$ is estimated to be 15.6 k Ω if assuming the 2D carrier density of Bi-contacted MoS₂ is around $2 \times 10^{13} \text{ cm}^{-2}$. Then the contact resistance is $R_C = (\rho_t R_{SH,C})^{1/2} + R_{SB0}$, where $R_{SB0} = k_B T / (q A_{2D}^* T^{3/2})$ is the residual contact resistance (according to the thermionic

model, eq. (1)) for a zero SB height. The contact resistance for Bi-MoS₂ is calculated to be 0.13 kΩ μm, in very good agreement with our measured values.

Velocity saturation, critical channel length (L_{cr}) and scaling rules in Bi-TMD transistors. In the linear regime, the transistor on-state current density (I_{ON}) is approximately determined by the total device resistance ($R_{TOT} = 2R_C + R_{CH}$), and the I_{ON} increases linearly with the applied V_{DS} at a given R_{CH} which can be modulated by the gate voltage. By taking the contact resistance into account, the effective drain-to-source voltage (V'_{DS}) dropped across the TMD channel is $V'_{DS} = V_{DS} - 2R_C I_{ON}$. As the V_{DS} increases and/or the channel length reduces, at a certain point where the lateral field becomes greater than the critical field strength (F_C) in the TMD material, the conducting electron in the TMD channel is accelerated to its saturation velocity (v_{sat}) and the I_{ON} saturates to a maximum of $I_{ON} = n_{2D} q v_{sat}$. In this velocity saturation regime, the I_{ON} in the transistor thus scales only linearly with n_{2D} induced into the TMD channel through electrostatic gating. Accordingly, for I_{ON} of 450 μA μm⁻¹ shown in Fig. 4a, the v_{sat} of monolayer MoS₂ is extracted to be $\sim 2.5 \times 10^6$ cm/s at an n_{2D} of $\sim 10^{13}$ cm⁻².

At a fixed V_{DS} and gate bias, there is a transition from the linear regime to the velocity saturation regime when the L_{CH} of the transistor reduces to L_{cr} , and the TMD channel reaches its critical field strength

$$F_C = \frac{V'_{DS}}{L_{cr}} = \frac{V_{DS} - 2R_C n_{2D} q v_{sat}}{L_{cr}} \quad (8)$$

Taking MoS₂ as an example, the F_C is 1.15×10^5 V/cm⁵⁴. Therefore, for a Bi-MoS₂ transistor with $R_C \sim 123$ Ω μm biased at a V_{DS} of 1.5 V with a n_{2D} of 1.5×10^{13} cm⁻², the L_{cr} is ~ 117 nm, which agrees with our experimental results. On the other hand, with the same device dimension and bias conditions, a higher R_C would drive the TMD channel to operate below F_C , or in linear regimes, with smaller I_{DS} than the saturation current; therefore, a larger V_{DS} is required to reach the maximum I_{ON} (saturation current) at a similar device dimension, limiting the allowed minimum power supply voltage.

For future transistor scaling, a low supply voltage (V_{DD}) is required. We further consider the minimum V_{DS} to bias the Bi-MoS₂ transistor in its velocity saturation regime while satisfying the IRDS target I_{ON} for high-performance and low-power logic transistors. Due to the short current transfer length of Bi contact ($L_T \sim 7$ nm), the R_C would remain low without significant current crowding even with a reduced contacted gate pitch (CGP = $L_{CH} + L_C$) used in the future technology node (i.e. $L_T < L_C$)³⁷. Thus, the minimum V_{DS} for Bi-TMD transistors to meet the target I_{ON} in different future technology nodes is shown in Extended Data Fig. 9c, d.

$$V_{DS,min} = F_C L_{CH} + 2R_C I_{ON} \quad (9)$$

The projection as shown in Fig. 4e suggests that the Bi contact to TMDs can potentially meet the IRDS requirements for future energy-efficient electronics. A n_{2D} of 4.5×10^{13} cm⁻² is assumed based on the use of a 3-nm ultrathin gate dielectric with a dielectric constant (κ) of 15 and an overdrive of 1.6 V. This condition corresponds to a vertical electric field of 5.3 MV/cm in the dielectric, which lies below its breakdown strength (F_{BD}) of 6.2 MV/cm ($F_{BD} = 35\kappa^{0.64}$)⁵⁵.

Bi Contacts for Other Monolayer TMDs and Effects of TMD Quality. We would like to point out that a high sample quality is the prerequisite for the proposed GSS mechanism. Both our DFT calculation (Extended Data Fig. 4b) and experiment observations (Extended Data Fig. 8 and Extended Data Table 1) indicate that a high density of structural defects such as chalcogen vacancies tend to obstruct the formation of ohmic contact while the gap-state pinning mechanism becomes dominant at the contact interface.

To study the effects of material quality, monolayer TMD crystals with different sample conditions are contacted with Bi electrodes and their electrical characteristics are measured. Since CVD normally exhibits a high variation in local concentrations of precursors along the growth substrate, CVD-grown TMD crystals typically show a larger variation in the sample quality. Extended Data Fig. 8a shows the output characteristics of a device based on a CVD-grown monolayer MoS₂ crystal possessing poor sample quality (i.e. non-clean surface with curved edges). The lower I_{DS} and the nonlinear I_{DS} - V_{DS} curves resulting from this device suggest the presence of contact barrier and imply that GSP takes over the band alignment mechanism at the MoS₂ surface, which is further confirmed by DFT calculation (Extended Data Fig. 4b). In our experiments, we note that MOCVD-grown MoS₂ crystals exhibit a higher homogeneity and reproducibility and low variation in sample quality likely due to the well-controlled flow rate of the precursors during the deposition (Extended Data Fig. 8b).

For the case of monolayer WSe₂, similar variation in the contact performance is also observed in CVD-WSe₂ devices. The aged sample with a defective surface (i.e. holes and cracks) even turns to p-type conduction with a low I_{DS} , which manifests the strong GSP at the metal-TMD interface where the Fermi level is aligned closer to the valence band of WSe₂, as shown in Extended Data Fig. 8e, f. This GSP effect is mitigated when a WSe₂ crystal with reasonable quality is utilized and the device behavior changes to ambipolar, indicating that the Fermi-level is pinned upward at a position closer to the CBM (Extended Data Fig. 8g, h). As Bi electrodes are in contact with a high-quality, freshly exfoliated WSe₂, the ohmic characteristics become prevalent at the Bi-WSe₂ interface, giving rise to a good ohmic contact and the significantly enhanced n-type conduction (Extended Data Fig. 8i, j). Note that good ohmic contacts can be also formed on CVD monolayer TMDs when a high-quality sample is obtained (Extended Data Fig. 8c, d).

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Extended Data Fig. 1 | Temperature-dependent electrical characteristics. **a,b**, Typical $I_{\text{DS}}-V_{\text{DS}}$ curves at 150 K (**a**) and 77 K (**b**) for the Bi-MoS₂ FET. The device exhibits linear output characteristics at all the temperatures measured. **c**, Schottky barrier height (Φ_{SB}) extraction for the Bi-MoS₂ FET, showing a negligible contact barrier. Inset: Logarithmic plot of the $I_{\text{DS}}-V_{\text{DS}}$ curve at 77 K and $n_{2\text{D}} \sim 4 \times 10^{12} \text{ cm}^{-2}$, demonstrating ohmic contact in the Bi-MoS₂ FETs. **d,e**, Typical $I_{\text{DS}}-V_{\text{DS}}$ curves at room temperature (**d**) and 77 K (**e**) for the Ni-MoS₂ FET. The nonlinear output characteristics at low temperatures suggest the existence of SB at the Ni-MoS₂ junction. **f**, Schottky barrier (Φ_{SB}) extracted by equation (3) as a function of the gate voltage for the Ni-MoS₂ FET. Φ_{SB} is around 100 meV at the flatband voltage (the elbow of the curve)². **g**, Typical $I_{\text{DS}}-V_{\text{GS}}$ curves of the Ti-MoS₂ FET. **h**, Typical $I_{\text{DS}}-V_{\text{DS}}$ curves at 77 K for the Ti-MoS₂ FET. Similar to the Ni-MoS₂ device, the Ti-MoS₂ FET exhibits both drain-current suppression and obviously nonlinear output characteristics at low temperatures due to the presence of a SB at the Ti-MoS₂ interface. **i**, Extracted Φ_{SB} for the Ti-MoS₂ FET as a function of the gate voltage, which is around 150 meV at the flatband voltage.

Extended Data Fig. 2 | Arrhenius plots and extraction of contact resistance. **a,b**, Arrhenius plots of Ni-contacted (**a**) and Bi-contacted (**b**) monolayer MoS₂ FETs. The two transistors yield opposite slopes derived from equation (3), reflecting different M-S junction configurations. The good agreement between the data extracted from the Ni-MoS₂ FET and the thermionic emission model suggests the thermally activated electronic transport at an energy barrier, that is, the Schottky barrier (SB) at the Ni-MoS₂ interface. In contrast, the deviation from the thermionic emission model and nearly saturated slopes at low temperatures observed in the Bi-MoS₂ FET indicate the disappearance of an energy barrier for electron injection. The light blue curve represents the off-state of the Bi-MoS₂ FET biased at a negative gate voltage of -60 V. The device at this condition shows a negative slope in the Arrhenius plot and the effective barrier height is extracted to be ~ 130 meV. This barrier originates from the energy difference between the Fermi level of the degenerate MoS₂ underneath Bi and the conduction band minimum of the depleted MoS₂ channel. **c**, Transfer characteristics, $I_{DS}-V_{GS}$, of Bi-contacted monolayer MoS₂ FETs on 100-nm-thick SiN_x with various channel lengths (L_{CH}) at a V_{DS} of 0.5 V for the TLM study. **d**, Plots of total device resistance R_{TOT} (normalized by width) versus L_{CH} for the Bi-MoS₂ FETs at various carrier densities, from which the total contact resistance ($2R_C$) can be extracted from the y -axis interceptions. Symbols are experimental data and lines are linear fits in (**a**) and (**d**).

Extended Data Fig. 3 | SAED patterns of the freestanding Au/Bi/1L-MoS₂ and Au/Bi/amorphous-carbon. **a,e**, Schematics of the Au/Bi layer deposited directly on the monolayer MoS₂ and amorphous carbon (a-carbon) in the TEM grid, respectively. **b-d**, SAED patterns of Au/Bi/1L-MoS₂ at three different locations. The [0001] zone axis of Bi is always observed in parallel to the electron beam throughout the whole sample. The diffraction spots of MoS₂ at 3.6 nm⁻¹ can be clearly identified. The in-plane rotation of MoS₂ with respect to Bi (0001) plane is 30°, 4° (to the nearest Bi diffraction spots), and 8°, respectively. For most of the areas, Bi demonstrates homogeneous orientation as shown in **(b)** and **(d)**, but polycrystalline areas can also be found as shown in **(c)**. The selected-area aperture is 1 μm. **f**, The diffraction ring located at 3.0 nm⁻¹ is identified to be from Bi₂O₃ polycrystal, as confirmed from **(g)** the atomic structure of Bi₂O₃ viewing at zone axes [110], and its simulated diffraction pattern shown in **(h)** demonstrating the diffraction pattern at 3.0 nm⁻¹.

Extended Data Fig. 4 | DFT results for Sb-MoS₂, Bi-MoS₂ with sulfur vacancy, and Bi-WS₂.
a, Projected local density of states (PLDOS) of MoS₂ before (upper panel) and after (lower panel) in contact with Sb. The valence band (VB) is shaded in light blue and conduction band (CB) in light red. Fermi level (E_F) is shifted from VBM inside the gap (before Bi contact) into CB (after Bi contact). **b**, **c**, LDOS of MoS₂ with a sulfur vacancy (**b**) and WS₂ (**c**) when in contact with Bi, respectively. Fermi level is pinned at the sulfur vacancy defect state inside the band gap. This implies that a high-quality TMD crystal with a low defect density is critical to form ohmic contact to Bi. The result of LDOS of WS₂ in contact with Bi, predicting that ohmic contact can also be formed at Bi-WS₂ interface due to GSS.

Extended Data Fig. 5 | Characterization of transition metal dichalcogenide monolayers. **a**, Raman characterization of MOCVD-grown monolayer MoS₂ (blue) and mechanically exfoliated WS₂ (green) and WSe₂ (red) monolayers for device fabrication. **b**, Raman characterization of Ni-MoS₂ and Au-MoS₂ interfaces. Samples are prepared using the mechanically tape-assisted exfoliation. No significant shifts in A_{1g} are observed for Ni and Au contacts. The shift in E'_{2g} is prevalently observed in the metal-MoS₂ system, likely originating from the strain induced at metal-MoS₂ boundary. **c**, Deconvolution of the XPS spectra of S2p and Bi4f for pristine monolayer MoS₂ and Bi-contacted MoS₂. The blueshifted core-level binding energies for the Bi-contacted MoS₂ indicate the upward shift of its Fermi level induced by the Bi contact, which is in good agreement with the DFT calculation and the Raman spectroscopy analysis. Moreover, the absence of characteristic peaks for Bi₂O₃ suggest that the Bi contact is free of oxidation when in contact with MoS₂, which is well consistent with the TEM results (Fig. 3b and Extended Data Fig. 3).

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901 **Extended Data Fig. 6 | Transfer characteristics of monolayer WS_2 and WSe_2 FETs with Bi**
 902 **contacts. a, b,** Typical transfer characteristics of Bi- WS_2 (a) and Bi- WSe_2 (b) FETs on 100 nm
 903 SiN_x at room temperature. Both transistors exhibit n-type conduction with a high $I_{\text{ON}}/I_{\text{OFF}}$ ratio of
 904 $> 10^7$.

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907 **Extended Data Fig. 7 | Record-high- I_{ON} monolayer MoS₂ transistors.** **a**, Transfer
 908 characteristics of a 35-nm L_{CH} Bi-MoS₂ FET. **b,c**, Transfer and output characteristics of a 50-nm
 909 L_{CH} Bi-MoS₂ FET. **d**, Output characteristics of a 120-nm L_{CH} Bi-MoS₂ FET. The excellent
 910 current-delivery capacities represent new records for monolayer MoS₂ at these device
 911 dimensions, outperform thicker TMD devices, and are comparable to 3D semiconductor devices
 912 such as 90-nm node strained Si and AlGaAs/InGaAs HEMT transistors with similar channel
 913 lengths^{38,39,45}. Note that the required drain voltage for the ohmic Bi-monolayer MoS₂ FET to
 914 achieve a high I_{ON} is relatively small compared to previously reported high-performance TMD
 915 transistors (i.e. typically $V_{DS} > 2$ V with a thicker channel thickness)^{18,22,30-33,41-44}. Inset: optical
 916 microscopic image of the device. **e**, Semi-logarithmic plot of the transfer characteristic of a
 917 different Bi-MoS₂ FET showing an excellent I_{ON}/I_{OFF} ratio of 10^8 . Insets: SEM image of a
 918 representative 150-nm- L_{CH} Bi-contacted monolayer MoS₂ FET on 100-nm-thick SiN_x and its
 919 channel region. **f**, Output characteristics of the same Bi-MoS₂ transistor in (**e**). The drain current
 920 saturates at V_{DS} of ~ 1.5 V and scale linearly with the gate voltage, which suggests that the
 921 electrons traveling in the monolayer MoS₂ channel reach its saturation velocity. The gate
 922 dielectrics of devices presented in this figure are 100 nm SiN_x.

Extended Data Fig. 8 | Effects of TMD quality on the output characteristics. **a,b**, Sample-quality-dependent contact performance for the case of monolayer MoS₂. The room-temperature output characteristics of the Bi-MoS₂ transistors fabricated with a CVD-grown defective MoS₂ monolayer **(a)** (Inset: optical image of a typical low-quality MoS₂ crystal with a non-clean surface and curved edges, scale bar: 5 μm) and MOCVD-grown MoS₂ monolayer **(b)** (Inset: optical image of a typical high-quality MoS₂ crystal with a clean surface, scale bar: 10 μm). **c,d**, Output characteristics of Bi-contact transistors fabricated with fresh CVD-grown monolayer WS₂ **(c)** and monolayer WSe₂ **(d)** FETs, showing that the proposed GSS-induced ohmic contact can also be formed on high-quality WS₂ and WSe₂ CVD samples. **e,f**, Room-temperature output characteristics **(e)** and transfer curves **(f)** of the Bi-WSe₂ transistors fabricated with an aged CVD-grown WSe₂ monolayer (low quality). Scale bar: 10 μm . **g,h**, Room-temperature output characteristics **(g)** and transfer curves **(h)** of the Bi-WSe₂ transistors fabricated with a fresh

CVD-grown WSe₂ monolayer (medium quality). Scale bar: 10 μm. **i,j**, Room-temperature output characteristics **(i)** and transfer curves **(j)** of the Bi-WSe₂ transistors fabricated with a mechanically exfoliated WSe₂ monolayer (high quality). Scale bar: 5 μm. The results show a clear evolution from p-type conduction to enhanced n-type conduction with the sample quality improvement. These variations could be attributed to the GSP effect induced by the chalcogen vacancies (Extended Data Fig. 4b). Insets in **(f)**, **(h)**, and **(j)** are the optical images of a typically low-quality CVD WSe₂ crystal with an obviously defective surface, a medium-quality CVD WSe₂ with an irregular crystal shape, and a freshly high-quality exfoliated WSe₂ with a clean surface, respectively.

Extended Data Fig. 9 | Performance projection of Bi-monolayer TMD technology. **a**, Fraction of channel resistance (R_{CH} , green line) and total contact resistance ($2R_C$, blue line) with respect to the total device resistance ($R_{TOT} = R_{CH} + 2R_C$) in Bi-MoS₂ FETs as a function of the channel length (L_{CH}) at room temperature based on the device and material parameters extracted from Fig. 2c. The dash lines show the quantum limit, representing the minimum R_C that can be achieved in a transistor. The quantum limit R_C is $\pi h / (4q^2 k_F) \sim 0.036(n_{2D})^{-0.5}$ k Ω μ m, which is determined by the quantum resistance ($h/2q^2 \approx 12.9$ k Ω) and the number of conducting modes per channel width (k_F/π) which is related to the 2D sheet carrier density (n_{2D} , in units of 10^{13} cm⁻²). **b**, Projection of $2R_C$ as a function of the contact length (L_C) in monolayer TMD transistors based on the transmission line model with various metal contacts at room temperature. The vertical dashed line represents the current transfer length (L_T) for each metal contact. The results are calculated based on the data extracted from previously reported TLM results^{13,46}. As can be seen, R_C increases as L_C becomes comparable to L_T due to the current crowding effect [equation (4)]¹⁸. Note that In, hexagonal boron nitride (hBN)/Co, Ni, and high-vacuum Au contacts to

965 monolayer MoS₂ exhibit similar values of R_C ($\sim 3\text{--}6\text{ k}\Omega\text{ }\mu\text{m}$) and ρ_C ($\sim 10^{-6} - 10^{-5}\text{ }\Omega$
966 cm^2)^{13,14,18,49}. **c**, Required minimum V_{DS} for Bi-contacted monolayer TMD transistors to work in
967 the velocity saturation regime using our best R_C of $123\text{ }\Omega\text{ }\mu\text{m}$ and a theoretical F_C of 1.15×10^5
968 V/cm. The V_{DD} required by IRDS is also plotted. **d**, The required V_{DS} to bias monolayer MoS₂
969 transistors in velocity saturation regime for different contact technologies.

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Extended Data Table 1 | Key performance metrics of representative devices. The field effect mobility, $\mu_{\text{FE},2\text{t}}$, is extracted by 2-terminal configurations in which the effect of contact resistance is included (See Methods for details).

Channel	Synthesis method	Contact	Gate oxide	L (nm)	$\mu_{\text{FE},2\text{t}}$ ($\text{cm}^2/\text{V/s}$)	I_{ON} ($\mu\text{A}/\mu\text{m}$) / V_{DS} (V)	$I_{\text{ON}}/I_{\text{OFF}}$
1L MoS ₂	MOCVD	Bi	100 nm SiN _x	120	21	560/1.5	10^7
				150	21	378/1.5	10^8
				500	17	150/1.5	10^7
		Ni	300 nm SiO ₂	1000	30	28/1	10^8
				1000	3	2/1	10^6
				1000	0.03	0.02	10^4
	CVD, high quality	Bi	100 nm SiN _x	35	22	1135/1.5	10^6
				50	25	1005/1.5	10^7
				100	16	434/1.5	10^7
				200	15	339/1.5	10^7
	CVD, low quality		300 nm SiO ₂	500	0.2	0.2/1	10^3
1L WS ₂	exfoliated, high quality	Bi	100 nm SiN _x	120	19	350/1.5	10^7
	CVD, high quality			150	21	100/1	10^7
1L WSe ₂	exfoliated, high quality	Bi	100 nm SiN _x	120	12	321/1.5	10^8
	CVD, high quality			1000	17	14/1	10^8

	CVD, medium quality			1000	4	3.9/1	10^6
	CVD, low quality (aged)		300 nm SiO ₂	300	0.02	0.06/1	10^4

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