Benchmarking Silicon FinFET with the Carbon-Nanotube, and, Two-dimensional-FETs for Advanced Node CMOS Logic Application

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Abstract—In this paper, the performances of Silicon FinFET is compared to carbon-nanotube (CNT-FET) and two-dimensional field-effect transistors (2D-FET) for the upcoming node CMOS logic application. Based on the experimental results, a 17-stage ring oscillator circuit is implemented using the compact models to analyze the stage delay and energy-delay performances. A tightly positioned 20nm and 10nm channel length-based CNT-FET enhances I_{ON} but also increases the leakage currents significantly. Due to poor electrostatic control and increased gate leakage, the CNT-FET and 2D-FET are providing lowered I_{ON} and a limited AC performance. Thus, targeting an off-state current, the FinFET delivers more than three times higher drive current, as well as 5-times better energy-delay performances in comparison to the CNT-FET and 2D-FET. On the other hand, scaled organic-FETs are yet far away to compare with FinFET technology. Hence, the silicon-based (3D) field-effect transistors are leading in all the devices (2D, 1D, and 0D) for scaling next-generation CMOS technology.

Index Terms—CMOS Logic, Si FinFET, Carbon-Nanotube-FET, 2D-FET, Compact modeling, Circuit simulation.

I. INTRODUCTION

ADVANCEMENT in the semiconductor industry has transformed the modern society. The availability of a high-performance mobile computing device and the fastest communication system becomes an everyday life activity. The engine behind this technological drive is a tiny transistor in an integrated circuit. Miniaturization of a silicon transistor is continuous over the last 50 years since the Gordon Moore's prediction [1]. While going from planar MOSFET to recent FinFET, the power-performance and area gain were confirmed in every new generation [2-4]. However, current challenges in FinFETs are expected to change the device design for the 5nm node and beyond technologies. Engineers are looking for the most suitable device option to gain the scaling benefit in the upcoming generations. The gate-all-around and recessed channel silicon field-effect-transistors are mostly studied for sub-5nm node dimensions [5-7]. However, many researchers have fabricated transistors using other non-silicon materials,

Fig. 1. Schematics of three different model transistor: (a) BSIM-CMG for silicon FinFET, (b) VS-CNT-FET model for carbon-nanotube, and (c) S2DSb model (2D semiconductor quasi-ballistic model) for 2D-FET.

TABLE I
PROPERTIES OF SILICON FINFET

Parameter	14nm FinFET [3]	10nm FinFET [4]	Δ
Contacted Gate Pitch	70nm	54nm	0.7x ↓
Metal Pitch (min)	52nm	36nm	0.7x ↓
Fin Height	42nm	46nm	4nm ↑
Fin Width	8nm	7nm	1nm ↓
Gate Length	20nm	~18nm	2nm ↓
I_{ON} (@ $V_{ds}, V_{gs} = 0.7V$)	1.04 mA/ μm	1.78 mA/ μm	~70% ↑

such as carbon-nanotube (CNT-FET) [8-12] and two-dimensional materials (2D-FET) [13-16], and the device performances are explained such that these emerging channel materials are better alternatives than silicon. Therefore, in this work, the recently published 14nm and 10nm node [3-4] silicon transistor from Intel corporation are studied along with the sub-20nm channel length-based CNT-FETs [8-10], as well as the sub-100nm channel length based 2D-FETs [13-15]. Although the most recently developed 5nm node silicon FinFET from TSMC is a qualified technology, there was limited data to extract the device parameters [17].

The extracted transfer and output characteristics of these transistors are used to validate a compact model to perform a circuit simulation. The FinFET, CNT-FET, and 2D-FET are fitted to the BSIM-CMG [18], VS-CNT-FET [19], and S2DSb [20] models, respectively. The BSIM-CMG is an industry-standard compact model widely used for the current FinFET technologies and the upcoming node gate-all-around FETs [21].

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The S2DSb model (2D semiconductor quasi-ballistic transistor compact model) is based on the MIT virtual source (MVS) model [22, 23] for the sub-100nm channel-based two-dimensional-FETs. Although the surface potential-based compact model is under development with disordered transport phenomena [24], we have considered virtual-source-based models for the 2D-FET and the CNT-FET devices. The schematics of these model transistors are presented in Fig.1. To benchmark the best suitable device option, the stage-delay and energy-delay (AC) performances are analyzed using the ring oscillator (RO) circuit [25]. Along with the energy-delay performances, the trends of the saturation drive current (I_{ON_Sat}) and effective drive current (I_{eff}) [26] at different drive voltages (V_{dd}) are also discussed.

II. EXPERIMENTAL DATA AND SIMULATION METHODOLOGY

The key FinFET parameters are highlighted in Table I. Keysight model builder program (MBP) tool [27] was used to fit these parameters into the BSIM-CMG model for both the n-type and p-type FinFETs. BSIM-CMG build macro model is also considered to include the parasitic resistance and capacitance for each device [18]. The CNT-FET characteristics were fitted into the VS-CNT-FET model using Matlab. Then the model was converted back into the Verilog file to run the circuit simulation. Top gated parasitic resistances and capacitances are included in the CNT-FET model for all devices [28]. Similarly, the characteristics of 2D-FETs are fitted to the S2DSb model using the Cadence Visualization and Analysis

Fig. 2. The ring oscillator (RO) circuit and oscillation output: (a) Two stages of RO chain having fan out 4, and considered load R_L and C_L . (b) Oscillation output showing the time period and total stage delays for considered device.

tool [29]. Although the S2DSb model doesn't include gate tunneling and major parasitic (fringe) components, the intrinsic AC performances can be validated further with the updated model.

Next, these validated models are used in the ring oscillator (RO) circuit implemented in the cadence Spectre [30]. A 17-stages RO circuit has a driving load of fan-out four and assumed interconnect load (BEOL) as R_L and C_L in each stage (shown in Fig. 2. (a)). A critical path in modern technology is assumed to be $6.3\mu\text{m}$ (90 times gate pitch length) [31], and the average interconnect loads are considered as (R_L) $43\Omega/\mu\text{m}$ and (C_L) $0.28\text{fF}/\mu\text{m}$, respectively [32]. Likewise, for the 10nm FinFET, a $50\Omega/\mu\text{m}$ resistance (R_L) and $0.35\text{fF}/\mu\text{m}$ capacitance (C_L) are considered [33]. Similar loads are also assumed for both the CNT-FET and 2D-FET based RO circuits. The stage delays (as shown in Fig.2 (b)) are calculated with a targeted off-state current by adjusting the threshold voltage parameters such as the gate metal work function in FinFET, flat band voltage in CNT-FET (V_{fb}), and threshold voltages (V_{th}) in 2D-FET model.

III. RESULTS AND DISCUSSION

Fig.3 shows the extracted 14nm node silicon FinFET experimental data, which are well fitted into the BSIM-CMG model for both the transfer and output characteristics. A similar fitting was also performed using the 10nm node silicon FinFET. Compared to the 14nm node p-type FinFET, the 10nm node p-

Fig. 3. The 14nm Silicon FinFET characteristics [3] are fitted to the BSIM-CMG model: (a) Fitted transfer characteristics, and (b) Output characteristics for both the devices at different gate voltages.

Fig. 4. Scaling benefit from 14nm to 10nm node: (a) A 70% increased saturation drive current, and (b) ~65% increased effective drive current at $V_{dd} = 0.7\text{V}$, (c) The AC analysis shows the gate delay is reduced by 45% in all the drive voltages, as well as (d) The energy-delay performances are improved in 10nm node FinFETs in comparison to the 14nm node devices.

FinFET provides $\sim 70\%$ increased saturation drive current, as well as $\sim 65\%$ increased effective drive current (at $V_{dd} = |0.7V|$), as shown in Fig. 4(a) and (b). A 272nm logic cell height (7.5 track 2 fin) is realized for the 10nm node technology compared to the 399nm (7.6 track 2 fin) in 14nm node CMOS. The stage delay for different V_{dd} and the energy versus delay performances are plotted in Fig. 4(c) and (d). A 45% reduction in stage delays is observed in 10nm node FinFET in comparison to the 14nm node technology (at $I_{off_target} = 10nA/FET$). Moreover, the 10nm FinFET consumes lower energy with a minimized delay than the 14nm node FinFETs. Thus, the performance benefit is ensured along with the area scaling.

Recently many carbon nanotube field-effect transistors are fabricated with ultra-small dimensions. The top three sub-20nm gate length-based CNT-FET are considered and benchmarked with the Si FinFETs. Table-III shows the critical dimensions of these CNT-FET transistors. A 20nm channel length based single-wall p-type CNT-FET is presented in [8]. The VS-CNT-FET model is fitted for both the transfer and output characteristics shown in Fig. 5(a) and (b). Assuming

TABLE II
CARBON NANOTUBE TRANSISTOR PARAMETERS

	CNT-FET [8]	CNT-FET [9]	CNT-FET [10]
Gate Length	20 nm	10 nm	11.4 nm
Contact Length	20 nm	25 nm	10.7 nm
CNT Diameter	1.1 nm	1.3 nm	1.0 nm
HfO ₂ thickness	10 nm	3.5 nm	5 nm
Spacer Length	3nm	5nm	3.6nm
CNT pitch	10 nm	8 nm	5 nm
Width	1000 nm	1000 nm	1000 nm

Fig. 5. A 20nm channel length based CNT-FET [8] : (a) The transfer plot of p-type CNT-FET is fitted to a VS-CNT-FET model, and (b) The fitted output characteristics for different gate voltages; (c) The stage delay in CNT-FET (10CNTs/FET) is 7-times than the 14nm Si FinFET ($I_{off} = 10nA/device$), (d) Significantly increased energy for CNT FET at lower delay operation.

a uniformity in CNT performances, the number of CNTs can be increased to increase the drive current. But then again, the increased off-state current doesn't allow to grow of the boundless CNTs to achieve a higher drive current. Thus, we have considered 10 CNTs/FET having a pitch of 10nm (width (W) = 100 nm), allowing maximum I_{off} as 10nA/FET. Symmetric n-type CNT-FET is also assumed to be fabricated, thus, implementing an inverter in the RO circuit. In doing so, the stage delay is observed more than seven-times (slower) than the 14nm node silicon FinFETs as shown in Fig. 5(c). Significant higher energy starts consuming while operating at lower stage delays. Thus, the silicon FinFET delivers better energy-delay performance than the 20nm channel length-based CNT-FET, as shown in Fig.5 (d).

Reducing the gate length to 10nm in CNT-FET may deliver better performances [9]. Both the fabricated n-type and p-type single-walled CNT-FETs are fitted into the VS-CNT-FET model, as shown in Fig. 6(a). Assuming a uniform pitch of 8nm

Fig. 6. The CNT-FET ($L_g = 10nm$ [9]) is compared with the FinFETs: (a) The transfer characteristics of fabricated CNT-FET is fitted to the VS-CNT-FET model for both the n-type and p-type FETs at $V_{dd} = |0.4V|$, and (b) Considering 125CNTs/ μm , the $I_d V_g$ of this device is plotted with the 14nm and 10nm node Si FinFETs at $V_{dd} = |0.7V|$.

Fig. 7. I_{ON} and AC benchmarking: (a) Single CNT gives 3.9nA as I_{off} , so, to target $I_{off} = 150nA/\mu m$ allows 40CNTs/ μm only. Thus the 10nm node FinFET provides three-times better saturation drive current than p-type CNT-FET (at $V_{dd} = -0.7$) (b) Also the effective drive current in FinFETs are higher than the CNT-FET, (c) The 10nm FinFET is operating at > 3 -times faster than the 10nm channel length based CNT-FET (while I_{off_target} of 10nA per device), (d) The energy performance in 10nm node FinFET is better than the CNT-FET as well.

(125 CNTs/ μm), the transfer characteristics of this CNT-FET is compared with the 14nm and 10nm node Si FinFETs, as shown in Fig. 5(b). Although the I_{ON} in CNT-FET is shown to be higher (at $V_{\text{ds}} = |0.4| \text{ V}$), the I_{off} (at $V_{\text{gs}} = 0 \text{ V}$) becomes very high as well ($\sim 1.2 \mu\text{A}/\mu\text{m}$), as the minimum I_{off} per n- and p-CNT are 9nA and 3.9nA respectively. On the other hand, FinFET provides increased I_{ON} (at $|0.7| \text{ V}$) with a minimized I_{off} ($\sim 2.5 \text{ nA}/\mu\text{m}$). Therefore, to compare the device currents with a targeted off-state current, CNT pitch is relaxed to 40 CNT/ μm allowing maximum of I_{off} as $150 \text{ nA}/\mu\text{m}$. The saturation and effective drive currents are plotted in Fig. 7(a) and (b). It is observed that 10nm FinFET provides three times better saturation and effective drive current than the CNT-FET. Therefore, targeting an off-state current (10 nA/FET), the stage delays in CNT-FET are observed to be lagging behind the FinFETs, as shown in Fig. 7(c). By reducing the stage delay in CNT-FET based RO circuit, higher energy is consumed in comparison to both the FinFETs (10nm and 14nm node), as shown in Fig. 7(d).

Considering a 40nm foot-print based CNT-FET [10], the benefit of scaling the CNT is expected as the total device length has been reduced. Hence to compare the DC and AC performances with the FinFET, the transfer and output

Fig. 8. A 40nm foot-print based CNTFET compared with FinFET: (a) The pCNT-FET is fitted to the VS-CNT-FET model for both Lin and Sat currents, (b) Fitted output characteristics for $V_{\text{gs}} = -3 \text{ V}$ to -1 V , (c) FinFET provides more than 3-times higher I_{ON} as well as less than 10^5 times lower I_{off} , (d) The energy consumed in CNT (100CNT/FET) is significantly higher than the recent FinFETs.

Fig. 9. Oscillation output at targeted off-state current (10nA/FETs): The 10nm node silicon FinFET based circuit is operating (at ~ 6 times) faster than the 10nm channel length-based CNT-FETs at $V_{\text{dd}} = 0.7 \text{ V}$.

characteristics are fitted into the VS-CNT-FET model, as shown in Fig. 8.(a) and (b). Even though the I_{ON} is increased slightly ($0.8 \text{ mA}/\mu\text{m}$ at $V_{\text{gs}} = -3 \text{ V}$, $V_{\text{ds}} = -0.5 \text{ V}$), the sub-threshold region is observed to be very poor ($\text{SS} = 680 \text{ mV/dec}$). While comparing the transfer plot with the 10nm node p-FinFET at ($V_{\text{ds}} = -0.5 \text{ V}$), the CNT-FET delivers less than three times lowered I_{ON} , and more than 10^5 times higher I_{off} (Fig. 8(c)). Therefore, a substantial higher energy consumption is observed while operating at lower frequency (even without an $I_{\text{off_target}}$ in CNT-FET), as shown in Fig. 8. (d).

Therefore, the performances of these CNT-FETs are lagging in both the drive current and sub-threshold operation. By fixing an equal width (68nm) and leakage power (7nW) per device, the transient output of the recent FinFET is found to be more than seven times faster than the best CNT-FET ($L_{\text{g}} = 10 \text{ nm}$ [9]), as shown in Fig. 9. The increased sub-threshold and gate induced drain leakage (GIDL) become a major concern for the carbon nanotube field-effect-transistor's performance irrespective of their fabrication challenges. Thus, the CNT-FET researchers need to overcome many fundamental issues such as placing uniform CNTs on a wafer and minimizing the leakage currents at a smaller dimension to outperform the silicon field-effect transistors.

Two-dimensional materials are fantastic candidates, however, unlike the Si and SiO_2 interface, the lack of dangling bond with gate dielectric constitute a significant concern for excessive gate leakage in 2D-FET. Irrespective of the process difficulties, the DC and AC performances of 2D-FET are compared with the silicon field-effect transistors. The performances are analyzed using validated compact models

Fig. 10. The quasi-ballistic 2D-FET model fitted with the experiments: (a) The output characteristics of 10nm gate length based MoS_2 -FET [13], (b) The transfer characteristics of 29nm gate length MoS_2 -FET [14], (c) The fitted $I_{\text{d}}V_{\text{g}}$ of MoS_2 -FET [15] having gate dielectric of 10nm HfO_2 , and (d) The fitted $I_{\text{d}}V_{\text{d}}$ of MoS_2 -FET having gate dielectric of 5nm HfO_2 .

(S2DSb) for the three most advanced MoS_2 transistors [13-15]. A 10nm channel length based MoS_2 transistor [13] is fitted to the S2DSb model, as shown in Fig. 10(a). Although the n-type MoS_2 transistor has a negative threshold voltage ($V_{\text{th}} = -3.8 \text{ V}$),

the V_{th} has been shifted to a positive value for targeting 100 nA/ μm as I_{off} . Similarly, a 29nm channel based MoS₂ transistor [14] is fitted to the model ignoring the gate leakage current, as shown in Fig. 10(b), in addition to, a 100nm channel based MoS₂ device [15] providing $\sim 400 \mu\text{A}/\mu\text{m}$ (at $V_{ds} = 1\text{V}$ and $V_{gs} = 4\text{V}$) having 10nm HfO₂ as a gate dielectric. The transfer and output characteristics with two different gate dielectrics as

Fig. 11. DC and AC analysis in 2D-FET: (a) Saturation drive currents and (b) Effective drive current with a targeted I_{off} 100nA/ μm (c) Stage delays in RO circuit for these device (d) The Energy consumption with the stage delays having 10nA I_{off} and 100nm device width.

10nm and 5nm are fitted to the same model, as shown in Fig. 10(c) and (d).

The saturated and effective drive currents at different drive voltages (while targeting similar I_{off}) are plotted in Fig 11. (a) and (b). The maximum saturation current (at $V_{dd} = 0.7\text{V}$) is found to be $45 \mu\text{A}/\mu\text{m}$ in comparison to the $\sim 1.7 \text{mA}/\mu\text{m}$ in the 10nm node FinFETs. Likewise, the effective drive currents are observed to be significantly lower than the FinFET in all drive voltages. The S2DSb model has no added parasitic capacitance and resistances, but the interconnect load (R_L and C_L) is considered equivalent to the 10nm node FinFETs. Although, many p-type 2D-FETs are fabricated with the WSe₂ as the channel material, the p-type 2D-FET are considered as

symmetric to the n-type 2D-FET for the ring oscillator simulation. Hence, the delays in RO circuit for these 2D-FET devices are plotted in Fig. 11(c). In addition, the energy versus stage-delays are plotted in Fig. 11(d). Although, the 100nm L_g based MoS₂-FET has better energy performances at lower drive voltages, the 29nm channel based MoS₂-FET provides lower delay with reduced device area.

Next, the AC performances of the best CNT-FET ($L_g = 10\text{nm}$ [9]) and the best 2D-FET ($L_g = 29\text{nm}$ [14]) are compared with the silicon 10nm node FinFET [4]. The stage delays at different V_{dd} are plotted in 12(a). It is observed that the FinFETs are providing much lower delays with a minimum transistor footprint area. In addition, the lowest energy is consumed to operate at the highest frequency, as shown in Fig. 12(b). Indeed, the FinFET will lose some electrostatics control at sub-5nm node dimensions, but other non-silicon materials such as 2D and 1D material-based field-effect transistors are lagging in both the overdrive as well as the sub-threshold performances.

On the other hand, many 0D material based organic-field-effect transistors (oFET) are presented for digital scaling [34-39]. However, digital CMOS technology is mainly driven by the area scaling along with the performance gain. Although the oFETs are used extensively for the display and other flexible technologies [39], the device dimensions are ~ 100 times larger than the recent FinFETs [40]. Compared to a current 272nm complete inverter cell (height) in the 10nm node technology, the channel lengths in oFETs are nearly 500nm or more. Along with the larger dimensions, the oFET are providing a much lower drain current ($\sim 10\mu\text{A}$) even at much higher drive voltages ($V_{dd} = \sim 3$ to 5V). Therefore these devices would be operating at a much slower frequency and consuming huge power to compare with the modern CMOS.

IV. CONCLUSION

The silicon FinFET is compared to the carbon nanotube and two-dimensional transistors for the upcoming technologies. Although the CNT-FET has the ability for high-density integration, they are suffering from the fundamental short channel leakages. Both the DC and AC analysis show that performances are yet lagging behind the FinFETs. Similarly, the two-dimensional materials are facing excessive gate leakage along with poor sub-threshold control. Thus, targeting an off-state current, the FinFET delivers more than three-fold better drive current and five-fold better energy-delay performance than the CNT-FET and 2D-FET. On the other hand, scaling organic-FETs are far away to compare with FinFET technology. Thus, the silicon FinFET is still performing better than the 2D, 1D, and 0D devices for scaling the next-generation CMOS technology.

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Fig. 12. Benchmarking three different transistors with an $I_{off_targeting}$: (a) The stage delays in FinFET is less than the CNT-FET, and the stage delay in CNT-FET is less than the 2D-FET (b) Also, the energy vs. delay performances are better in FinFET than CNT-FET than the 2DFET transistors.

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