Chapter 6

On-Chip Antenna: Challenges and Design Considerations

Atif Shamim¹ and Haoran Zhang¹

This book chapter focuses on on-chip antennas (OCA). The challenges associated with OCA design, implementation, and characterization are discussed in detail. In addition, this chapter highlights the research work that has been conducted in this field to date. This chapter concludes by proposing future research directions in the field of OCA.

6.1 Introduction

Presently, the most common approach for the realization of a wireless system is through the assembly of discrete components, such as digital integrated circuits (IC), mixed-signal ICs, radio-frequency integrated circuits (RFIC), and passive components, on printed circuit boards (PCB), as displayed in Figure. 6.1. This arrangement is known as system-on-board (SoB) [1], and there are several problems associated with this conventional SoB approach. Since separate ICs are mounted on the PCB, each IC requires a bulky and costly IC package for physical protection and input-output (I/O) connections from the chip set to the system board. This involves the use of on-chip bond pads and bond wires, which limits the chip's performance and reliability. The overall system in this approach occupies a large size, and the realization cost is high. In addition, since various types of ICs are used for one system, different design and fabrication processes are required for the realization of RFICs, digital ICs, and mixed-signal ICs, which unfortunately creates issues of compatibility and reliability. Other than the ICs, antennas are designed on a separate PCB, which must be integrated with the PCB containing ICs and other discrete components. In some cases, the antenna can be on the same PCB as the ICs. This PCB antenna is connected to the RFIC through bond wires and bond pads, which unfortunately introduce additional radio-frequency (RF) insertion loss and transmission uncertainty because the RF properties of these bond wires and bond pads are not well characterized, especially for higher frequencies. To resolve the aforementioned problems associated with SoB, the best solution is to combine all discrete components on a single chip, an arrangement known as system-on-chip (SoC) [2].

¹Electrical Engineering Program, King Abdullah University of Science and technology (KAUST), Saudi Arabia

Figure 6.1 System PCB integrated with RFIC, mixed-signal IC, digital IC, and separate PCB antenna

Over the past few decades, the aggressive miniaturization of complementary metal oxide semiconductor (CMOS) transistors, followed by Moore's law, has promoted the development of ICs into a higher-integration level, which makes it possible to integrate the complete system on a single chip, realizing an SoC. The highly integrated SoC provides the benefits of low cost, small physical size, light weight, and low power consumption, which facilitate the realization of portable and highly compact devices, such as internet of things (IoT) sensors and compact radar systems. Due to the rapid development of ICs, the digital module, analog module, and RF front-end can be integrated on a single chip. However, some issues remain in combining all different modules in one chip. One major issue is that each circuit module requires its own specialized process. If all the circuit modules are integrated in one chip, the process might not be suitable for all of them being in the best performance. Nonetheless, it is feasible to integrate all the circuit modules in a single chip; however, the bottleneck for a real wireless SoC is the realization of an on-chip antenna (OCA). The typical chip sizes are on the order of a few millimeter squares to around 100 mm^2 . However, the antenna size is proportional to the wavelength, which is quite large at low frequencies. As a result, the typical antenna size is much larger than the size of the available chip space for low-frequency applications. For example, a typical WiFi antenna length is approximately 60 mm, so it cannot be efficiently realized on a chip. Moreover, after the integration of all the circuit modules, there is limited space for the realization of OCA. Over the past two decades, driven by the high demands of high bandwidth and system compactness, tremendous efforts have been made in the development of millimeter-wave (mm-wave) and sub-terahertz applications. The use of mm-wave and sub-terahertz frequency bands has significantly decreased the antenna sizes (due to shorter wavelengths), providing the possibility of implementing the antenna on the chip. Figure 6.2 illustrates the concept of OCA integration with ICs. Since the OCA can be fed by the circuit through an on-chip transmission line, the influence of bond wires and bond pads can be eliminated. Furthermore, integrating OCA and circuits in the same chip removes the restriction of 50Ω impedance matching. Instead, more flexible methods of impedance matching can be applied, providing IC and antenna designers with greater design freedom. However, it is difficult to realize an OCA with high performance in a typical CMOS process. Many challenges related to the OCA still must be tackled. These issues are discussed in detail in the following section.

Figure 6.2 Concept of system-on-chip

6.2 On-Chip Antenna Challenges

As mentioned in the previous section, OCA presents an excellent solution for the applications that require higher integration levels and lower cost. However, it is feasible to realize the OCA in the commercial CMOS processes, and there remain many challenges related to the OCA. In this section, challenges of OCA are studied from the perspectives of design, layout, and characterization.

6.2.1 Incompatible CMOS Stack-Up

Bulk silicon is the most commonly used substrate in standard CMOS processes. It has low resistivity and is highly suitable for the circuits. Its abundance ensures a lower cost for CMOS processes. However, the bulk material properties of silicon and the CMOS stack-up are not suitable for efficient realization of OCAs.

A typical CMOS stack-up is depicted in Figure. 6.3. A 300–500 μm thick silicon substrate is located at the bottom. On top of the silicon substrate, thin layers of dielectrics (around 7–15 μm thick) are embedded with 6–9 metal layers, each of which has a thickness approximately 500 nm, except for the top metal layer, which has a thickness of 1–2 μm . The metal layers are typically used to realize the passive components, such as capacitors, inductors, and transmission lines. The interconnections are also implemented in these metal layers and use the inter-layer vias. Among all the metal layers, the top layer is the best choice for the implementation of OCA because its relatively higher metal thickness can minimize the skin depth effect, especially for the antennas in mm-wave and sub-terahertz frequency bands. The dielectric layers (typically SiO_2) between the metal layers provide good insulation. On top, the chip is typically covered with a thin layer of silicon nitride or polyimide for protection, which is known as the passivation layer.

Figure 6.3 Silicon-based CMOS stack-up

6.2.1.1 Low Radiation Efficiency

Low radiation efficiency is the most critical issue for the effective realization of an OCA. The primary reason for low radiation efficiency is the use of the low-resistivity silicon substrate in commercial CMOS processes.

As a semiconductor, the silicon substrate has a low resistivity of around 10–15 $\Omega\cdot\text{cm}$, which is an advantage for IC design, since low resistivity is helpful for avoiding latch-up issues. Latch-up occurs due to current conduction by parasitic NPN or PNP devices formed in the substrate. By using low-resistivity substrates, the gain of these devices is reduced, which reduces the likelihood of latch-up [3]. However, the use of a low-resistivity substrate is catastrophic for OCA design. When the antenna is closely placed on top of this silicon substrate with low resistivity, the electromagnetic (EM) waves find a low resistive path in the silicon substrate. Thus, the silicon substrate absorbs most of the RF power, which is dissipated in the silicon substrate in the form of heat [4] rather than being radiated in the air, as displayed in Figure 6.4. As a result, OCA offers very low radiation efficiency.

In addition to the property of high loss, the silicon substrate also has a high permittivity value of 11.9. This results in more EM fields in the substrate compared with the free space radiation. In fact, the ratio of the power that is trapped in the substrate compared with the power that radiates into the air can be calculated approximately using the following equation [5]:

$$\frac{P_{air}}{P_{sub}} = \frac{1}{\epsilon_r^{3/2}}$$

where P_{sub} is the power trapped/absorbed in the substrate, and P_{air} is the power that is radiated in the air. According to the equation, 97% of the total power is coupled to the typical bulk silicon substrate, while only 3% RF power is radiated in the air. The power coupled in the substrate is mostly dissipated as heat. Some power is radiated from the substrate in unintended directions; however, this is an issue that will be discussed in the following sub-section.

Figure 6.4 Overview of system-on-chip and on-chip antenna challenges

6.2.1.2 Surface Waves

Other than the low radiation efficiency, the OCA suffers from the generation of surface waves due to the high permittivity of the silicon substrate and its large thickness. These high-order surface waves distort the desired antenna radiation pattern. The typical thickness of the silicon used in the CMOS foundries is in the range of 300–700 μm , which is considered electrically thick for mm-wave frequency applications. In addition, the high permittivity of the silicon substrate reduces the guided wavelength in the substrate. As a result, high-order surface waves can be generated in this silicon substrate. The antenna substrate always supports one surface wave mode as least. This surface wave mode is known as the TM_0 mode, which does not have a cut-off frequency, so they are always being excited. The following equation reveals the surface wave cut-off frequency for higher modes:

$$f_{\text{cut-off}} = \frac{nc}{4h\sqrt{\epsilon_r - 1}}$$

where n is the surface wave mode number ($n = 0, 2, 4, \dots$ for TM_n modes; $n = 1, 3, 5, \dots$ for TE_n modes), c is the speed of light in free space, h is the thickness of the substrate, and ϵ_r is the substrate permittivity. According to the equation, the larger substrate thickness and higher permittivity lead to a lower cut-off frequency; as a result, more surface waves with higher modes can be excited. For example, a 77 GHz OCA can excite a higher-order surface wave— TE_1 mode, which has a cut-off frequency of 56.8 GHz—if the antenna has a silicon substrate with a permittivity of 11.9 and thickness of 400 μm .

As displayed in Figure 6.4, surface waves can radiate at substrate side surfaces and surface discontinuities, such as truncations and cavities in the substrate, which cause changes in the radiation pattern and polarization characteristics. An investigation of how the surface waves distort the radiation pattern of OCA has been conducted in [6]. As presented in Figure 6.5, a satisfactory donut-shaped radiation pattern is obtained when the silicon substrate thickness is 20 μm . As the

silicon substrate thickness increases, the radiation pattern begins to distort. Especially when thickness is increased to $500\text{ }\mu\text{m}$, high-order surface waves are generated in the substrate, which completely distort the original radiation pattern.

Figure 6.5 3-D radiation patterns of a planar on-chip bowtie antenna at 77 GHz for various silicon thicknesses. (a) 20 μm thick silicon, (b) 50 μm thick silicon, (c) 500 μm thick silicon [6]

6.2.2 Co-design of Circuits and On-Chip Antenna

In an on-chip implementation, the antenna and circuits are placed very close to each other due to the limited space available on the chip. Thus, their influence on each other's performance can no longer be ignored. The coupling between the OCA and the other on-chip components, particularly on-chip inductor, capacitors, and RF interconnects, can be detrimental for system performance. Therefore, a co-design strategy for the circuits and antenna must be adapted to eliminate surprises after the chip has been fabricated; however, reliable and efficient simulation mechanisms, for the co-design approach, are still far from optimal. In this section, the issue of crosstalk between the OCAs and circuits is discussed first. Afterward, the co-simulation approach and its challenges are presented.

6.2.2.1 Coupling Effects between OCAs and Circuits

As previously mentioned, the antenna is typically realized on a separate PCB; therefore, the crosstalks or coupling effects between circuits and antennas are not significant due to the large distance between them. However, the SoC is a highly integrated environment in which the OCAs and circuits are integrated in a single chip with extremely small spacing between them. In this case, the crosstalks or coupling effects cannot be ignored. Since the field of OCA is relatively young, few papers have investigated the coupling effects between the OCAs and on-chip circuits [7, 8].

Unwanted coupling effects can distort the OCA's input impedance matching and radiation performance, such as radiation efficiency and radiation patterns. The close-by metals from the circuit part can alter the OCA's current distribution; thus, the OCA's input impedance and radiation performance can be affected. The circuit part primarily comprises active components, passive components, and some other elements, such as bond pads and dummy metal fills. The feature sizes of active components, such as transistors and diodes, are very small; therefore, they do not strongly impact the OCA's performance; however, the passive components, such as inductors, capacitors, and transmission lines, have relatively large sizes

(proportional to the operation frequency), and their presence in the close vicinity of the OCA is detrimental. In addition, the side length of a bond pad is typically larger than 50 μm , which is considered large, particularly for a mm-wave OCA. On the other hand, dummy metal fills are used in all metal layers to fulfill the specific layout rules defined by the CMOS foundries. Though dummy metal fills have relatively small dimensions, they are placed in large numbers in close proximity and thus cause unwanted coupling effects. Figure 6.4 illustrates the coupling effects between an OCA and some close-by metals.

Negative effects can occur on the circuits' performance, as well, such as the frequency response of an amplifier's gain being distorted by unwanted coupling. Other than the coupling of electromagnetic energy through air, coupling can also occur through the substrate. The noise currents, generated by OCA, are injected into silicon substrate [9]. When the noise currents in the substrate reach the active region of the circuits, the circuit performance will be affected [10], as presented in Figure 6.6. Conversely, the noise currents generated by the circuits' active region can flow toward the critical area below the OCA and influence the antenna's performance. One good solution to avoid the noise currents is through the use of guard rings that can isolate the OCA and circuits' active regions [11-13].

Figure 6.6 Substrate noise coupling [10]

6.2.2.2 Co-Simulations of OCAs and Circuits

Typically, antenna design is performed in an EM simulator, such as Ansys HFSS [14] or CST STUDIO SUITE [15], which rely on solving Maxwell equations with appropriate boundary conditions. Circuit designers, on the other hand, do not require EM simulations and therefore use simulators such as Cadence [16] or Keysight ADS [17] for circuit simulations, which generally perform voltage- or current-based nodal analysis. Integrated circuit design in particular relies heavily on Cadence simulations that use the technology files for device models from the relevant foundry. Unfortunately, there are only a few mainstream simulation tools that can run both EM and circuit simulations simultaneously, but even in these simulators, capturing the coupling between OCA and the circuits is not completely feasible. For this reason, the OCA design is normally first optimized in an EM simulator; then, its layout is exported to an IC design tool, such as Cadence. However, the antenna structure cannot be simulated in the IC design tool, so the complete system (circuits and antenna) cannot be simulated together. This is

because the EM simulators are based on solving Maxwell equations in the meshed fields to obtain the exact EM performance of the 3D structures, which also accounts for all the coupling effects [18]. However, the coupling effects and antenna characteristics, such as radiation performance, cannot be modeled and simulated in circuit simulators because circuit simulators typically rely on nodal voltage- and current-based calculations of lumped or distributed equivalent models. Similarly, circuit performances cannot be simulated in EM simulators.

The antenna must be simulated in the exact same manner as it is connected to the circuit, and vice versa. Although it is challenging to run a true co-simulation, several methods exist for partially investigating the effects of OCA and the circuits on each other. The most common method for including the OCA's effects on circuit performance is to extract the OCA's S-parameters from the EM simulator after optimization and import them into an IC design tool. Then, the circuit can be co-simulated with the OCA's input impedance characteristics. As presented in Figure 6.7(a), the OCA's S-parameters are imported into Cadence to run a co-simulation with an on-chip voltage-controlled oscillator (VCO). Normally, it requires several iterations between the EM simulator and IC design tool to achieve an optimized design with good impedance matching between the circuit and the OCA. This, however, considerably increases the complexity and simulation time. In addition, the extracted S-parameters of the OCA are in the frequency domain and cannot be directly used in the time-domain analysis [19]. In addition, the OCA's S-parameters are influenced by the port impedance in the EM simulator, so it is important to ensure that the interface impedance is consistent with the port impedance in the EM simulator. To include the influence of circuit and other on-chip metal structures on the OCA's performance, the conventional method is to model the close-by metal structures, such as passive circuit components, bond pads, and dummy metal fills, in the EM simulator to ensure that the simulated OCA's performance is reliable and accurate, as presented in Figure 6.7(b). However, this approach also encounters several challenges. First, layout is the last stage of the IC design, and since the antenna and circuit designs are done in parallel, the antenna designer must re-optimize the antenna after the IC layout is complete. Second, although the layout of the circuit part, including the passive components, bond pads, and dummy metal fills, can be imported in the EM simulator from the IC design tool, the circuit models are still not representative of the real case, as the circuit is not working in the EM simulator. For example, the coupling effects between an OCA and a close-by inductor without any currents differ from the case of the OCA being close to an inductor with currents. In addition, including the exact layout of the metal structures in EM simulation can dramatically increase the simulation time. Moreover, the EM simulators are unable to account for all the attributes in the semiconductor processes, which can be studied well only in the IC design tool [20].

This issue can be resolved only when the full-wave EM simulations and circuit simulations can be run together, in either a single simulator or two simulators running in conjunction.

Figure 6.7 (a) Co-simulation in Cadence, (b) co-simulation in HFSS

6.2.3 On-Chip Antenna Layout Issue

In the IC design cycle, after the schematic design, there is another critical step that can significantly affect the OCA's performance. This step is the chip layout drawing, which is restricted by the design rule check (DRC). During the layout drawing stage, DRC is an important process for ensuring that the chip layout fulfills the rules defined by the semiconductor foundries. Each semiconductor foundry has its own set of rules to ensure sufficient fabrication margins such that the chip fabrication has good repeatability and minimum variability in the fabrication process.

Among hundreds of rules in the DRC, three types of design rules are critical for OCA design. The first is the requirement of a certain metal density in each metal layer because the metal density impacts the etching rate in the fabrication stage. Global metal density rules indicate the metal density required for the entire chip, while local density rules define the metal density requirements for a certain area, normally an area of $100\ \mu\text{m} \times 100\ \mu\text{m}$. The typical metal density range is 30% to 70%. To meet the metal density requirement, a large number of dummy metal sheets should be placed in the empty area, while many slots should be etched on a large metal sheet surface. Figure 6.8 reveals that the blue dummy metal fills are placed in an empty area in all layers, while some slots are etched in the black large antenna patch metal. Once the slots and dummy metal sheets are introduced in the OCA area, the antenna's performance can deteriorate. In particular, the close-by dummy metal blocks can cause undesired interference with the OCA. The second type of critical design rules is the metal layer design rule, which indicates the maximum/minimum metal wire width, minimum spacing, and minimum size of the enclosure. Normally, the lower limits of the wire width, spacing, and enclosure size do not affect the OCA performance, as they are of the nanometer scale, while mm-wave and sub-terahertz antennas only require micron-scale fabrication resolution. However, the upper limit of the metal wire's width is approximately $20\text{--}30\ \mu\text{m}$, which can restrict the antenna design's flexibility. The third type is the via design rule, which includes the requirements for the size of a single via and the size of a via array. In the case of OCA design involving multilayers, a solid RF connection between the layers is highly desired, so the single via size and via array size play an important role.

Figure 6.8 Microscope view of an RFIC with dummy metal fills

Some other design rules could potentially affect the OCA. Thus, when designing the OCA, all these design rules should be considered and properly included in the simulations to avoid discrepancies between the simulations and the final measurements.

6.2.4 On-Chip Antenna Characterization

Typically, the IC fabrication is outsourced to commercial CMOS foundries, such as Taiwan Semiconductor Manufacturing Company (TSMC) or GlobalFoundries, among others. After the chip is ready, the most important and challenging step is the accurate and reliable characterization of the OCA.

The conventional antenna characterization is performed in an anechoic chamber by connecting the antenna to a network analyzer through an SMA connector, as presented in Figure. 6.9(a). This connector-based characterization method is convenient and accurate for measuring relatively large-sized antennas; however, this is not feasible for OCA characterization. The dimensions of the connector and its signal pin are on the scale of a few centimeters and millimeters, respectively, while the sizes of OCAs are typically on the orders of hundreds of micrometers, depending on their operation frequencies. Moreover, the RF pads for the measurement of OCAs are even smaller, typically in the range of $50 \times 50 \mu\text{m}^2$ to $100 \times 100 \mu\text{m}^2$. In such a case, the OCA is too small to be connected through the connector. Therefore, instead of the SMA connector, an RF probe is commonly used for getting access to the OCA, as displayed in Figure. 6.9(b). The RF probe is specially manufactured for proper landing on the RF pads of RFICs and OCAs. The tiny tips of the RF probe can be landed on the RF pads accurately with the help of a microscope. The OCAs cannot be tested in standard anechoic chambers; thus, specialized chambers are required, which are very expensive. One such chamber is illustrated in Figure. 6.10. It is a commercially available mm-wave anechoic chamber. Covered with an EM absorber, the chamber contains a theta/phi-direction rotatable disk attached with the reference antenna, a fixed arm for probe landing and placing the OCA at the chamber center, and a microscope as a part of the vision system to ensure accurate and reliable probe landing on chip pads. In addition, there are some customized chambers dedicated for OCA measurements [21-24]. Although such an anechoic chamber can be used for the characterization

of an OCA's reflection coefficients and radiation patterns, there are still several challenges related to the measurement accuracy of probe-based characterization.

Figure 6.9 Antenna characterization method. (a) connector based, (b) probe based

Figure 6.10 Probe-based OCA characterization set-up in μ -Lab anechoo chamber.

Among all the challenges related to probe-based OCA characterization, the interference between the RF probe and OCA is considered the most critical. As depicted in Figure. 6.9(b), the RF probe consists of a large conductor body, and the probe tips are attached to a metallic arm, which is partially covered by the EM absorber. With the presence of the close-by large conductor body of the RF probe, EM waves get reflected from the probe body. The directly radiated EM waves from the antenna and the reflected waves from the probe conductor body interfere with each other. The final radiation pattern is the superposition of the radiated and reflected waves. The maximum and minimum radiations can be obtained at certain angles, depending on the phase difference between the radiated and reflected waves [25], as presented in Figure. 6.11. As a result, the OCA's radiation pattern is distorted due to the presence of the probe's conductor body. Other than the influence on the antenna's radiation patterns, the unwanted interference between

the OCA and probe's conductor body and uncovered probe tips can cause unexpected changes in the reflection coefficient, though the probe's inner impedance has been de-embedded through the impedance calibration [26]. Another challenge related to probe-based characterization is the self-radiation of the probe, itself. As previously mentioned, the probe tips are not covered by the EM absorber. Since the RF probe itself also radiates, the final radiation pattern is a superposition of the OCA's radiation pattern and the probe's radiation pattern [27]. To investigate the probe self-radiation, the probe's radiation pattern is characterized when the probe is connected to a calibration $50\ \Omega$ load, which represents a well-matched antenna. In such a case, only negligible radiation occurs from the $50\ \Omega$ load, so the measured radiation pattern can be approximately considered as the probe's self-radiation. The measured radiation pattern of a 60 GHz probe is presented in [27], which reveals that the maximum gain of the probe self-radiation is almost -21 dBi. This maximum defines the gain measurement sensitivity of the probe-based measurement system. This probe self-radiation is negligible for high-gain antenna measurement; however, it is considerable for the measurement of low-gain antennas, such as OCAs. Due to the low gain of the OCA, the probe self-radiation is comparable with the antenna's gain, thus causing the inaccuracy in the OCA's radiation pattern characterization. There is another drawback of probe-based OCA characterization: the radiation blockage in the probe area. Due to the presence of the probe, the OCA's radiation, in certain directions, is blocked by the probe body and its supporting arm. Thus, a complete radiation pattern cannot be obtained by the probe-based characterization method.

Figure 6.11 Interference between OCA's radiation and its reflection from probe

6.3 On-Chip Antenna Overview

Despite the challenges mentioned in the previous section, much work has been conducted in the area of OCAs. Throughout the past two decades, tremendous efforts have been made to resolve the aforementioned challenges and issues related to OCAs. This section highlights the important work conducted in this area. It is organized with respect to the most prominent challenges and their solutions in this field. In this section, we begin by introducing several existing approaches for the gain and radiation efficiency enhancement of OCAs. These enhancement approaches primarily consist of the modification of lossy silicon substrate and the use of reflection surface, superstrate, focusing lens, and MEMS structures, which are explained in detail in this section. On the other hand, regarding the antenna and circuit co-design issue, some important co-design strategies are discussed. These

can be applied to obtain more accurate and reliable results. In addition to the co-design strategies, two co-design simulators, which can run both the circuit and EM simulation at the same time, are introduced. Toward the end of this section, the latest improvement methods for probe-based OCA characterization are presented, which can decrease the undesired probe interference and self-radiation.

6.3.1 Gain and Radiation Efficiency Enhancement

As mentioned in Section II, the low radiation efficiency of OCAs is one of the major challenges related to OCA design and is primarily caused by the incompatible silicon substrate. To minimize the silicon substrate's negative influence on OCA performance, many researchers have been working on enhancement methods for OCA gain and radiation efficiency.

6.3.1.1 Modification of Incompatible Silicon Substrate

The lossy silicon substrate is the main cause of OCAs' low radiation efficiency. Essentially, there are three key negative-impact factors on OCAs' radiation efficiency due to the commercially used silicon substrate: low resistivity, high permittivity, and relative large thickness. A relatively straightforward approach is to alter the aforementioned properties of silicon substrate to decrease the losses in the substrate. Bulk micromachining and proton implantation are the two well-known methods for the modification of silicon substrate properties.

Bulk micromachining is a fabrication process used to form trenches or cavity structures in silicon or other substrates via selective etching [28]. It can be used to thin the silicon substrate under the OCA area. The overall relative permittivity of the mixture of air cavity and silicon substrate under the OCA area consequently decreases from 11.9 to a much lower value. However, more importantly, the overall loss due to the silicon substrate is also reduced. Bulk micromachining has been widely used for radiation efficiency enhancement [11, 29, 30]. For example, in [29], an air cavity was formed at the backside area of the on-chip patch antenna through selective etching, as presented in Figure. 6.12. Comparison simulations between on-chip patch antennas with and without air cavity were performed, which presented around a 28% radiation efficiency enhancement with the help of the air cavity.

Figure 6.12 Geometry of micromachined patch antenna [29].

In addition to bulk micromachining, proton implantation is another nano-fabrication method for improving on-chip antennas' radiation performance. Proton implantation is the process of implanting ions in the silicon substrate. Through proton implantation, the resistivity of the silicon substrate can be increased, resulting in improved radiation performance. For example, in [31], the substrate

resistivity increases from $10\ \Omega\text{-cm}$ to $10^6\ \Omega\text{-cm}$ by utilizing proton implantation. Eventually, the OCA demonstrates a 5 dB gain enhancement at 10 GHz.

From this point of view, bulk micromachining and proton implantation are capable of improving antenna radiation efficiency. However, both methods require additional nano-fabrication processes, which lead to an increase in fabrication complexity and higher fabrication cost. Moreover, entirely changing the silicon substrate's resistivity is not good for the circuits' performance. This approach can be suitable if the change is made in a selective manner so that it changes the resistivity only in the area of the OCA.

6.3.1.2 On-Chip Reflecting Surface

Instead of altering the properties of silicon substrate, a proper on-chip reflecting surface can be utilized to isolate the OCA from lossy silicon substrate. One easy approach is to use a PEC surface in between the OCA and silicon substrate; however, the radiation from the image currents in the PEC surface negatively affects the radiation from the OCA due to the electrically small spacing between the OCA and the PEC surface, as mentioned in Section II. Alternately, a perfect magnetic conductor (PMC) surface can be placed in the metal layers underneath the OCA to isolate it from the silicon substrate. This is beneficial, as in-phase reflection occurs on the PMC surface in contrast with a PEC surface and can boost the OCA's direct radiation. However, since PMC surfaces do not exist in nature, researchers have found an approximate equivalent in the form of artificial magnetic conductor (AMC) surfaces, which mimic PMC surfaces for a particular frequency range.

An AMC surface is realized through specially designed periodic structures over a PEC surface that acts a ground plane [32], as presented in Figure 6.13. The in-phase reflection performance of an AMC surface is primarily controlled by three important factors: the thickness of the substrate between the periodic structure and the ground plane, the size of the AMC surface, and the dimensions and shape of the AMC unit cell. Among the three factors, the substrate thickness is fixed by the CMOS stack-up. In theory, an infinite AMC surface behaves the same as a PMC surface for a certain frequency range; however, the AMC surface size is always restricted by the finite chip size. Therefore, the designed AMC surface size should be a reasonable compromise between AMC performance and limited chip size. Thus, for an on-chip AMC surface design, the dimensions and shape of the AMC unit cell are typically the only parameters that can be controlled by the designer to optimize the AMC performance. When the period of the periodic structure and the dimensions of its unit cell are sufficiently small compared with the free space wavelength in the operating frequency range, the structure can be assumed to be a homogeneous surface, which can be described by the parameter of surface impedance [33, 34]. Theoretically, the surface impedance of this AMC structure can be tuned by making it resonant at the desired operating frequency through the dimensions and period of the AMC unit cell. In this way, a very high surface impedance can be achieved over the operating frequency range. In terms of an equivalent circuit, when an RF signal travels toward an open load, the reflection coefficient is positive, representing a zero-degree reflection phase shift. Similarly, in-phase reflection occurs from the AMC surface due to the high impedance it presents to the incident EM wave. Other than the period and dimensions of the AMC unit cell, its shape too can affect the overall performance. In [35], a

comparison between the different shapes of an AMC unit cell has been made by studying their effect on bandwidth and return loss. Figure 6.14 displays five common structures for an AMC unit cell. It has been concluded that the square patch-based AMC surface has the widest bandwidth and lowest return loss among the five structures. Due to the capability of in-phase reflection, an AMC surface has been used to increase the radiation efficiency and boresight gain of OCAs [36-41]. For example, as presented in Figure 6.15, a 235 GHz double-layered dipole antenna is fed by the ground-signal-ground (GSG) pads through a balun on the M6 layer, while the entire structure is backed by a specially designed AMC surface on the M1 layer. Eventually, the AMC-based on-chip dipole antenna presents a decent gain of 0 dBi and a high radiation efficiency of 63%.

Figure 6.13 Geometry of a square patch-based AMC surface [32]

Figure 6.14 Geometry of a square patch-based AMC surface [35]

Figure 6.15 3D view of the AMC-based on-chip dipole antenna [36].

6.3.1.3 Superstrate

As mentioned in Section II, for a typical OCA, more EM energy goes to the high-permittivity silicon substrate instead of free space radiation. This is one of the major causes of OCAs' low radiation efficiency. One way to improve this situation is by adding a high-permittivity substrate on top of the OCA, also known as a superstrate.

Figure 6.16 illustrates the superstrate-substrate concept that can be beneficial for an OCA design. High boresight directivity can be achieved through this arrangement. With proper design, radiated power in air can be enhanced compared with the power coupled to the lossy silicon substrate, thus enhancing the radiation efficiency, as well. Although the use of a superstrate tends to somewhat increase the dielectric loss, it can be minimized by using low-loss material for the superstrate implementation. Nonetheless, through the appropriate use of a superstrate, the overall OCA gain can be enhanced at the boresight. To understand and analyze the high-gain condition, transmission line theory is considered convenient for theoretical investigation [42, 43]. This high-gain condition is also known as the radiation resonance condition because the equivalent transmission lines at the boresight under this condition act as a resonance circuit [42]. In terms of transmission line theory, each dielectric layer can be treated as an equivalent transmission line with a certain characteristic impedance. The thickness of the superstrate layer greatly impacts the resonance condition. Theoretically, for the high-directivity resonance condition, the thickness of the high-permittivity superstrate must be equal to odd multiples of a quarter wavelength. In other words, the superstrate behaves similarly to a quarter-wavelength impedance transformer [42]. It is relatively easier to realize a superstrate, as it is simply a dielectric layer with no metallization patterns required.

Figure 6.16 The superstrate-substrate concept

Recently, on-chip implementations of superstrate layers have been reported for enhancing the OCA's radiation performance [37, 44-46]. For example, in [44], an 89 GHz elliptical slot antenna has been realized in a CMOS 0.13 μm process with an off-chip quartz superstrate, as illustrated in Figure 6.17 (a). Through the integration of the quarter-wavelength superstrate, the OCA achieves 6.4 dB of gain enhancement and approximately a 20% radiation efficiency enhancement. Since a relatively thicker superstrate is realized for OCA gain enhancement, it can also protect the chip from the environment. An example of the superstrate layer acting as the chip package, in addition to providing gain enhancement, has been demonstrated in [37]. However, one downside is that considerable reflection can occur at the interface between the high-permittivity superstrate and the air, if the design is not optimized appropriately. Furthermore, surface waves can be generated, which can distort the radiation pattern and degrade the radiation efficiency to some extent. To resolve the generation of surface waves in the superstrate, an artificial dielectric layer (ADL) has been proposed to be used as a superstrate layer for OCA [47, 48]. A dielectric material's equivalent relative permittivity can be increased to a high value by embedding several layers of specially designed non-resonant

periodic metallic structures, known as the ADL. The ADL can be used as a superstrate layer for OCAs' gain enhancement without any surface waves due to its anisotropic properties [47]. In [48], an ADL superstrate with an equivalent relative permittivity of 32 has been designed and stacked on top of an on-chip dipole antenna, as presented in Figure 6.17 (b). This resulted in a considerably high radiation efficiency of 87 % and a decent gain of 6.8 dBi at 280 GHz.

Figure 6.17 (a) Stack-up for on-chip elliptical slot antenna with off-chip quartz superstrate [44], (b) on-chip dipole antenna loaded with artificial dielectric superstrate [48]

6.3.1.4 Focusing Lens

Lens structures have been widely used in optical systems; however, lens can also be used in the microwave or mm-wave range of frequencies for directivity enhancement. Similar to the superstrate case, lens can be beneficial for OCA radiation performance enhancement.

Primarily three different lens configurations have been investigated for OCAs' gain enhancement in the literature [5, 49-56]. The first is the use of a silicon hemispherical lens at the backside of the chip [5, 49-53], as displayed in Figure 6.18 (a). As mentioned in Section II, the generation of high-order surface waves is a critical issue for OCA design. In addition, most radiated waves are absorbed by the silicon substrate. The advantage of a backside silicon hemisphere lens is that it can help to transform the unwanted backside radiation and surface waves into useful radiation from the backside [5]. Moreover, the silicon lens behaves as a heat sink to dissipate the heat generated by the active on-chip circuits. The silicon lens must be specially designed with respect to the OCA's operational frequency. For example, in [49], a silicon lens has been designed and attached to the backside of the 120 GHz OCA's silicon substrate, as presented in Figure 6.18 (a). A matching layer has been coated on top of the silicon lens to match the characteristic impedance in silicon (110Ω) to the characteristic impedance in air (377Ω) [5]. This helps to achieve a high gain of 16.7 dBi and a radiation efficiency of 86.4% at 122 GHz. However, this approach restricts the OCA's radiation to the backside, and all the radiated EM waves must pass through the lossy silicon substrate. In addition, the unwanted small air gap between the chip and silicon lens can cause impedance mismatching [55]. Alternately, a boresight hemispherical lens has also been proposed for OCAs' gain enhancement [54-56]. In this configuration, the dielectric lens is placed on top of the OCA at a certain distance, which is typically

one focal length. Figure 6.18 (b) displays a 300 GHz OCA placed in a multi-layered low-temperature co-fired ceramic (LTCC), where the silicon hemispherical lens has been placed on top of the OCA with an air cavity between them [54]. In this design, the OCA achieved more than 90% radiation efficiency. One of the major issues for the conventional hemispherical lens is that it has a relatively large size compared with the OCA. To reduce the lens size, a Fresnel lens has been proposed to enhance the OCA's boresight gain [57]. For enhanced functionality, the chip package has been shaped into a Fresnel lens structure for gain enhancement. As presented in Figure 6.18 (c), a Fresnel-lens-shaped package provides protection and gain enhancement.

Figure 6.18 (a) Silicon hemispherical lens attached to the backside of IC [49], (b) structure of OCA with boresight silicon hemispherical lens in LTCC [54], (c) OCA with superstrate layer in a proposed Fresnel lens package[57]

6.3.2 Co-Simulation of OCAs and Circuits

As previously discussed, conducting accurate co-simulations of OCAs and circuits that account for all kinds of couplings between the two (through substrate and through air) is challenging. In this section, several state-of-art co-simulation methods and simulators are introduced.

CST STUDIO SUITE [15] provides a co-simulation approach, which is named a transient EM/circuit co-simulation solution. In this solution, the 3D structures of the OCA can be symbolized by a block in a schematic, while the circuit components are connected to the ports of this 3D OCA's structure block. Then, a single simulation is performed with exactly the same excitation defined in the

circuit simulation. The circuit's output is then fed to the OCA for EM simulations. The EM and circuit simulations run simultaneously, indicating that the currents and voltages are continuously exchanged at the interface of the circuit and OCA's block. This approach is beneficial because of its bidirectional simulation nature and faster simulation speed, as the OCA's full S-parameters are not required [18]. However, there does not yet exist an example that reveals that this simulation approach has been used for the co-simulation of the OCA and the circuits. Nonetheless, the main drawback is that this approach does not account for the OCA's radiation in addition to the coupling effects between the OCAs and the circuits, as this is only a schematic-level simulation. Similarly, in [19], the partial element equivalent circuit (PEEC) theory has been presented to model the antenna as an equivalent circuit with several lumped circuit components. This approach enables a co-simulation between the antenna and the circuits in both the frequency and time domain; however, this also does not include the coupling effects. To incorporate the coupling effects in the co-simulation, WiPL-D Microwave proposes a different co-simulation strategy [58]. The OCA's EM models can be pre-parameterized and imported into the circuit as any other circuit component. The inclusion of the EM models enables the investigation of an OCA's radiation and coupling effects between the OCA and the circuits. However, only limited options of antenna types are available in the 3D model library of the simulator, which restricts the design freedom for antenna designers.

In addition to including EM models of the antennas in the circuit simulations, the lumped circuit components can be imported in the EM simulator for co-simulations. In [59], the lumped circuit components and their characteristics are included in EM simulation through the finite difference time domain (FDTD) updating equations. The lumped circuit components contain active sources; nonlinear circuit elements, such as diodes and transistors; and linear circuit elements, such as resistors, capacitors, and inductors. When a circuit component is placed between the two nodes, its performance can be characterized by the I - V curve between the two nodes, where I and V represent the current flows through the circuit components and the voltage across the two nodes, respectively. According to Maxwell's curl equation (as presented below), the electric currents that flow through the circuit component, denoted as an impressed current density of J_i , are the sources that lead to the generation of electric fields and magnetic fields in the computational domain [60].

$$\nabla \times \vec{H} = \epsilon \frac{\partial \vec{E}}{\partial t} + \sigma^e \vec{E} + \vec{J}_i$$

where the electric field E and J_i can be expressed by the following two equations:

$$\vec{E} = -\nabla V$$

$$I = \int_S \vec{J} \cdot d\vec{s}$$

where S is the cross section of a unit cell perpendicular to the flow direction of the current. With the help of this approach, the circuit simulation can be transformed into an EM simulation, making it possible to run a true co-simulation for the OCAs and the circuits in an EM simulator. This functionality has been integrated into an EM simulator: the Computational Electromagnetic Simulator (CEMS) [59].

6.3.3 Advance On-Chip Antenna Characterization Methods

As mentioned in Section II, the accurate and reliable characterization of the OCA is one of the major challenges. The OCA cannot be measured through connector-based methods in a conventional chamber. Although in recent years, a few dedicated chambers for OCA characterization have become commercially available, they are quite expensive and complicated to use. As OCAs' characterization requires RF probe feeding, which is much larger than the antenna itself, a number of issues arise, such as unwanted interference and self-radiation of the probe. To improve the accuracy and reliability of OCAs' characterization, several potential solutions are discussed in this section.

In some cases, OCAs are connected to the circuits on the same chip, making it impossible to directly measure the OCAs' reflection coefficient by landing the RF probe. In [26], a focus ion beam (FIB) has been used to cut off the connection between the OCA and its driving circuits so that independent impedance characterization can be performed without the loading effects from the circuit part. However, cutting off the connection is an irreversible process. In [61], a de-embedding process for a balun circuit has been conducted in a simulator to eliminate its effects on the characterization of OCAs' reflection coefficient. In addition to the aforementioned issue, the unwanted coupling effects between the probe conductor body and the OCA can cause considerable discrepancies between the simulated and measured results, though the influence of the probe's inner impedance can be eliminated through proper calibration at the plane of the probe tips. In [62], an air coplanar probe has been modeled in HFSS, as illustrated in Figure 6.19, and its ABCD matrix has been obtained by exciting it from the coaxial side and landing the probe on short, open, and load calibration substrate in HFSS. Following this, a new simulation is performed after the calibration substrate is replaced with the OCA in HFSS. Based on the simulated results from the above two simulations, the de-embedding process is applied to remove the probe's inner impedance influence on the OCA reflection coefficient. The coupling effects between the probe and the OCA are also included in the simulation. Therefore, the simulated results with the probe model, after de-embedding, demonstrate satisfactory agreement with the measured results.

Figure 6.19 3D schematic of the chip and probe model feeding the L antenna [62]

Other than the characterization of the OCA's reflection coefficient, the radiation pattern's measurement is strongly affected by the presence of the RF

probe, as discussed in Section II. Several methods have been presented in the literature for minimizing the probe's negative influence on the measurement of the OCA's radiation pattern [23, 25, 63, 64]. To eliminate the influence of probe self-radiation, two probe radiation de-embedding methods are proposed in [63]. Two measurements are required for the first method. As presented in Figure 6.20 (a), the RF probe is placed in the air while remaining close to the OCA. In this setup, the probe's self-radiation can be measured, denoted as $S_{21}^{(P1)}$. In the second setup, the RF probe is landed on the OCA to excite it. Then, the overall radiation pattern $S_{21}^{(2)}$ can be obtained, which is a combination of probe self-radiation $S_{21}^{(P2)}$ and the OCA's radiation $S_{21}^{(a)}$. To obtain only the OCA's radiation, the probe self-radiation can be de-embedded from the measured radiation pattern. Although the probe self-radiation is not available in setup 2, it can be obtained by scaling the magnitude of the probe self-radiation in setup 1. Eventually, the antenna radiation can be calculated from the following equation [63]:

$$S_{21}^{(a)} = S_{21}^{(2)} - S_{21}^{(P2)} = S_{21}^{(2)} - \text{ScalingFactor} \times S_{21}^{(P1)}$$

Another method has been proposed in [63] for de-embedding the influence of the probe self-radiation. As displayed in Figure 6.20 (b), this method requires two identical OCAs and RF probes. The S_{21} results are measured in four different measurement setups. For the first setup, both probes are landed on OCAs, indicated as $(P, A)(P, A)$. For the second and third measurement setups, one RF probe is landed, while the other probe is floating in the air, denoted $(P)(P, A)$. In the last measurement setup, the measured S_{21} parameter $(P)(P)$ is obtained when both probes are not landed and are in the air; then, the desired S_{21} parameter of the OCA to OCA, denoted $(A)(A)$, can be calculated according to the phasor subtraction, as follows [63]:

$$(A)(A) = (P, A)(P, A) - (P)(P) - (P)(P, A) - (P, A)(P)$$

However, the de-embedding results of the S_{21} are obtained for only one direction. To obtain the radiation pattern based on this de-embedding method, the relative locations of the two OCAs can be adjusted to obtain the radiation pattern on the horizontal plane, as presented in Figure 6.20 (b). However, this approach requires multiple probe landings, which is time consuming and has a high chance of damaging the probe and RF pads.

(a)

(b)

Figure 6.20 Probe radiation de-embedding methods: (a) one probe based, (2) two probe based [63]

Although the probe self-radiation can be de-embedded by applying the aforementioned methods, the strong interference between the OCA and RF probe still exists. Several strategies have been employed to minimize the unwanted reflection from the probe conductor body [23, 25, 64]. A probe with less interference and smaller radiation blockage has been proposed in [64]. As illustrated in Figure 6.21 (a), the probe tip feeder has been modified so that the large probe conductor body is moved away from the OCA. Therefore, the interference between the OCA and the RF probe is minimized. Moreover, the radiation blockage area is reduced to only 20 degrees. A similar approach has been presented in [25], in which an extended waveguide is used to increase the distance between the probe tips and the probe conductor body, as displayed in Figure 6.21 (b). To further reduce the interference and radiation blockage area, a bent RF probe has been proposed in [23]. Figure 6.21 (c) reveals that the large probe conductor body is moved to the backside of the OCA by bending the waveguide between the probe tips and probe conductor body. In addition, an RF absorber is inserted between the OCA and the probe to further decrease the interference.

Figure 6.21 Novel probe configurations for less interference: (a) probe with less scattering [64], (b) extended probe model [25], (c) bent probe model [23]

6.4 Emerging Trends

It is well established that many advantages exist to integrating antennas on the chip, such as a lower overall cost, smaller physical size, lighter weight, and lower power consumption, among others. All these features are extremely important for portable and compact wireless devices, such as wireless sensors for IoT applications or compact radar systems, among others. With the aforementioned competitive advantages and due to the relevant emerging applications, it is expected that the field of OCA will surge further in the foreseeable future. This section describes some of the emerging trends that will dictate the future directions of research in the field of OCAs.

6.4.1 Drive Toward Higher Frequencies Reaching Terahertz Bands

With the maturity and refinement of CMOS processes, it is feasible to have operating frequencies that reach the sub-terahertz bands (100–300 GHz) or even early terahertz bands (300–3,000 GHz). The size of the antenna becomes extremely small, and thus, it becomes feasible to have antenna arrays on chip rather than only a single antenna. This is extremely attractive for phased arrays, particularly for imaging systems. Moreover, there is more available bandwidth for the OCA in the sub-terahertz and terahertz frequency bands, which is beneficial for extremely high-data-rate communication systems.

Recently, considerable research has focused on the sub-terahertz and terahertz OCA designs, which can be applied in multiple important applications, such as high-data-rate communication systems, short-range radar systems, medical detections, and imaging [53, 65-71]. In [65], a 340 GHz patch OCA is realized and integrated with a receiver front-end in 40 nm CMOS technology, which is a good candidate for the applications of THz biomedical imaging. In another work, a 300 GHz dipole OCA is integrated with an ASK receiver circuit for the application of high-data-rate communication [53]. This antenna achieves a high gain of 24 dBi by packaging the chip with a silicon lens. In addition, the antenna has a large bandwidth of more than 50 GHz, which makes it possible for the overall system to achieve a high data rate of 24 Gbps for a communication range of 3 m. Other than the investigation of sub-terahertz OCAs, some examples demonstrate the CMOS OCA designs in terahertz frequencies [68-71]. For example, in [70], a graphene patch antenna is proposed for a wireless on-chip network at 2.5 THz. This graphene-based OCA is compatible with the CMOS process. In simulations, a gain of 5 dBi has been achieved.

Although there exist many attractive applications for sub-terahertz and terahertz OCAs, several challenges must be tackled in the near future. First, OCAs in the sub-terahertz and terahertz frequency range also suffer from low radiation efficiency. This is more critical for these high-frequency bands because the RF power generated on chip is low. The issue of surface waves is also more prominent at these frequencies. Second, as the frequency increases, the probe feeding also becomes complicated for the characterizations of the OCAs due to the size of the probe tips being comparable to the OCAs.

6.4.2 OCA Becoming a Key for Biomedical Wireless Implants

Recently, with the rapid development of biomedical technology and the personalized healthcare system, biomedical implantable devices have attracted

much attention. The concept of implanting a medical monitoring or treatment device in the human body, which can send out information about health conditions in a wireless fashion, has opened many doors for healthcare providers [72]. Naturally, the space is limited to biomedical-implantable devices; thus, compactness and low power consumption are two important features for such devices. The OCA, as an ultimate solution for compactness, is considered to be the best candidate for the realization of wireless biomedical implantable devices. It is important to design miniaturized OCAs while keeping an acceptable radiation performance to ensure efficient communication between the device and its reader. In addition to the challenge of OCA miniaturization, the human body effects must be considered during the design stage of the implantable OCA because the presence of human body tissue can strongly degrade the antenna's performance. Some examples of biomedical implantable OCA can be found in the literature. For example, in [73], a chip is proposed to be implanted in the human eye for monitoring the intraocular pressure, as presented in Figure 6.22. In this chip, a specially designed octagonal loop acts as both the inductor for the VCO and the antenna for the transmitter at 2.45 GHz. Designed in a $0.18\ \mu\text{m}$ CMOS process, a 5.2 GHz receiving monopole OCA is also integrated in the same chip for wirelessly powering the chip. Overall, an acceptable read range of ~ 10 cm is achieved for this wireless sensing system. To miniaturize the OCA size, a highly meandered differential wire OCA is presented in [74], which realizes a detection range of approximately 6 cm with a -42 dB link gain at 900 MHz. With improvements in the CMOS processes and maturity of OCA technology, improved performance can be achieved in future, which will open doors for the widespread use of OCA technology in biomedical applications.

Figure 6.22 Implantation of the SoC in the anterior chamber of the human eye [73]

6.4.3 Advanced Simulation Platforms for Co-design of OCAs and Circuits

A true co-design simulation platform is one that can include all aspects, such as coupling effects, the influence of OCA radiation on IC performance, and impedance matching, among others. The time-consuming iterative process between an OCA simulator and an IC simulator can be avoided through this approach. However, a simulator, which can provide the aforementioned simulation features simultaneously, is not available at present. Although several co-simulators have been developed recently [18, 58], and a novel co-simulation strategy has been

proposed in [59], there remain many unresolved issues. Issues include the port definition in the EM simulator not being compatible with the circuit simulation, or the requirement of extremely small meshing for the fine structures in the circuit layout, which increases the EM simulation time considerably, or truly capturing the coupling effects between the OCA and the circuits; these are some of the many deficiencies that the existing simulators have. This is an active area of research for computational tool developers on both the computational EM and circuits side.

6.4.4 Specialized CMOS Process for OCA

As mentioned in Section II, the incompatibility of the commercially used CMOS stack-up is the major reason for the OCA's low radiation efficiency and the excitation of unwanted surface waves. A silicon substrate with low resistivity and thin inter-metal dielectric layers is suitable for IC designs; however, the bulk material properties of the silicon substrate and the CMOS stack-up are not suitable for the efficient realization of OCAs. Nonetheless, with the growing interest in OCA, questions are being raised regarding specialized processes that offer the best of both worlds, referring to processes that can accommodate circuits and antennas efficiently. Some mainstream foundries are investigating this issue. However, there exist several examples that demonstrate considerable radiation efficiency enhancement of OCAs by applying specialized fabrication processes, such as bulk micromachining or proton implantation [11, 29-31]. However, these modifications are for the entire substrate and thus are not useful for circuits. One possible solution is selective alteration of the silicon substrate (i.e., pockets of high resistivity are created in bulk Si, in which the OCA can be realized efficiently, while the resistivity remains unchanged in the circuit area). Other options, such as realization of OCA on the thick-field oxide rather than the metal layers on the thin oxides, may also be beneficial. Based on the above discussion, it can be seen that it is required that antenna designers, IC designers, and nanofabrication engineers work in close collaboration to develop specialized CMOS processes that are suitable for the efficient integration of both OCAs and circuits.

Reference

- [1] R. T. Rao, *System on Package: Miniaturization of the Entire System*. New York: McGraw-Hill Education (in eng), 2008.
- [2] Y. P. Zhang and D. Liu, "Antenna-on-Chip and Antenna-in-Package Solutions to Highly Integrated Millimeter-Wave Devices for Wireless Communications," *IEEE Transactions on Antennas and Propagation*, vol. 57, no. 10, pp. 2830-2841, 2009, doi: 10.1109/TAP.2009.2029295.
- [3] F. Semiconductor, "Understanding Latch-Up in Advanced CMOS Logic," *Fairchild Semiconductor Corporation, Tech. Rep*, 1999.
- [4] H. M. Cheema and A. Shamim, "The last barrier: on-chip antennas," *IEEE Microwave Magazine*, vol. 14, no. 1, pp. 79-91, 2013, doi: 10.1109/MMM.2012.2226542.
- [5] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Receiver and Antennas," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2795-2806, 2006, doi: 10.1109/JSSC.2006.884811.
- [6] L. Marnat, A. A. A. Carreno, D. Conchouso, M. G. Martı́nez, I. G. Foulds, and A. Shamim, "New Movable Plate for Efficient Millimeter Wave Vertical on-Chip Antenna," *IEEE Transactions on Antennas and Propagation*, vol. 61, no. 4, pp. 1608-1615, 2013, doi: 10.1109/TAP.2013.2241720.
- [7] K. Huang and D. D. Wentzloff, "60 GHz on-chip patch antenna integrated in a 0.13- μ m CMOS technology," in *2010 IEEE International Conference on Ultra-Wideband*, 20-23 Sept. 2010 2010, vol. 1, pp. 1-4, doi: 10.1109/ICUWB.2010.5615699.
- [8] K. Huang and D. D. Wentzloff, "A 60 GHz Antenna-Referenced Frequency-Locked Loop in 0.13 μ m CMOS for Wireless Sensor Networks," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2956-2965, 2011, doi: 10.1109/JSSC.2011.2162768.
- [9] J. Briaire and S. Krisch, "Principles of substrate crosstalk generation in CMOS circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 6, pp. 645-653, 2000, doi: 10.1109/43.848086.
- [10] T. Deng and Y. P. Zhang, "On-Chip Antennas," in *Handbook of Antenna Technologies*, Z. N. Chen, D. Liu, H. Nakano, X. Qing, and T. Zwick Eds. Singapore: Springer Singapore, 2016, pp. 1565-1584.
- [11] H. Chu, Y. Guo, T. Lim, Y. M. Khoo, and X. Shi, "135-GHz Micromachined On-Chip Antenna and Antenna Array," *IEEE Transactions on Antennas and Propagation*, vol. 60, no. 10, pp. 4582-4588, 2012, doi: 10.1109/TAP.2012.2209855.
- [12] K. Kang *et al.*, "A 60-GHz OOK Receiver With an On-Chip Antenna in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1720-1731, 2010, doi: 10.1109/JSSC.2010.2053095.
- [13] S. Uemura, Y. Hiraoka, T. Kai, and S. Dosho, "Isolation Techniques Against Substrate Noise Coupling Utilizing Through Silicon Via (TSV) Process for RF/Mixed-Signal SoCs," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 4, pp. 810-816, 2012, doi: 10.1109/JSSC.2012.2185169.
- [14] Ansys.com. (n.d.). ANSYS HFSS: High Frequency Electromagnetic Field Simulation Software. [online] Available at: <https://www.ansys.com/products/electronics/ansys-hfss>.
- [15] CST Studio Suite 3D EM simulation and analysis software. [Online] Available at: <http://www.cst.com>.

- [16] Cadence: EDA Tools and IP for Intelligent System Design. [online] Available at: <https://www.cadence.com>.
- [17] Keysight: PathWave Advanced Design System (ADS). [online] Available at: <https://www.keysight.com/zz/en/products/software/pathwave-design-software/pathwave-advanced-design-system.html>.
- [18] A. Scott and V. Sokol, "True Transient 3D EM/Circuit Co-Simulation Using CST STUDIO SUITE," *Conference Proceedings*, 2008.
- [19] Y. Zhang, N. H. W. Fong, D. C. W. Ng, and N. Wong, "Co-simulation of RFIC with bondwire antenna via retarded PEEC method," in *2012 IEEE International Symposium on Circuits and Systems (ISCAS)*, 20-23 May 2012 2012, pp. 229-232, doi: 10.1109/ISCAS.2012.6271751.
- [20] M. R. Karim, X. Yang, and M. F. Shafique, "On Chip Antenna Measurement: A Survey of Challenges and Recent Trends," *IEEE Access*, vol. 6, pp. 20320-20333, 2018, doi: 10.1109/ACCESS.2018.2821196.
- [21] R. N. Simons, "Novel On-Wafer Radiation Pattern Measurement Technique for MEMS Actuator Based Reconfigurable Patch Antennas," in "NASA STI/Recon Technical Report N," October 01, 2002 2002, vol. 02. [Online].
- [22] D. Titz, F. Ferrero, and C. Luxey, "Development of a Millimeter-Wave Measurement Setup and Dedicated Techniques to Characterize the Matching and Radiation Performance of Probe-Fed Antennas [Measurements Corner]," *IEEE Antennas and Propagation Magazine*, vol. 54, no. 4, pp. 188-203, 2012, doi: 10.1109/MAP.2012.6309179.
- [23] A. C. F. Reniers, A. R. v. Dommele, A. B. Smolders, and M. H. A. J. Herben, "The Influence of the Probe Connection on mm-Wave Antenna Measurements," *IEEE Transactions on Antennas and Propagation*, vol. 63, no. 9, pp. 3819-3825, 2015, doi: 10.1109/TAP.2015.2452941.
- [24] S. Beer and T. Zwick, "Probe based radiation pattern measurements for highly integrated millimeter-wave antennas," in *Proceedings of the Fourth European Conference on Antennas and Propagation*, 12-16 April 2010 2010, pp. 1-5.
- [25] L. Boehm, M. Hitzler, F. Roos, and C. Waldschmidt, "Probe influence on integrated antenna measurements at frequencies above 100 GHz," in *2016 46th European Microwave Conference (EuMC)*, 4-6 Oct. 2016 2016, pp. 552-555, doi: 10.1109/EuMC.2016.7824402.
- [26] H. Zhang and A. Shamim, "Tackling the Issues of Millimeter-wave On-chip Antenna Measurements," in *2019 13th European Conference on Antennas and Propagation (EuCAP)*, 31 March-5 April 2019 2019, pp. 1-5.
- [27] S. Ranvier, M. Kyrö, C. Icheln, C. Luxey, R. Staraj, and P. Vainikainen, "Compact 3-D On-Wafer Radiation Pattern Measurement System for 60 GHz Antennas," *COST 2100, Pervasive Mobile & Ambient Wireless Communications*, vol. 51, 02/01 2009, doi: 10.1002/mop.24034.
- [28] S. Spearing, "Micro Devices and Micro Systems, Materials for," 2016.
- [29] I. Papapolymerou, R. F. Drayton, and L. P. B. Katehi, "Micromachined patch antennas," *IEEE Transactions on Antennas and Propagation*, vol. 46, no. 2, pp. 275-283, 1998, doi: 10.1109/8.660973.
- [30] W. T. Khan *et al.*, "A D-Band Micromachined End-Fire Antenna in 130-nm SiGe BiCMOS Technology," *IEEE Transactions on Antennas and Propagation*, vol. 63, no. 6, pp. 2449-2459, 2015, doi: 10.1109/TAP.2015.2416751.
- [31] K. T. Chan, A. Chin, Y. B. Chen, Y. Lin, T. S. Duh, and W. J. Lin, "Integrated

- antennas on Si, proton-implanted Si and Si-on-quartz," in *International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224)*, 2-5 Dec. 2001 2001, pp. 40.6.1-40.6.4, doi: 10.1109/IEDM.2001.979659.
- [32] G. Goussetis, A. P. Feresidis, and J. C. Vardaxoglou, "Tailoring the AMC and EBG characteristics of periodic metallic arrays printed on grounded dielectric substrate," *IEEE Transactions on Antennas and Propagation*, vol. 54, no. 1, pp. 82-89, 2006, doi: 10.1109/TAP.2005.861575.
- [33] H. Mosallaei and K. Sarabandi, "Antenna miniaturization and bandwidth enhancement using a reactive impedance substrate," *IEEE Transactions on Antennas and Propagation*, vol. 52, no. 9, pp. 2403-2414, 2004, doi: 10.1109/TAP.2004.834135.
- [34] A. P. Feresidis, G. Goussetis, W. Shenhong, and J. C. Vardaxoglou, "Artificial magnetic conductor surfaces and their application to low-profile high-gain planar antennas," *IEEE Transactions on Antennas and Propagation*, vol. 53, no. 1, pp. 209-215, 2005, doi: 10.1109/TAP.2004.840528.
- [35] B. S. Cook and A. Shamim, "Utilizing Wideband AMC Structures for High-Gain Inkjet-Printed Antennas on Lossy Paper Substrate," *IEEE Antennas and Wireless Propagation Letters*, vol. 12, pp. 76-79, 2013, doi: 10.1109/LAWP.2013.2240251.
- [36] H. Zhu, X. Li, W. Feng, J. Xiao, and J. Zhang, "235 GHz on-chip antenna with miniaturised AMC loading in 65 nm CMOS," *IET Microwaves, Antennas & Propagation*, vol. 12, no. 5, pp. 727-733, 2018, doi: 10.1049/iet-map.2017.0710.
- [37] H. Zhang and A. Shamim, "Gain and Efficiency Enhancement of a 77 GHz On-Chip Antenna through AMC and Superstrate Package," in *2018 IEEE International Symposium on Antennas and Propagation & USNC/URSI National Radio Science Meeting*, 8-13 July 2018 2018, pp. 363-364, doi: 10.1109/APUSNCURSINRSM.2018.8608189.
- [38] X. Bao, Y. Guo, and Y. Xiong, "60-GHz AMC-Based Circularly Polarized On-Chip Antenna Using Standard 0.18- μ m CMOS Technology," *IEEE Transactions on Antennas and Propagation*, vol. 60, no. 5, pp. 2234-2241, 2012, doi: 10.1109/TAP.2012.2189725.
- [39] H. Kuo, H. Yue, Y. Ou, C. Lin, and H. Chuang, "A 60-GHz CMOS Sub-Harmonic RF Receiver With Integrated On-Chip Artificial-Magnetic-Conductor Yagi Antenna and Balun Bandpass Filter for Very-Short-Range Gigabit Communications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 4, pp. 1681-1691, 2013, doi: 10.1109/TMTT.2013.2247622.
- [40] H. Chu, Y. X. Guo, F. Lin, and X. Q. Shi, "Wideband 60GHz on-chip antenna with an artificial magnetic conductor," in *2009 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, 9 Jan.-11 Dec. 2009 2009, pp. 307-310, doi: 10.1109/RFIT.2009.5383667.
- [41] S. Pan, D. Wang, C. Guclu, and F. Capolino, "High impedance layer for CMOS on-chip antenna at millimeter waves," in *2011 IEEE International Symposium on Antennas and Propagation (APSURSI)*, 3-8 July 2011 2011, pp. 903-906, doi: 10.1109/APS.2011.5996422.
- [42] D. Jackson and N. Alexopoulos, "Gain enhancement methods for printed circuit antennas," *IEEE Transactions on Antennas and Propagation*, vol. 33, no. 9, pp. 976-987, 1985, doi: 10.1109/TAP.1985.1143709.
- [43] N. Alexopoulos and D. Jackson, "Fundamental superstrate (cover) effects on printed circuit antennas," *IEEE Transactions on Antennas and Propagation*, vol. 32, no. 8, pp. 807-816, 1984, doi: 10.1109/TAP.1984.1143433.

- [44] J. M. Edwards and G. M. Rebeiz, "High-Efficiency Elliptical Slot Antennas With Quartz Superstrates for Silicon RFICs," *IEEE Transactions on Antennas and Propagation*, vol. 60, no. 11, pp. 5010-5020, 2012, doi: 10.1109/TAP.2012.2207353.
- [45] M. Uzunkol, O. D. Gurbuz, F. Golcuk, and G. M. Rebeiz, "A 0.32 THz SiGe 4x4 Imaging Array Using High-Efficiency On-Chip Antennas," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2056-2066, 2013, doi: 10.1109/JSSC.2013.2262739.
- [46] J. Xu and D. S. Ricketts, "Broadband W-band on-chip Yagi antenna using superstrate for high efficiency and endfire radiation," in *2014 Asia-Pacific Microwave Conference*, 4-7 Nov. 2014 2014, pp. 360-362.
- [47] W. H. Syed, G. Fiorentino, D. Cavallo, M. Spirito, P. M. Sarro, and A. Neto, "Design, Fabrication, and Measurements of a 0.3 THz On-Chip Double Slot Antenna Enhanced by Artificial Dielectrics," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 2, pp. 288-298, 2015, doi: 10.1109/TTHZ.2015.2399276.
- [48] D. Cavallo, W. H. Syed, and A. Neto, "Artificial dielectric enabled antennas for high frequency radiation from integrated circuits," in *2017 11th European Conference on Antennas and Propagation (EuCAP)*, 19-24 March 2017 2017, pp. 1626-1628, doi: 10.23919/EuCAP.2017.7928187.
- [49] B. Goettel, W. Winkler, A. Bhutani, F. Boes, M. Pauli, and T. Zwick, "Packaging Solution for a Millimeter-Wave System-on-Chip Radar," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 8, no. 1, pp. 73-81, 2018, doi: 10.1109/TCPMT.2017.2758725.
- [50] K. Statnikov, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, "160-GHz to 1-THz Multi-Color Active Imaging With a Lens-Coupled SiGe HBT Chip-Set," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 2, pp. 520-532, 2015, doi: 10.1109/TMTT.2014.2385777.
- [51] M. Neshat, D. M. Hailu, M. Nezhad-Ahmadi, G. Z. Rafi, and S. Safavi-Naeini, "Gain Measurement of Embedded On-Chip Antennas in mmW/THz Range," *IEEE Transactions on Antennas and Propagation*, vol. 60, no. 5, pp. 2544-2549, 2012, doi: 10.1109/TAP.2012.2189772.
- [52] J. Grzyb, K. Statnikov, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 210–270-GHz Circularly Polarized FMCW Radar With a Single-Lens-Coupled SiGe HBT Chip," *IEEE Transactions on Terahertz Science and Technology*, vol. 6, no. 6, pp. 771-783, 2016, doi: 10.1109/TTHZ.2016.2602539.
- [53] H. Song, J. Kim, K. Ajito, M. Yaita, and N. Kukutsu, "Fully Integrated ASK Receiver MMIC for Terahertz Communications at 300 GHz," *IEEE Transactions on Terahertz Science and Technology*, vol. 3, no. 4, pp. 445-452, 2013, doi: 10.1109/TTHZ.2013.2252954.
- [54] T. Tajima, H. Song, and M. Yaita, "Compact THz LTCC Receiver Module for 300 GHz Wireless Communications," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 4, pp. 291-293, 2016, doi: 10.1109/LMWC.2016.2537044.
- [55] J. Shi, D. Cui, H. Hao, C. Deng, and X. Lv, "220 GHz high spatial resolution detector with above-chip mounted dielectric lens," *Electronics Letters*, vol. 53, no. 8, pp. 538-540, 2017, doi: 10.1049/el.2016.4755.
- [56] J. Al-Eryani, H. Knapp, J. Kammerer, K. Aufinger, H. Li, and L. Maurer, "Fully Integrated Single-Chip 305–375-GHz Transceiver With On-Chip Antennas in SiGe BiCMOS," *IEEE Transactions on Terahertz Science and Technology*, vol. 8, no. 3, pp. 329-339, 2018, doi: 10.1109/TTHZ.2018.2823202.
- [57] H. Zhang and A. Shamim, "Gain Enhancement of Millimeter-Wave on-Chip Antenna

- through an Additively Manufactured Functional Package," *IEEE Trans. Antennas Propag.*, to be published, 2020.
- [58] WiPL-D. Microwave, "Effective Antenna Design Using EM and Circuit Co-Simulation in WiPL-D Microwave," *Available Online: www.wipl-d.com*.
 - [59] A. Elsherbeni and V. Demir, *The finite-difference time-domain method for electromagnetics with MATLAB® simulations: ACES series, 2nd edition*. 2016, pp. 1-531.
 - [60] R. F. Harrington, *Time-Harmonic Electromagnetic Fields*. Wiley, 2001.
 - [61] A. Shamim, L. Roy, N. Fong, G. Tarr, and V. Levenets, "On-Chip Antenna Measurements: Calibration and De-embedding Considerations," in *2005 IEEE Instrumentation and Measurement Technology Conference Proceedings*, 16-19 May 2005, vol. 1, pp. 463-466, doi: 10.1109/IMTC.2005.1604158.
 - [62] M. Seyyedesfahlan and I. Tekin, "ACP Probe Measurement of On-Chip Strip Dipole Antennas at W Band," *IEEE Transactions on Antennas and Propagation*, vol. 64, no. 4, pp. 1270-1278, 2016, doi: 10.1109/TAP.2016.2529642.
 - [63] J. N. Murdock, E. Ben-Dor, F. Gutierrez, and T. S. Rappaport, "Challenges and approaches to on-chip millimeter wave antenna pattern measurements," in *2011 IEEE MTT-S International Microwave Symposium*, 5-10 June 2011, pp. 1-1, doi: 10.1109/MWSYM.2011.5973566.
 - [64] Z. Tsai, Y. Wu, S. Chen, T. Lee, and H. Wang, "A V-Band On-Wafer Near-Field Antenna Measurement System Using an IC Probe Station," *IEEE Transactions on Antennas and Propagation*, vol. 61, no. 4, pp. 2058-2067, 2013, doi: 10.1109/TAP.2012.2237091.
 - [65] C. Li, C. Ko, M. Kuo, and D. Chang, "A 340-GHz Heterodyne Receiver Front End in 40-nm CMOS for THz Biomedical Imaging Applications," *IEEE Transactions on Terahertz Science and Technology*, vol. 6, no. 4, pp. 625-636, 2016, doi: 10.1109/TTHZ.2016.2566580.
 - [66] P. H. Siegel, "Terahertz technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 910-928, 2002, doi: 10.1109/22.989974.
 - [67] D. L. Woolard, R. Brown, M. Pepper, and M. Kemp, "Terahertz Frequency Sensing and Imaging: A Time of Reckoning Future Applications?," *Proceedings of the IEEE*, vol. 93, no. 10, pp. 1722-1743, 2005, doi: 10.1109/JPROC.2005.853539.
 - [68] Z. Ahmad and K. O. Kenneth, "0.65–0.73THz quintupler with an on-chip antenna in 65-nm CMOS," in *2015 Symposium on VLSI Circuits (VLSI Circuits)*, 17-19 June 2015, pp. C310-C311, doi: 10.1109/VLSIC.2015.7231303.
 - [69] B. Khamaisi, S. Jameson, and E. Socher, "0.61THz radiating source with on-chip antenna on 65nm CMOS," in *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, 3-4 Oct. 2016, pp. 389-392, doi: 10.1109/EuMIC.2016.7777573.
 - [70] S. Mrunalini and A. Manoharan, "Dual-band re-configurable graphene-based patch antenna in terahertz band for wireless network-on-chip applications," *IET Microwaves, Antennas & Propagation*, vol. 11, no. 14, pp. 2104-2108, 2017, doi: 10.1049/iet-map.2017.0415.
 - [71] Y. Kanazawa *et al.*, "CMOS Terahertz Imaging Pixel with a Wideband on-Chip Antenna," in *2018 43rd International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, 9-14 Sept. 2018, pp. 1-2, doi: 10.1109/IRMMW-THz.2018.8509895.
 - [72] R. Karim, A. Iftikhar, B. Ijaz, and I. B. Mabrouk, "The Potentials, Challenges, and

- Future Directions of On-Chip-Antennas for Emerging Wireless Applications—A Comprehensive Survey," *IEEE Access*, vol. 7, pp. 173897-173934, 2019, doi: 10.1109/ACCESS.2019.2957073.
- [73] L. Marnat, M. H. Ouda, M. Arsalan, K. Salama, and A. Shamim, "On-Chip Implantable Antennas for Wireless Power and Data Transfer in a Glaucoma-Monitoring SoC," *IEEE Antennas and Wireless Propagation Letters*, vol. 11, pp. 1671-1674, 2012, doi: 10.1109/LAWP.2013.2240253.
- [74] C. Liu, Y. Guo, X. Liu, and S. Xiao, "An Integrated On-Chip Implantable Antenna in 0.18- μm CMOS Technology for Biomedical Applications," *IEEE Transactions on Antennas and Propagation*, vol. 64, no. 3, pp. 1167-1172, 2016, doi: 10.1109/TAP.2016.2518201.