150 nm × 200 nm Cross-Point Hexagonal Boron Nitride-Based Memristors

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Abstract

The introduction of 2D materials in the structure of memristors has been shown to provide the devices with enhanced flexibility and transparency. However, their use is still not well justified, as the electrical performance of 2D materials-based memristors is still behind that of transition

metal oxide (TMO)-based memristors. This work presents the fabrication of metal/*h*-BN/metal memristors with ultra-low power consumption that beat the previous record set by Au/HfO_x:Ag/Au memristors. Moreover, all the methods used to synthesize the 2D materials and fabricate the devices are scalable (e.g., chemical vapor deposition synthesis), and the 2D materials-based memristors here fabricated here use a vertical metal/insulator/metal configuration (i.e., low variability and 3D stackable). To the best of current knowledge, the metal/*h*-BN/metal memristors here presented are the smallest 2D materials-based memristors ever reported.

1. Introduction

Memristors are being considered as one of the most promising candidates for next generation electronic devices and systems, including nonvolatile memories^[1] and neuromorphic systems,^[2,3] due to their high performance, easy fabrication, and high-density integration. A memristor is a two-terminal metal/insulator/metal (MIM) cell that can change its conductivity depending on the electrical stresses previously applied between the two electrodes.^[4] The memristors that exhibit the highest performances operate based on the formation and disruption of a conductive nanofilament (CNF) across the dielectric.^[4] Depending on the metallic and insulating materials used, memristors with different performances can be fabricated. For example Ti/HfO₂/TiN memristors have shown low operation voltages (<0.3 V),^[5] TiN/Ti/HfO₂/TiN memristors have shown fast switching speed (<1 ns),^[6] TiN/Hf/HfO_x/TiN memristors have shown low energy consumption (<0.1 pJ per transition),^[7] Pt/Ta₂O_{5-x}/TaO_{2-x}/Pt memristors have shown outstanding endurance (>10¹² cycles),^[8] and Pt/TaO_x/Pt memristors have shown long retention times (>10 years at 85 °C).^[9] However, so far there is no materials combination able to meet all these performances simultaneously.^[10] Furthermore, other desired properties of memristors like analog linear and symmetric switching or stable multilevel switching have never been reliably fabricated—some claims exist in the literature, but they do not prove the behaviors statistically providing

device-to-device variability information. For these reasons, fabricating memristors using new materials that can meet the performances required is necessary.

The introduction of 2D materials in memristive technologies has gained a substantial amount of interest because they can provide additional capabilities to the devices (e.g., flexibility and transparency).^[11] For example, Graphene has been used as interfacial layer to avoid the interactions between metallic electrodes and the resistive switching (RS) medium (e.g., oxygen vacancies migration from the insulator to electrodes, and metal ion penetration into the insulator).^[12] Other 2D materials like graphene oxide (GO),^[13-17] black phosphorous (BP),^[18] molybdenum disulfide (MoS₂),^[19,20] and hexagonal boron nitride (*h*-BN)^[21] have been used as RS active medium, and the switching mechanisms have been attributed to the migration of intrinsic atomic species in the 2D material (e.g., O in GO, S in MoS₂ and B in *h*-BN), and in some cases it is combined with the penetration of metal ions.^[22] Unfortunately, 2D materials based memristors are still not being taken seriously because: i) most of the works just show proof-of-concept RS observations (e.g., no variability data is presented), ii) they use device structures that are not competitive from a technological point of view (e.g., the 2D material is obtained by mechanical exfoliation, the size of the electrodes is too large, >0.01 mm², and/or they use planar MIM configurations that consume too much space and lead to high device-to-device variability), and iii) the performance of 2D materials based memristors is still behind that of transition metal oxide (TMO)-based memristors in terms of switching speed, power consumption, endurance, and retention.

Here we show the fabrication of vertical cross-point metal/*h*-BN/metal memristors fabricated using scalable chemical vapor deposition (CVD) approach, small size down to 150 nm × 200 nm, and low power consumption down to 0.1 fW in standby mode and 3 nW per state transition. This work implies that, for the first time, 2D materials based memristors overcome the performances of TMO-based memristors (at least from a power consumption point of view). So far, these are the smallest 2D materials based memristors ever reported.

2. Results and Discussion

Figure 1a shows the optical microscope image of Au/Ti/*h*-BN/Au cross-point memristors with sizes ranging from $50\ \mu\text{m} \times 50\ \mu\text{m}$ down to $5\ \mu\text{m} \times 5\ \mu\text{m}$. Both the top electrode (TE) and the bottom electrode (BE) can be easily distinguished by the color contrast, i.e., the Au TE looks yellow and the Au BE looks orange, due to the presence of the multilayer *h*-BN on the BE, which adsorbs a non-negligible amount of light - before the measurement, the *h*-BN on the BE has been removed mechanically and/or electrically. In scanning electron microscope (SEM) images the presence of *h*-BN is evident, as the typical wrinkles can be easily observed (Figure 1b). Atomic force microscopy (AFM) indicates that the surface of the *h*-BN stack after the transfer is reasonably clean (Figure 1c). Sporadic rests of polymer scaffolds derived from the 2D material transfer process (see experimental section) have been found, but their effect is less harmful than in planar field effect transistors, as in RS cells they only produce a decrease of the effective area of the devices —polymer-rich areas are much more insulating than polymer-free areas, and therefore the CNF will never form there because its formation is a stochastic process that always takes place at the weakest location of the active area of the memristor.^[23,24] In more than 20 devices inspected by SEM, the area covered with polymer residues was always <5%, which has a negligible effect on the variability of the properties of these devices. The surface roughness has been analyzed at different spots of the sample by AFM (see Figure 1c), and the uniformity of the *h*-BN stack after transfer can be seen by comparing red and black lines. As it can be observed, the profiles of SiO₂ (black) and *h*-BN/SiO₂ (red) are very similar, indicating that the *h*-BN does not introduce additional roughness. This confirms that the surface of the *h*-BN stack is atomically flat, in agreement with Ref. [25].

Matrixes of Au/Ti/*h*-BN/Au devices with small areas of $150\ \text{nm} \times 200\ \text{nm}$ have been fabricated using electron beam lithography (EBL). Figure 1d,e shows the corresponding SEM images of the devices. Because the EBL processes in a university lab are not optimal, we observe

(via SEM) that 50% of the devices have broken wires or metallic particles attached, resulting in a lower fabrication yield. Nevertheless, still 50% of the devices were fabricated successfully, which allowed us to statistically prove their electrical properties. The cross-sectional transmission electron microscopy (TEM) images prove the correct layered structure of the *h*-BN stacks (9-15 layers) and the correct fabrication of the entire devices (Figure 1f).

Fresh Au/Ti/*h*-BN/Au devices with different areas (Figure 1a) have been stressed by applying current versus voltage (I-V) curves at the top (Ti) electrode (bottom metal grounded). In total, 95 out of 100 devices showed very low currents (<100 pA) for voltages of <2 V (**Figure 2a**), which indicates that the *h*-BN works well as insulator, and that it is mainly free of cracks and/or pinholes. The good reproducibility of the results indicates low device-to-device variability.^[22] The currents increase with the area (Figure 2a) and the current densities, calculated by dividing the currents by the device area, overlap (Figure 2b); this means that the conduction before forming the CNF is homogeneously distributed along the entire active area of the memristor, which is something desired to avoid variability problems.^[10] High temperature I-V curves show clear increase of the leakage currents, even when using inert top electrodes (i.e., Au/*h*-BN/Au, Figure 2c). This indicates that some defects in the *h*-BN stacks may get activated under high temperature; most probably these are boron vacancies, as they show the lowest activation energy in the Au/*h*-BN/Au cell.^[26] When applying higher voltages, the CNF across the multilayer *h*-BN stack can be entirely formed. Statistically, the forming voltage decreases as the device area increases (see Figure 2d) in agreement with previous observations in SiO₂ and TMO insulating films.^[27] Overall Figure 2 demonstrates that *h*-BN stacks can be effectively used as insulator in electronic devices.

Under sequences of I-V curves of opposite polarities, the Au/Ti/*h*-BN/Au memristors show stable bipolar RS (see **Figure 3a**). Interestingly, the cycle-to-cycle variability observed (Figure 3a-c) is similar to that previously reported in HfO₂ and TaO_x based RS devices.^[28] The set and reset voltages (V_{SET} and V_{RESET}) for ≈ 140 RS cycles fall within a difference of just 0.5 V (from 0.5 to 1 V for V_{SET} , and from -0.5 to -1 V for V_{RESET} , see Figure 3b). The resistance in high resistive state

(HRS) and low resistive state (LRS) has been measured (at $V=0.1$ V) and the variability is also small (Figure 3c,d). The I_{LRS}/I_{HRS} ratio is ≈ 100 , which is enough to reliably distinguish each logic resistive state. While conducting an exhaustive endurance test is out of the scope of this work, it should be noted that the number of cycles measured for each device (≈ 150) is comparable to that achieved in other h-BN based memristors,^[22, 29] and larger than that memristors based on other 2D materials. For example, GO-based devices (e.g., Ag/GO/Pt) never showed endurance above 100 cycles.^[11] We have observed repeatable bipolar RS in 128 (out of 135) $5\ \mu\text{m} \times 5\ \mu\text{m}$ Au/Ti/h-BN/Au devices ($\approx 95\%$). It is also worth noting that many of the devices that failed did it not because the permanent dielectric breakdown was triggered, but because the metallic wire that connect the cross-point structure was melted due to the high currents in LRS. Therefore, h-BN memristors fabricated in industrial facilities (i.e., with less contamination) should result in higher endurance.

In order to analyze the device-to-device variability, we selected 12 devices ($5\ \mu\text{m} \times 5\ \mu\text{m}$ Au/Ti/h-BN/Au) and collected several I-V curves (between 40 and 300 cycles) in each of them. In Figure 3e, the median I-V curve for these 12 devices has been plotted. The median was selected according to I_{HRS} : for each device we selected the I-V curve that shows the median I_{HRS} at a voltage of 0.1 V. The deviation detected falls within an order of magnitude, which is comparable to that observed in TMO-based memristors.^[30] Similarly, the variability of V_{SET} is very small (Figure 3f), competitive for memristive technologies.

Au/Ti/h-BN/Au devices with smaller sizes have been also characterized. For all devices studied the smaller the device size, the lower the I_{HRS} (similar to Figure 2a), and I_{LRS} was almost constant independently on the area. As an example, **Figure 4a** shows the typical bipolar RS detected in $150\ \text{nm} \times 200\ \text{nm}$ Au/Ti/h-BN/Au devices. As it can be observed, in most of the cycles $I_{HRS} \approx 10^{-14}$ A (at $V = 0.1$ V, see also Figure 4b), and I_{LRS} before the reset (at $V = -0.1$ V) is ≈ 2 mA, similar to that seen in $5\ \mu\text{m} \times 5\ \mu\text{m}$ devices (Figure 3a). This value is outstanding compared to other memristors reported in the literature, including also memristors made of standard materials (see

Table 1). I_{HRS} is so low that these devices may work even without a selector; the reason should be the excellent insulating nature of the *h*-BN stack.^[31] This feature may be useful to reduce the standby currents of memristors, as well as sneak path in crossbar arrays.

In most cycles the currents after the set (during the backward positive I-V) stay at the current compliance level (I_{CC}) until very low biases (≈ 0.1 V), and in the next (negative) I-V curve I_{LRS} is initially very high. This switching behavior is the most repetitive and $I_{LRS}/I_{HR} = 10^{11}$ (the largest ratio ever reported compared with other devices in **Table 2**, Figure 4b). But there is another group of I-V curves (which increases the overall variability) in which the currents after the set are not so large, and the next (negative) I-V shows a sharp jump before the reset (see dashed blue squares in Figure 4b).

The large jumps observed in the cyclical I-V curves indicate that the RS is driven by the formation/disruption of one or few CNFs in the *h*-BN stack. This has been further corroborated by cross-sectional TEM images (Figure 4c). In our previous work,^[22] we found that the RS in Ti/*h*-BN/Cu devices is governed by B migration into the Ti electrode plus penetration of Ti into the *h*-BN stack (under positive bias applied to the Ti, Cu grounded). The migration of B in the *h*-BN shows certain parallelism to the migration of O in TMOs, but the penetration of Ti in the *h*-BN stack was still necessary to produce the HRS-to-LRS transition (in TMOs if O ions migrate the remaining atoms are metallic, but in *h*-BN if B migrates N stays alone, which is not enough to form a stable and nonvolatile CNF).

When using Cu and Ag as top electrode the preforming currents increase and the forming voltage decrease, while Au shows no forming even after applying 8 V (**Figure 5a**). This was expected, as Cu and Ag ions migrate at lower fields.^[32] For Ti the forming is reached at ≈ 6.5 V. Interestingly, Ag/*h*-BN/Au devices show excellent threshold type RS with ultra-low I_{HRS} (Figure 5b) that beats the previous record in Table 1. These devices may be used as ultra-low power selectors for resistive switching cells; their power consumption in standby is $P = I_{HRS} \times V_{READ} = 1 \text{ fA} \times 0.1 \text{ V} = 0.1 \text{ fW}$, and per transition is $P = I_{CC} \times V_{SET} = 10 \text{ nA} \times 0.3 \text{ V} = 3 \text{ nW}$. As normal

switching time of filamentary memristors are typically below 1 μ s, Ag/*h*-BN/Au devices show extraordinary potential for low energy consumption.

3. Conclusion

Metal/*h*-BN/metal cross-point memristors with sizes down to 150 nm $\times$ 200 nm show reliable threshold and/or bipolar RS (with high yield and low variability) depending on the top electrode material used. The current LRS/HRS ratio can be as high as 10^{11} , the currents in HRS are the lowest ever reported, and the Ag/*h*-BN/Au devices show ultra-low power consumption that may enable their use as selector. We demonstrate that *h*-BN is a reliable RS medium for small size memristive technologies. This work indicates the possibility for further research of memristive devices using layered *h*-BN in a crossbar or other structures.

4. Experimental Section

Device Fabrication: Matrixes of cross-point like bottom electrodes consisting on 40 nm Au on 10 nm Ti have been evaporated on a 300 nm SiO₂/Si wafer after a photolithography step. The shape of an electrode consisted on a 100 μ m $\times$ 100 μ m pad connected to a $\approx$ 150 μ m long wire, with a width ranging from 5 μ m to 50 μ m. Then, a 9-15 layers thick *h*-BN stack (previously grown on a Cu substrate by chemical vapor deposition using borazine as precursor)^[22] was transferred on the bottom electrodes using poly-methyl methacrylate (PMMA) polymer scaffolds (the PMMA was removed after the transfer).^[33] Then, top electrodes with the same shapes as the bottom ones (but rotated 90°) were patterned on the *h*-BN stacks crossing the bottom electrodes, and delimiting devices of areas ranging from 5 μ m $\times$ 5 μ m to 50 μ m $\times$ 50 μ m. Three different top electrode materials were used, leading to Au/Ti/*h*-BN/Au, Au/Ag/*h*-BN/Au and Au/*h*-BN/Au devices. The thickness of the top electrode metals was 40 nm for Au, 20 nm for Ti and 20 nm for Ag, respectively.

For the small size devices, EBL and electron beam evaporation were used. The structure was Au/Ti/*h*-BN/Au and the top metals was 15 nm for Ti.

Transfer of hexagonal boron nitride: The devices investigated in this study needed a standard transfer process of *h*-BN. First, the substrate (300 nm SiO₂/Si) was cleaned by acetone, alcohol, and deionized (DI) water under ultrasonication (KQ-100KDB with 100W) sequentially and each process lasted for 20 min. After the deposition of bottom electrode metal, the target substrate was already prepared. A suitable piece of *h*-BN/Cu ($\approx 0.7 \text{ cm} \times 0.7 \text{ cm}$) was cut from the original *h*-BN foil stored in an electronic moisture proof box located in our clean room (1000 level). The whole transfer process was operated in the clean room to protect the sample from contamination. Two pieces of glass was used to make the *h*-BN/Cu foil keep flat. PMMA (Sigma-Aldrich, molecular weight $\approx 996 \text{ kg mol}^{-1}$) was coated on the surface of *h*-BN via spin coating (500 rpm for 6 s and 3500 rpm for 30 s). After a soft bake (at 100 °C for 3 min), the PMMA/*h*-BN/Cu was put in FeCl₃ saturated solution to etch the Cu foil. This process can last several hours until that the sample showed to be transparency. Then the PMMA/*h*-BN was cleaned in HCl (2 wt%) and deionized water, respectively. After this, it was picked up from the water by the target substrate (Au/Ti/SiO₂/Si in our case) prepared before. We put the PMMA/*h*-BN/Au/Ti/SiO₂/Si in an electric thermostatic drying oven at 50 °C for 5 min, and then whole sample was soaked in acetone over 10 h to remove the top PMMA. Through Optical and SEM images, the presence of *h*-BN stack by the color and wrinkles was observed.

Electron beam lithography: This process includes the steps below: i) PMMA (molecular weight $\approx 200 \text{ kg mol}^{-1}$) was spin-coated on 300 nm SiO₂/Si substrate with 4000 rpm for 15 s. Immediately after that, a soft bake process is needed at 180 °C for 5 min. The thickness of PMMA film is about 200 nm. ii) The EBL system consisting of a pattern generator (Raith Elphy VII) and a Supra 55 SEM from Carl Zeiss is used to form the required electrode pattern. iii) After the electrodes were patterned, the developing process was performed in the particular solution

(isopropanol: methyl isobutyl ketone = 3: 1) for 40 s. After the fabrication, we usually used the optical microscopy to ensure the correct fabrication of EBL.

Device Characterization: Morphologies of the devices were investigated by optical microscope (DM 4000M, Leica), SEM (Supra 55, Carl Zeiss), cross-sectional TEM (JEOL JEM-2100 with a working voltage of 200 kV) and AFM (Multimode V, Veeco). The cross-sectional TEM sample was prepared by using a focused ion beam (FIB) from FEI (model: HELIOS NANOLAB 450S), which can cut thin lamellas from the devices and then these thin lamellas were placed on a copper grid for TEM inspection. The electrical characterizations were collected by using a probe station (M150, Cascade), which was connected with a semiconductor parameter analyzer (4200, Keithley) and temperature control stage (SP72-T2, ERS electronic GmbH). All the I-V curves were collected under DC voltages.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

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List of Figures

Figure 1. a) Optical microscopy image of the $5\ \mu\text{m} \times 5\ \mu\text{m}$ to $50\ \mu\text{m} \times 50\ \mu\text{m}$ Au/Ti/h-BN/Au cross-point RS cells. The size of the pads is $100\ \mu\text{m} \times 100\ \mu\text{m}$. b) SEM image of a $5\ \mu\text{m} \times 5\ \mu\text{m}$ Ag/h-BN/Ag cross-point device. The wrinkles in the *h*-BN stack are detected (even below the top metal electrode). No large polymer residues are observed. c) (Top) AFM topography maps of the SiO₂ (left) and *h*-BN/Au/SiO₂ (right). (Down) Cross-section spectra of random locations in the AFM topography maps obtained on different substrates. The black line is the height of SiO₂. For clarity, the red (*h*-BN/SiO₂) and blue (*h*-BN/Au/SiO₂) lines are offset 4 nm and 12 nm. d) SEM image of a Au/Ti/*h*-BN/Au cross-point device with an area of $150\ \text{nm} \times 200\ \text{nm}$. e) Zoom-in SEM image of one cross-point Au/Ti/*h*-BN/Au device with an area of $150\ \text{nm} \times 200\ \text{nm}$. f) Cross-sectional TEM image of a cross-point Ag/*h*-BN/Au device showing good 2D layered structure in the *h*-BN stack.

Figure 2. a) Preforming I-V characteristic of 95 Au/Ti/h-BN/Au devices with different areas. The currents increase for larger devices. b) Current density obtained by dividing the plots in Figure 2a by the area of each device. The densities overlap (homogeneous currents). c) Preforming I-Vs in five $5\ \mu\text{m} \times 5\ \mu\text{m}$ Au/h-BN/Au devices modifying the temperature from $150\ ^\circ\text{C}$ (first) to $30\ ^\circ\text{C}$ (last). d) Weibull plot of the forming voltage in Ag/h-BN/Au devices depending on their area.

Figure 3. a) I-V curves displaying 140 cycles bipolar RS in a $5\ \mu\text{m} \times 5\ \mu\text{m}$ Au/Ti/h-BN/Au device. b) Statistic analysis of V_{RESET} and V_{SET} in the I-V curves measured in Figure 3a. c) Resistance in HRS/LRS for each cycle shown in Figure 3a. The read voltage was 0.1 V. d) Cumulative probability plot of resistance values shown in Figure 3c. The variability is low. e) Median I-V curves (taking into account I_{HRS}) of twelve $5\ \mu\text{m} \times 5\ \mu\text{m}$ Au/Ti/h-BN/Au devices. The number of I-Vs per device was from 40 to 300. f) Cumulative probability plot of V_{SET} in twelve $5\ \mu\text{m} \times 5\ \mu\text{m}$ Au/Ti/h-BN/Au devices. The number of points per device ranges from 40 to 300.

Figure 4. a) I-V curves displaying 250 cycles bipolar RS in a 150 nm × 200 nm Au/Ti/h-BN/Au device. The number of points per I-V curve was kept low to reduce the test time. The backward I-V after reset is not collected to save time. b) Resistances in HRS and LRS for each cycles shown in Figure 4a. The read voltages are +0.1 V and -0.1 V. c) High resolution cross sectional TEM image collected in a stressed device. The stress induced defects are outlined.

Figure 5. a) Typical forming process in $5\ \mu\text{m} \times 5\ \mu\text{m}$ metal/*h*-BN/Au cells with different top electrodes. b) Typical threshold type RS behavior in Ag/*h*-BN/Au devices.

Table 1. Comparison of standby power consumption (in standby mode) of different memristors reported in the literature. The method used to calculate the power consumption of each reference is further described in the Supplementary Information.

Memristor Structure	Memory Type	Read Voltage	Power Consumption	Size	Reference
Au/HfO _x :Ag/Au	Volatile	0.1 V	10 fW	10 μm ×10 μm	[2]
Pd/HfO _x /Ag	Volatile	0.1 V	10 fW	5 μm ×5 μm	[34]
Ni/GeO _x /HfON/TaN	Non-volatile	0.5 V	0.5 pW	-	[35]
Au/silk-Ag nanowires/Au	Volatile	0.1 V	1 pW	100 μm ×100 μm	[36]
G/SiO _x /G	Non-volatile	1 V	1 pW	100 μm ×100 μm	[37]
Ag/a-Si:H/Pt	Volatile	0.5 V	0.5 pW	0.049 μm^2	[38]
Ag/TiO ₂ /Pt	Volatile	0.1 V	100 fW	0.0314 μm^2	[39]
TE/Doped-chalcogenide/BE	Volatile	0.1 V	1 pW	-	[40]
Pt/Doped-HfO ₂ /Cu	Volatile	0.1 V	100 fW	-	[41]
Au/Ag/ <i>h</i> -BN/Au	Volatile	0.1 V	0.1 fW	5 μm ×5 μm	This work

Table 2. Comparison of the I_{LRS}/I_{HRS} ratio of different memristors reported in the literature.

Memristor Structure	Memory Type	I_{LRS}/I_{HRS} ratio	Size	Reference
Au/HfO _x :Ag/Au	Volatile	$\approx 10^{10}$	10 $\mu\text{m} \times 10 \mu\text{m}$	[2]
Pd/Ag/HfO _x /Ag/Pd	Volatile	$\approx 10^{10}$	5 $\mu\text{m} \times 5 \mu\text{m}$	[34]
TE/SLT/BE	Volatile	$\approx 10^{10}$	100 nm $\times$ 100 nm	[42]
Al/silk:Au NP /ITO	Non-volatile	10^6	$2.8 \times 10^6 \mu\text{m}^2$	[43]
Au/Ti/TiO ₂ /SrTiO ₃ /SiO _x	Non-volatile	$\approx 10^7$	$3.14 \times 10^4 \mu\text{m}^2$	[44]
Cu/ZnO-NW/Pd	Non-volatile	10^6	-	[45]
Cu/a-SiC/Au	Non-volatile	10^8 - 10^{10}	5 $\mu\text{m} \times 5 \mu\text{m}$	[46]
Au/Co:BaTiO ₃ /Pt/Ti/SiO ₂	Non-volatile	$\approx 10^7$	$7 \times 10^4 \mu\text{m}^2$	[47]
Au/Ti/h-BN/Au	Non-volatile	$\approx 10^{11}$	150 nm $\times$ 200 nm	This work