Investigation of On-chip Integrated Inductors Fabricated in SOI-MUMPs for RF MEMS ICs

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Abstract

This paper presents for the first time implementation of zig-zag and solenoidal on-chip inductors in standard and cost effective SOI-MUMPs fabrication process. The solenoidal inductor offers high Q-factor and inductance as compared to planar zig-zag inductor. Bonding wires are used to construct the top conductor loop of the solenoidal inductor. The inductors are also characterized at elevated temperature for performance investigation in harsh environment. The mechanical resonance frequency of the inductors are characterized using the Finite element software COMSOL. The inductors are characterized using a vector network analyzer from 60 MHz to 3 GHz, and the results of both inductors are compared. The total size of the device is $2 \times 0.7 \text{ mm}^2$.

Keywords: On-chip inductor, solenoidal, SOI-MUMPs, Q-factor.

Introduction

The integrated inductor is a key component for compact radio frequency RF systems, such as RF front ends, RF transceivers, RF filters, and matching networks [1, 2]. It is essential for an inductor to have high quality factor (Q-factor) and self-resonant frequency. However, on-chip inductors normally exhibit low Q factor [3, 4]. Particularly, CMOS-based inductors suffer due to their low quality factor [5, 6]. Alternatively, Microelectromechanical systems (MEMS) inductors offer better performance in terms of the Q-factor and self-resonance frequency (SRF) [7]. Furthermore, unlike CMOS inductors, which are confined to planar structures, MEMS inductor offers various geometrical structures, such as planar inductor [8, 9] solenoid inductor [10], 3D inductors [11], and vertical inductors [12]. However, these inductors involve complex and high cost fabrication process, which undermines their performance advantage.

Silicon-on-insulator (SOI) process technology has advantages over CMOS process because of the better isolation between consecutive layers, low parasitics, better RF performance, and higher operation temperature [13]. Furthermore, the commonly used silicon dioxide layer acts as a sacrificial layer for suspending MEMS component and can act as an etch stop for bulk micromachining techniques. Thus, the SOI process is good for transistors as well as MEMS passive devices fabrication [14].

Commercially available SOI-MUMPs process is a cost effective MEMS fabrication for industry, universities and governments worldwide [15]. This process has been widely used for optimizing MEMS based navigational sensors, such as accelerometer [16] and gyroscope [17], MEMS based resonators for filtering [18], oscillators [19], micro mirrors [20], and microgrippers [21]. So far the process utility for optimizing of MEMS based inductors has not been investigated thoroughly. Inductors, besides their application in RF systems, also help in the effective excitation of micro and nano resonators and their higher order modes [22]. Therefore, it is essential that inductors and MEMS/NEMS resonators to be monolithically fabricated on the same wafer for improved performance and compactness.

This paper deals with the characterization and performance comparison of two inductor structures; planar zig-zag and solenoidal in SOI-MUMPs, and the study of temperature variation effects on their performance. As SOI-MUMPs offers only single metal layer for the inductor structure, therefore bonding wire has been used as the second metal layer for realizing the solenoidal shape. It is evident from the results that despite low resistive substrate, the inductor's RF performance is acceptable.

Device Modeling and Fabrication

Fig.1 shows 3D schematics of the planar zig-zag and solenoidal inductors. The silicon layer is the structure layer with a thickness of $25\text{ }\mu\text{m}$ and two separate gold layers are deposited on top of the structure layer having thickness of $0.5\text{ }\mu\text{m}$ and $0.6\text{ }\mu\text{m}$, respectively. Thus, the dc resistance is greatly reduced by adding multiple metal layers. In order to suspend the structure layer, DRIE etching has been performed to reduce the substrate coupling. Thus the resonance frequency f_{res} is increased and Q factor is improved by reducing the substrate loss. For comparison purpose, both type of inductors have same dimensions. For the solenoidal shape inductor, bonding wire has been utilized as a second structural layer as shown in Fig. 1(b). The dimensions of the inductors structures are given in Table 1.

Fig. 1 3D schematics of SOI-MUMPs based inductors; (a) planar zig-zag, (b) solenoidal.

Table1

Parameters	Design values	
	Zig-Zag	Solenoidal
Length of conductor	$650\text{ }\mu\text{m}$	$650\text{ }\mu\text{m}$
Number of turns	6	6
Width of conductors	$100\text{ }\mu\text{m}$	$100\text{ }\mu\text{m}$
Thickness of conductor(silicon/gold)	$25/1.1\text{ }\mu\text{m}$	$25/1.1\text{ }\mu\text{m}$
Diameter of gold wire	$38\text{ }\mu\text{m}$	$38\text{ }\mu\text{m}$
Length of gold wire	—	$1000\text{ }\mu\text{m}$ (approx..)
Size of the device	$2\times 0.7\text{mm}^2$	$2\times 0.7\text{mm}^2$
Air-trench thickness (μm)	$400\text{ }\mu\text{m}$	$400\text{ }\mu\text{m}$

Fig. 2 shows the lumped parameter model of the on-chip inductor. C_p denotes the capacitance between different windings, R_s represents the inductor series resistance, L_s denotes the inductance of the inductor, C_{ox} is the parasitic capacitance between the metal of the spiral and substrate, which is negligible due to the trench underneath the structure layer, R_{si} represents ohmic losses in the substrate by eddy currents induced in the substrate, and C_{si} models the capacitive effect of the substrate.

Fig. 2. Lumped parameter model of an on-chip inductor.

The substrate capacitance C_{si} and resistance R_{si} can be calculated by

$$C_{si} = \frac{WlC_o}{2} \quad (1)$$

$$R_{si} = \frac{2}{WlG_o} \quad (2)$$

where W is width and l is the length of the inductor, and C_o is the substrate capacitance per unit area. G_o is the substrate conductance per unit area. If conductance per unit area decreases, R_{si} increases and eddy currents in substrate decrease, which increases the Q-factor of the inductor. The AC resistance of the inductor is dependent on the skin effect. The skin depth, δ can be calculated from the below equation

$$\delta = \sqrt{\frac{\rho}{\pi\mu f}} \quad (3)$$

where μ is the magnetic permeability, ρ is the resistivity of the metal, and f is the frequency. It is clear from the equation that the skin depth is inversely proportional to frequency. The AC resistance of the inductor can be calculated as [23]

$$R_{AC}(f) = R_{DC} \frac{t}{2\delta(1 - \exp(-t/2\delta))} \quad (4)$$

where t is the thickness of the gold layer and $R_{DC} = \frac{l}{Wt\sigma}$, l is the length, W is the width, and σ is the conductivity of material. It is evident from the equation that the AC resistance increases with the decrease in skin depth.

The fabrication process of SOI-MUMPs starts with double-sided polished SOI wafer having 400 μm thick carrier substrate, 2 μm oxide layer and 25 μm SOI silicon layer as shown in Fig. 3(a). The silicon layer is doped with phosphosilicate glass (PSG) to dope the phosphorous dopant into the top surface and etched afterwards. A 20 nm chrome and 500 nm gold layers are patterned through a lift off process using pad metal mask layer as shown in Fig. 3(b). Then, the silicon layer is etched down to oxide using same mask layer through DRIE as shown in Fig. 3(c). Then the back side of the carrier silicon substrate is also etched using DRIE and a trench is made beneath the inductor structure. Afterwards, the oxide is removed using wet etching from the trenches and vapor HF process is carried out for etching the remaining oxide as shown in Fig. 3(d). Then, the second metal layer with

50 nm chrome and 600 μm gold is evaporated on the wafer and patterned using shadow mask as shown in Fig. 3(e,f). Finally, in post-processing for solenoidal inductor, bonding wire is used to connect inductor turns with each other. The photograph images of planar zigzag and solenoidal inductor are shown in Fig. 4.

Fig. 3. Step by step fabrication process of SOI-MUMPs inductor.

Fig. 4. Photographs of the SOI-MUMPs based inductors. (a) Planar zig-zag; (b) solenoidal.

To investigate the mechanical robustness of the inductor, its mechanical resonance frequencies are calculated. Since the device might be subjected to environmental vibrations with frequencies less than 1 kHz. It is clear from Fig. 4(a) that the single conductor in the planar zigzag inductor is a clamped-clamped beam. The mechanical resonance frequency is calculated from the following equation:

$$f = \frac{1}{2\pi} \sqrt{\frac{k}{m}} \quad (5)$$

$$k = \frac{32Ewt^3}{l^3} \quad (6)$$

where E is the Young's modulus of the beam, m is the mass, l is the length of clamped-clamped beam. By using the above equation, the resonant frequency of the zig-zag planar inductor is 460.182 kHz and from Finite element simulations it is 464.54 kHz as shown in Fig. 5(a). For the solenoidal inductor, the frequency of the bond wire inductor can be obtained using a finite element simulation of the fixed-fixed loop bonding wire as shown in Fig. 5(b). It is clear from the figure that the resonance frequencies of inductors are far away from 1 kHz.

Fig. 5 Fundamental 1st mode of vibration; (a) planar zig-zag, (b) solenoidal inductor.

Results and Discussions

On-wafer measurements of micro-inductors have been carried out using Cascade Microtech's Summit 12000 AP semi-automatic high-frequency probe station, as shown in Fig. 6. The scattering parameters (S-parameters) were measured using infinity GSG probes of 150 μm pitch along with Rohde and Schwarz ZVB 20 vector network analyzer. Vector network analyzer calibration is very critical for the S-parameter measurements. It is done for correcting imperfection and errors in the path, such as load mismatch, directivity, and frequency response. Therefore open, short, load, and through calibrations have been utilized using the Agilent's on-wafer calibration tool of impedance standard substrate. The S-parameters of the devices were recorded from 60 MHz to 3GHz. The device pad parasitics were de-embedded from the micro-inductor using the procedure reported in [24]. The chuck temperature was varied using Espec temperature controller as shown in Fig. 6.

Fig. 6. Photograph of the experimental setup for characterization of inductors.

Fig. 7. Measured parameters of a planar zig-zag inductor versus frequency at different temperatures; (a) Inductance, (b) quality factor.

Fig. 7(a) shows the inductance of the planar zig-zag inductor. It is clear from the figure that the inductance is almost constant from 100 MHz to 1.5 GHz and decreases slightly with the increase in the frequency. Similarly, the effect of temperature on inductance is very small at low frequency but it is more pronounced at high frequency. The quality factor of the zig-zag inductor is maximum at 480 MHz, which decreases with the increase in frequency due to the increase in AC resistance. Furthermore, the quality factor is decreased with the increase in temperature mainly due to the increase of resistance at high temperatures as shown in Fig. 7(b).

Fig. 8 (a) shows inductance of bond-wire solenoidal inductor. It is observed that the solenoidal inductor has achieved higher inductance as compared to the planar inductor. The inductance is almost constant from 100 MHz to 2 GHz. Also it is noted that the effect of temperature on the inductance is significant at higher frequency. Similarly, solenoidal inductor achieves higher quality factor as compared to the planar inductor. The maximum quality factor of 7.10 is achieved at 478 MHz. The quality factor of the inductor can be improved further if the resistance of the silicon structure layer is decreased or by replacing the low resistive substrate with a high resistive one. The quality factor of the solenoidal inductors decreases sharply with the increase in temperature as shown in Fig. 8(b). This is due to the increase of resistance at higher temperatures.

Fig. 8 Measured parameters of solenoidal inductor versus frequency at different temperatures; (a) inductance, (b) quality factor.

Conclusion

This work has presented a comparison between a planar zig-zag inductor and a bond-wire solenoidal inductor fabricated in SOI-MUMPs standard process. It is concluded that the bond-wire on chip solenoidal inductor achieves better inductance and Q-factor as compared to the planar inductor while keeping the same dimensions of the structure. This technique improves the Q-factor of the inductor; and hence efficient electrical passive component can be realized on the same SOI-MUMPs wafer for interconnection with mechanically active components such as resonators/oscillators for efficient overall performance of the system. Furthermore, the Q-factor of the inductors can be further improved by selecting lower silicon resistance and higher handle layer wafer resistance to improve RF performance further.

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