Growth of *n*-Ga doped ZnO nanowires interconnected with disks over *p*-Si substrate and their heterojunction diode application

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ABSTRACT

In this paper, the heterojunction diode based on *n*-Ga doped ZnO nanowires interconnected with disks/*p*-Si assembly was fabricated and their low-temperature electrical properties were examined. The Ga-doped ZnO nanowires interconnected with disks were grown over *p*-Si substrate and studied by numerous techniques to understand the structural, compositional and morphological characteristics. Electrical properties, at low-temperatures ranging from 77 K–295 K, were examined for the fabricated heterojunction diode assembly both in reverse and forward biased conditions which exhibited an excellent stability over all the temperature range. The detailed electrical characterizations revealed that the current decreases gradually from 1.9 μ A, to 0.87 μ A to 0.84 μ A when temperature increases from 77 K, 100 K to 150 K and then increases gradually from 1.86 μ A–3.36 μ A and to 9.95 μ A when temperature increases from 200 K–250 K and to 295 K, respectively. Both the highest rectifying ratio at 100 K and the lowest one at 295 K occur in the voltage range of 2–5 V.

Keywords: Ga-Doped ZnO, Electrical Properties, Heterojunction Diode.

1. INTRODUCTION

Recently, the nanomaterials, due to their exotic and interesting properties, have broadly used for several important applications in various areas of science and

technology [1–3]. Among various nanomaterials, the semiconductor nanostructures are extensively studied not only in terms of their fundamental properties but also to their applications [4–6]. Because of their shape and size dependent characteristics, semiconductor nanomaterials exhibited stimulating properties and applications in optics, electronics, optoelectronics, biology, environment, etc. [7–9]. The nanostructures of zinc oxide (ZnO),

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a II–VI semiconductor, are among the most important semiconductor nanomaterials as they possess wide-band gap (3.37 eV at room temperature), high-exciton binding energy (60 meV) and visible optical transmittance (above 80%), thermal and chemical stability, non-toxicity, and so on [10–13]. Because of their significant use in electronics, sensors (gas, chemical and bio), optical devices, photocatalysis, energy devices (solar cells, supercapacitors, batteries, hydrogen energy, etc.), bio related applications (antibacterial, cancer detection, cancer therapy), and so on, ZnO is widely studied [14–18]. Owing to numerous applications, various ZnO nanostructures such as nanorods, nanowires, nanofibers, nanodisks, nanoflowers, nanosheets, nanowhiskers, and so forth are synthesized by a number of techniques and reported in the literature [19–23].

Recently, the fabrication and applications of ZnO nanomaterials based electronic devices, especially the heterojunction diodes based on *n*-ZnO/*p*-Si substrate, have attracted tremendous interest due to compatibility of Si substrate to the current generation CMOS technology [24–28]. The properties of the fabricated heterojunction diodes were evaluated at various temperatures [24–28]. Aksoy et al. have fabricated *n*-ZnO/*p*-Si heterojunction diode and examined the effect of ambient temperature on the electrical properties of the device [24]. Sharma et al. studied the electrical characteristics of *n*-ZnO/*p*-Si based heterojunction diode prepared using vacuum coating process [25]. The effect of oxygen plasma treatment on the electrical properties of fabricated *n*-ZnO/*p*-Si heterojunction diode was examined by Kim et al. [26]. Ozmen et al. examined the electrical properties, under dark and light conditions, of heterojunction diode fabricated based on spray derived *n*-ZnO nanostructured/*p*-Si substrate assembly [27]. Singh et al. have examined the high temperature electrical performance of fabricated *p*-Si/*n*-ZnO nanoparticle based heterojunction diode and reported in the literature [28]. To enhance the properties and for specific applications, recently, various doped ZnO nanomaterials were used to fabricate heterojunction diodes. Interestingly, the doping of specific ions into the lattices of ZnO was done in such a specialized manner that ZnO retains its *n*-type conductivity. Recently, *n*-MgZnO thin film was grown over *p*-Si substrate and the assembly was used to fabricate heterojunction diode [29]. To enhance the properties compared to *n*-ZnO/*p*-Si based heterojunction diode, *n*-type Al-doped ZnO film grown over *p*-Si substrate assembly was used to fabricate heterojunction diode which exhibited improved electrical properties [30]. Yttrium (Y) doped ZnO thin film over *p*-Si substrate was deposited by sol–gel process and their electrical properties were examined [31]. It was observed that the Y-doped ZnO based heterojunction diodes exhibited better electrical characteristics because of the availability of more donor electrons and hence cause the Fermi energy level shift to the conduction band [31].

In this paper, we report the facile growth and characterizations of *n*-Ga-doped ZnO nanowires interconnected with disks/*p*-Si assembly. The prepared assembly was further used to fabricate *p*–*n* heterojunction diode and their electrical properties were examined at low-temperature in the range of 77 K–295 K both in reverse and forward biased conditions.

2. EXPERIMENTAL DETAILS

n-Ga doped ZnO nanowires interconnected with disks were grown over *p*-Si substrate via thermal evaporation of metallic zinc and gallium powder in presence of oxygen gas. The evaporation process was performed in a horizontal tube furnace consists of halogen heating system with rapid heating rate of 10–15 °C/s. The used silicon substrate was thoroughly cleaned before the deposition process. For the growth of Ga-doped ZnO over *p*-Silicon substrate, appropriate ratio of metallic zinc (Zn) (1 g) and gallium (Ga) powders (0.1 g) were mixed and grinded well using mortar and pestle and placed in a small alumina boat which was placed in the middle of the quartz tube. Consequently, several small pieces (1.5 × 1.5 cm²) of *p*-Si substrates were placed adjacent to the boat. After such a specific arrangement, the pressure of quartz tube was down to 2–4 torr using rotary vacuum pump. After attaining the required pressure, the furnace temperature was increased to 700 °C under the constant flow of high-purity nitrogen (N₂: 30 sccm) and oxygen (O: 15 sccm) gases. During the reaction, the vapors of mixed metallic powder were oxidized in presence of oxygen gas and transported with the help of nitrogen as gas carrier and deposited over *p*-Si substrates placed adjacent to the alumina boat containing mixed metallic powder. The reaction was lasted for 90 min. After completion of the reaction, the furnace was cooled to room-temperature and the deposited layer of Ga doped ZnO on Si substrates were examined to understand the structural, compositional and morphological properties of the deposited nanomaterial. Finally, the materials deposited on Si substrates were used to fabricate heterojunction diodes and their electrical characteristics were investigated at low-temperature between 77 K and 295 K.

The crystal and compositional characteristics of the deposited material were examined by X-ray diffraction (XRD; PAN analytical Xpert Pro.) and energy dispersive spectroscopy (EDS), respectively. The XRD analysis was done in the 2θ range of 30–75°. The shape and size of the deposited material were investigated by field emission scanning electron microscopy (FESEM; JEOL-JSM-7600F). Electrical properties of the fabricated heterojunction diode were performed at low-temperature range (77 K–295 K), both in reverse and forward biased conditions using silver (Ag) metal as a contact electrode. Gaussian distribution model of barrier heights was used to

analyze the electrical properties of the fabricated hetero-junction assembly.

3. RESULTS AND DISCUSSION

3.1. Characterizations and Properties of *n*-Ga-Doped ZnO Nanowires Interconnected with Disks Over *p*-Si Substrate

The deposited Ga-doped ZnO layer on the silicon substrate was examined by XRD, and the observed result is shown in Figure 1(a). Interestingly, all the observed diffraction peaks are belonging to the wurtzite hexagonal crystal structure of ZnO and could be assigned as ZnO (100), (002), (101), (102), (110), (103), (200), (112), (201) and (001). No other peak related to Ga or based oxides are seen in the observed pattern which might be due to almost similar atomic radii of Zn (1.38 Å) and Ga (1.41 Å) ions. It is expected that due to almost similar atomic radii, the Ga ions have successfully replaced Zn ions and Ga has been incorporated into the lattices of ZnO without considerable lattice distortion. Further, all the observed diffraction peaks in the pattern are well-defined and possess high intensity, hence one can predict the high-crystallinity for the deposited material over *p*-Si substrate. The elemental composition of the deposited material was investigated by energy dispersive spectroscopy (EDS) and result is shown in Figure 1(b). The observed EDS spectrum exhibited several peaks related to oxygen, zinc and

gallium which reflects that the deposited material is Ga-doped ZnO. No other peaks related to any impurity were detected in the observed EDS spectrum which further confirmed the high purity of the deposited Ga-doped ZnO material over Si substrate.

The general morphologies of the Ga-doped ZnO material over Si substrate were examined by FESEM and results are shown in Figures 1(c) and (d). Figures 1(c) and (d) depicts the typical FESEM images which clearly confirmed that the deposited material is composed of nanowires attached with the disks shaped morphologies. The nanowires are originated from the upper surfaces of the disks and hence can be termed as “nanowires interconnected with disks.” The structure is uniformly grown over the substrate surface. The typical diameters of the nanowires are in the range of 120 ± 30 nm while lengths are from 1–3 μm . The dimensions of the disks are in the range of 250 ± 50 nm.

3.2. Low-Temperature *I*–*V* Characteristics of *n*-Ga-Doped ZnO/*p*-Si Substrate Heterojunction Assembly

Figure 2 shows the low-temperature range (77–295) of the *I*–*V* characteristics of the fabricated *p*–*n* junction. In this range of temperatures, the turn-on voltage is ~ 0.2 V. The current decreases gradually from 1.9 μA , to 0.87 μA to 0.84 μA when temperature increases from 77 K, 100 K to 150 K and then increases gradually

Fig. 1. Typical (a) XRD pattern, (b) EDS spectrum and (c and d) FESEM images of Ga-doped ZnO nanowires interconnected with disks over Si substrate.

Fig. 2. Typical I - V characteristics of the fabricated heterojunction diode assembly based on n -Ga-doped ZnO/ p -Si substrate in the low-temperature range of 77 K–295 K.

from $1.86 \mu\text{A}$ – $3.36 \mu\text{A}$ and to $9.95 \mu\text{A}$ when temperature increases from 200 K–250 K and to 295 K. Both the highest rectifying ratio at 100 K and the lowest one at 295 K occur at voltages of 2–5 V.

3.2.1. Low-Temperature I - V Characteristics of n -Ga-Doped ZnO/ p -Si Substrate Heterojunction Assembly on the Basis of Thermionic Emission Model

On the basis of thermionic emission model, the current across the p - n junction in a heterojunction diode is related to the applied voltage and temperature as follows [32, 33]:

$$I = I_o(T)[e^{(eV/nkT)} - 1] \quad (1)$$

where, $I_o(T)$ is the saturation current which is expressed by

$$I_o(T) = AA^{**}T^2 e^{-(eV_o/nkT)} \quad (2)$$

where A and A^{**} , T , e , V_o , n , k , are contact area, Richardson constant, temperature, electronic charge, barrier height, the quality factor, and Boltzmann constant, respectively. The plot of $\ln(I)$ versus voltage V of forward bias of heterojunction diode, in Figure 3, shows three mechanisms exhibited in three regions. This is found in agreement with other work [34]. The linear dependence of current on the applied voltage, in Region I (with $V < 0.4$ V), indicates that the dominant mechanism is either field emission or tunneling. Here, in this region the values of n are larger than the ideal value of one. Knowing A , A^{**} , and T , one can obtain the saturation current I_o , the barrier height V_o and the quality factor n at different temperatures, from region I of Figure 3. Since V_o and n depends on temperature, any inaccurate evaluation of these quantities is due to inaccurate measurements of temperature.

Fig. 3. Plots of $\ln(I)$ versus forward bias voltage at different low temperatures.

Moreover, exponential dependence of the current on the applied voltage which appeared in region II (with $0.4 < V < 1.8$ V) is attributed to recombination-tunneling mechanism. In region II, the quality factor n exhibits very much higher values than those of region I. Finally, region III (with $V > 1.8$ V) that follows the power law, is due to the mechanism controlled by the space-charge-limited current.

Figure 4 depicts saturation currents I_o and quality factors at different temperatures for the fabricated heterojunction diode obtained from Figure 3. The trend of change of I_o and n is found in agreement with that shown by others [32, 33]. Transparent deviations around the straight line fit are obtained for the quality factor. The increase in the quality factor n is attributed to the decrease in the steepness of the slope of line fit of data in region I. One can also conclude that a corresponding increase in the resistance is also attributed to the decrease in the steepness of the latter slope.

Fig. 4. The low temperature dependency of saturation current I_o and quality factor n from the Ga-doped ZnO nanowires/Si heterojunction diode.

Fig. 5. The plot of $\ln(I_o)$ versus the inverse of temperature. The best line fit provides a value of activation energy of ~ 6.5 meV. The data fluctuates around the best line fit.

An underestimated value of activation energy is found from the best line fit of the data of $\ln(I_o)$ versus the inverse of temperature (Fig. 5). Large deviations around the best line fit are resulted.

The slope of best line fit in Figure 6(a) gives the mean barrier height $V_b = 0.65$ V as a single effective Schottky height. The linear fit also gives the standard deviation $\sigma_s = 0.085$ eV. The employment of the model of Gaussian distribution of barrier heights becomes important when lateral fluctuations exist. This may require the use of the relation between the barrier height V_o and the mean barrier height V_b . This relation is expressed by [35]:

$$V_o = V_b - \frac{e\sigma_s^2}{2kT} \quad (3)$$

Figure 6(b) shows that the barrier height is linearly dependent on the quality factor for different temperatures. This also asserts the existence of some lateral inhomogeneities in the barrier height. A homogenous barrier height value of ~ 0.595 eV is obtained when the best line fit of the data is extrapolated to $n = 1$. This barrier height is expected to get extracted from an ideal contact. However, such real contact has inhomogeneities in the barrier height which is resulted from the mismatch in the lattice constant between ZnO and Si at the interface.

3.2.2. The Modified Method of Gaussian Distribution of Barrier Heights

The adoption of this modified method implies the use of the modified Richardson formula [35]:

$$\ln\left(\frac{I_o}{T^2}\right) - \left(\frac{e\sigma_s}{\sqrt{2}kT}\right)^2 = \ln(AA^*) - \frac{eV_b}{kT} \quad (4)$$

This formula provides a better single effective Schottky barrier height, V_b , which represents the distribution of

Fig. 6. (a) Plot of barrier heights extracted from I - V analysis versus the inverse of temperature. The values of $V_b = 0.65$ eV and $\sigma_s = 0.085$ eV as extracted from the linear fit (line); (b) barrier heights V_o plotted versus quality factor n . The value of homogenous barrier height of ~ 0.595 eV is obtained when the line fit is extrapolated to $n = 1$.

low Schottky barrier heights patches. When Eq. (4) is employed, Richardson plot, in Figure 7, gives value of mean barrier height of ~ 0.71 eV which is consistent with the value of ~ 0.65 eV obtained using Eq. (3) as long as the uncertainty $\sigma_s = 0.085$ eV is concerned. These two values are also close to the energy difference (~ 0.72 eV) of the work function between Si and ZnO; the Fermi level below the vacuum level is 4.97 eV for *p*-Si and 4.25 eV for ZnO.

3.3. Low-Temperature C - V Characteristics of *n*-Ga-Doped ZnO/*p*-Si Substrate Heterojunction Assembly

The value of effective height of the Schottky barrier can be extracted from the analysis of C - V measurements. Such measurements are conducted when small AC voltage with frequency of 1 MHz is superimposed on the DC bias across the Schottky contact. A depletion layer is formed

Fig. 7. The modified Richardson plot for the *n*-Ga-doped ZnO nanowires/*p*-Si heterojunction diode, using Eq. (4). The value of mean barrier height of 0.71 eV is extracted from Richardson plot.

when the diode is in the reverse bias condition, where opposite charges are developed on the metal surface of the contact and in the semiconductor material. The capacitance C of depletion layer is related to the reverse bias voltage V_r and is expressed by:

$$\frac{e\epsilon_{Si}\epsilon_0 A^2}{2C^2} = \frac{V_b^{C-V} - V_r}{N_D} \quad (5)$$

Here, N_D , V_b , A , ϵ_0 , ϵ_{Si} , and e are concentration of carriers in the depletion region, the barrier height, the contact area of the junction, the permittivity of free space, the static dielectric constant of Si, and electronic charge, respectively. When both the reverse bias voltage and the temperature increase, the capacitance decreases in C - V measurements. Figure 8 shows a linear behavior when the inverse of square of capacitance is plotted versus reverse bias voltage for different temperatures. However, some deviations occur around the best line fit at high reverse bias voltages. The values of barrier height obtained from analysis of C - V measurements ($=3.93$ eV and 3.4 eV) due to respective change in temperature between 77 K and 295 K, are less than the corresponding values obtained from I - V analysis.

The results observed here asserts that the interface states cannot follow the AC signal and cannot considerably contribute to the capacitance of the device. This may lead to the conclusion that, at this low frequency of 1 MHz, it is extremely difficult to observe an abrupt heterojunction. This consequently leads to the conclusion that the interface states which are responsible for the trapping of charges may cause a non-ideal behavior of C - V characterization [36]. The value of barrier height obtained from I - V analysis of $V_b^{I-V} = 0.71$ eV with a standard deviation of $\sigma_s = 0.085$ eV is in agreement with the energy difference (0.72 eV) of the work function between Si and ZnO. Here, the analysis of V_b^{I-V} with varying temperature

Fig. 8. The values of C^{-2} plotted versus reverse bias voltage V_r at different temperatures.

is based on the assumption of using Gaussian distribution of barrier heights which provide us with the estimated value of σ_s . However, C - V analysis does not exhibit any sensitivity to the latter estimated value of σ_s . The possible band bending which occurs in a semiconductor may lead to inaccurate values of barrier height, V_b^{C-V} . As long as a close insight into the band bending effect is not available, we cannot count on the obtained values of barrier height, V_b^{C-V} unless this matter is completely resolved because these values depend on the mean band bending of the prepared semiconductor.

The equation $V_b^{C-V} = -\alpha T + V_b^{C-V}(T = 0 \text{ K})$, can be taken into consideration, as an approximation, to test the linear dependence of barrier height V_b^{C-V} on temperature. Here, $V_b^{C-V}(T = 0 \text{ K})$ is the barrier height when extrapolated to absolute zero temperature and α is the temperature coefficient. This latter equation may be used to fit the measured values of V_b^{C-V} . The linear fit to measured values of V_b^{C-V} is shown in Figure 9. The values of V_b^{C-V}

Fig. 9. The barrier height V_b^{C-V} in eV obtained from C - V measurements is plotted versus temperature.

Fig. 10. The values of $V_b^{C-V} - V_b^{I-V}$ are plotted versus the inverse of temperature.

($T = 0$ K) = 4.27 eV and $\alpha = 0.0053$, are obtained. In an alternative approach, the assumption can be made that the difference between the barrier heights obtained from *C*-*V* data and those obtained from *I*-*V* data (i.e., $V_b^{C-V} - V_b^{I-V}$) may be also used to estimate both α and σ_s . One can write [34]:

$$V_b^{C-V} - V_b^{I-V} = \frac{e\sigma_s}{2kT} + \frac{e\alpha}{2k} \quad (6)$$

Figure 10 depicts the observed values of $V_b^{C-V} - V_b^{I-V}$ versus the inverse of temperature. From the linear fit, the values of $\alpha = 0.00044$ eV K⁻¹ and $\sigma_s = 0.018$ eV are extracted. Inappropriately, the values of both α and σ_s do not agree with those obtained in our earlier analysis. This departure means that above adopted assumption is not satisfactory in producing closer results to those obtained earlier for the low temperature range considered in the present work.

4. CONCLUSIONS

In summary, high-density growth of *n*-Ga-doped ZnO nanowires interconnected with disks over on *p*-Si substrate were performed by the thermal evaporation of metallic zinc and gallium powder in presence of oxygen. The grown nanostructures over Si were studied by numerous techniques to understand the structural, compositional and morphological characteristics. To examine the electrical properties, a heterojunction diode based on *n*-Ga-doped ZnO nanowires interconnected with disks/*p*-Si substrate assembly was fabricated and examined at low-temperature ranging from 77 K–295 K, both in reverse and forward bias conditions. The detailed electrical characterizations revealed that the current decreases gradually once the temperature increase upto 150 K and then increases gradually when the temperature increases from 200 K–250 K and to 295 K, respectively.

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