High Performance WSe₂ Transistors with Multilayer Graphene Source/Drain

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Abstract

P-channel WSe₂ FETs along with multilayer graphene source/drain (S/D) are demonstrated by the CVD growth of the WSe₂ monolayer to the patterned graphene. Multilayer graphene (MLG) is adopted to reduce contact resistance while the monolayer WSe₂ served as the channel for the electrostatics integrity of the FET. Furthermore, by increasing the *p*-type doping concentration of the graphene S/D, the I_{on}/I_{off} ratio can be enhanced to 10⁸ and the unipolar *p*-channel characteristics are retained regardless the choice of the work function of the metal used for the S/D contact.

Key words: Graphene, WSe₂, raised source/drain

Introduction

Two-dimensional materials have been recognized as atomically-thin semiconductors which are promising for future electronics. The conventional bulk (3D) metal contact to 2D materials severely hinders the scaling roadmap of 2D nanotechnology due to the large transistor size and large schottky barrier between metal and 2D semiconductor. Graphene is believed to be one of the most suitable source/drain material owing to its semimetal nature and its workfunction can be easily modulated. Recently, several groups have explored lateral graphene-MoS₂ [1-3] and graphene-WSe₂ [1, 4] heterostructures using CVD synthesis, where the graphene provide a low intrinsic device size along with a low contact resistance. To date, all the field-effect transistors (FETs) based on those reported graphene-TMD heterostructures are all *n*-type channel. Therefore, to realize a CMOS-compatible technology, it is highly desirable to construct the lateral heterostructures based on a *p*-type material such as WSe₂. Furthermore, we use multilayer graphene to serve as RSD and impose doping engineering to further improve the performance of *p*-type WSe₂ transistor.

Formation of multilayer graphene RSD

The large-area Multilayer graphene (MLG) was grown on a Cu foil using CVD technique, the CH₄ provide the carbon source and Ar and H₂ serve as carrier gas as illustrated in **Fig. 1a** [5, 6]. To obtain the MLG, the growth time should be extended than the single layer graphene. In **Fig. 2a**, the MLG then transferred onto sapphire substrates by wet transfer

method.[7] After patterning, MLG films occupy the two sides and the sapphire is exposed in the center region. Then the patterned sample is placed into another CVD furnace for the WSe₂ growth as illustrated in **Fig. 1b** using WO₃ and Se power as precursor. The WSe₂ selectively fills the center and there is no visible gap at MLG-WSe₂ junction in **Fig. 2b**. The raman mapping of MLG in **Fig. 2c** indicates the coverage region of MLG; the mapping of WSe₂ signal in **Fig. 2d** shows that the WSe₂ only grows in the center region which proves that WSe₂ is not grown on the top of the graphene layers. The Raman peak of MLG in **Fig. 2e** having 2D/G ratio (< 1) corroborates that the as-patterned graphene is multilayered.[8, 9] An obvious and broad D band emerges after WSe₂ growth (curve ii) is attributed to amorphous carbon transformed from photoresists residue after high temperature annealing.[4] PL and Raman (**Fig. 2f** and **Fig. 2g**) suggest that the WSe₂ is a monolayer. Consequently, we obtain atomically thin WSe₂ channel with thickened source/drain region with MLG which is the proposed 2D version raised source/drain (RSD) design for the transistor.

Physical Feature of the RSD-channel junction

High-resolution transmission electron microscopy (HRTEM) at MLG-WSe₂ junctions in **Fig. 3a** shows that the MLG in the RSD region is 3.7 nm thick (ten graphene layers). Few-layered WSe₂ is found at the patterned MLG edge, and WSe₂ growth is more likely to penetrate into the space between MLG and sapphire substrate, forming a thicker overlapped junction as shown in **Fig. 3b**. In **Fig. 3c**, the layer number of WSe₂ gradually reduces from few-layers at the junction to a monolayer when the location is away from the junction. Note that the CVD condition used here is optimized for monolayer WSe₂ growth on a blank sapphire substrate. The WSe₂ at the channel region exhibits a thickness of 0.62 nm corresponding to a monolayer as shown in **Fig. 3d**. The MLG-WSe₂ heterostructure and the RSD reduce the parasitic series resistance, while in the channel region the monolayer WSe₂ serves as the ultra-thin channel under excellent gate control.

Transistor performance

Top-gate transistors are fabricated by the process flow shown in **Fig. 4**. Single layer (SLG) graphene and *p*-doped small grain size MLG (sMLG) devices are also separately prepared for comparison shown in **Fig. 5a** by controlling the

graphene CVD condition. The WSe₂ CVD condition is identical for all kinds of graphene S/D. Both G and 2D Raman peaks of sMLG blue shift in **Fig. 5b** curve ii indicates the sMLG is *p*-doped. [10] It is likely due to unintentional oxidation taking place along the grain boundaries or defect sites (**Fig. 5c**) during WSe₂ CVD. The *p*-doping in sMLG remains stable even after 300 °C annealing in ambient air, as proved by the unchanged Raman features (**Fig. 5b** curve iii). The transfer curves all exhibit p-type transport in **Fig. 5d** and *p*-doped sMLG shows the best performance with I_{on}/I_{off} ratio exceeds 10⁷. The on-current of MLG S/D is ten times larger than SLG S/D due to the RSD benefit. The hole barrier is further reduced at sMLG-WSe₂ junction as the *p*-doping effect taking places at the sMLG, the band diagrams for the *p*-doped sMLG-WSe₂ junction are proposed in **Fig. 5e**. The performance of *p*-sMLG RSD is significantly enhanced for more than 1000X. The contact resistances R_{sd} , mobility μ_0 and threshold voltage V_t are extracted by Y-function method (YFM) [11] and listed in **Table1**. The contact resistance in our study mainly raises from the graphene-WSe₂ junction, we can see the R_{sd} for *p*-sMLG is obviously reduced. Moreover, unipolar p-type FET is always obtained even using a low work function metal Ti in **Fig. 6a**, since the barrier at WSe₂-graphene junction is responsible for the preference of injection carrier type. The electrical results for the reported CVD based monolayer WSe₂ transistors are summarized in **Fig. 6b** for better comparison.

Conclusion

In summary, we use monolayer WSe₂ as a channel material to achieve *p*-type transistor with MLG RSD. By imposing *p*-doping, the unipolar on-current is improved by more than 1000 times with the I_{on}/I_{off} ratio exceeding 10⁷ for the *p*-sMLG RSD. This device may pave the way for the realization of the sub 5nm technology by using atomically thin channel.

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Fig. 1 Schematic illustration for the growth of (a) graphene, and (b) WSe₂ in CVD hot-wall furnaces.

Fig. 2 Top view OM for (a) as-patterned MLG (b) after WSe₂ CVD growth respectively. Raman mappings of (c) graphene G band and (d) WSe₂ E' band respectively. (e) graphene raman before and after WSe₂ CVD. (f-g) Single point PL and Raman of WSe₂ respectively. The scale bars are 5 μ m.

Fig. 3 The cross-sectional high-resolution TEM images of (a) the MLG region. (b) The overlapped MLG-WSe₂ heterojunction region. (c) The WSe₂ few layers near the junction transit to a monolayer once the location is away from the junction. (d) The monolayer WSe₂ channel region. The scale bars are 5 nm.

Fig. 5 (a) Transistor geometry of SLG-, MLG- and *p*-doped sMLG. (b) sMLG Raman: i, as-patterned; ii, after WSe₂ CVD; iii, after annealing (c) Doping effect takes place at defect sites or the grain boundaries. (d) The transfer curves of the transistors (e) Qualitative band diagram for *p*-doped sMLG-WSe₂ junction.

Fig. 4 Fabrication processes for a top-gated transistor.

TABLE I

Transistor parameter extracted by YFM. The field-effect mobility (μ_{eff}) is listed for reference.

Device	V_t (V)	R_{sd} (ohm- μm)	μ_{eff} (cm ² /V·s)	μ_o (cm ² /V·s)
SLG	-1.14	2.4×10^8	3.2×10^{-3}	3.9×10^{-3}
MLG	-1.14	1.5×10^7	3.6×10^{-2}	3.9×10^{-2}
<i>p</i> -sMLG	-0.73	4.9×10^4	58.4	83.9

Fig. 6 (a) The transfer curve sMLG contacted by a Ti metal. (b) Summary of the published results for transistors based on CVD grown monolayer WSe₂.