A W-Band EBG backed Double Rhomboid Bowtie-Slot On-chip Antenna

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Abstract—A double-rhomboid bowtie-slot on-chip antenna aided by a back-to-back E-shaped electromagnetic band-gap surface for gain enhancement at W-band is presented. The specific structure of both, the antenna and the EBG surface is being reported for the first time in an on-chip implementation. The antenna is analyzed independently as well as backed by different electromagnetic band-gap reflective surfaces using standard 0.13 μm BiCMOS process. The proposed EBG surface provides a measured gain enhancement of 2 dB and 8 dB when used as a frequency selective surface and as an artificial magnetic conductor, respectively. With an overall chip-size of $1 \times 1 \text{ mm}^2$, the on-chip antenna demonstrates a -6 dB impedance bandwidth from 75-100 GHz and an effective gain bandwidth from 80-90 GHz with a peak measured gain of -0.58 dBi at 84 GHz. The antenna has the smallest reported size and the highest gain in W-Band with artificial magnetic conductor as reflective surface.

Index Terms—Artificial magnetic conductor, electromagnetic band-gap, frequency selective surface, gain, on-chip antenna.

I. INTRODUCTION

In recent years, research in W-band (75-110 GHz) has increased considerably due to its applications in mm-wave imaging, automotive radars, non-lethal weaponry, satellite communication and biomedical fields. Smaller wavelengths between 2.7-4.0 mm in W-Band make it particularly suitable for antenna's on-chip implementation, thus enabling potential integration of wireless subsystems on a single chip, resulting into highly miniaturized and compact systems [1].

On-chip antennas (OCA) suffer from low gains and poor radiation efficiency as silicon substrate is not suitable for antenna design due to its high dielectric constant ($\epsilon_r=11.9$) and low resistivity ($\rho \leq 50 \Omega\text{cm}$). The former accounts for wave confinement inside the substrate and reduces radiation into the air due to which the bore-sight gains are very low, typically below -10 dBi. On the other hand, low resistivity causes increased losses inside the substrate deteriorating the radiation efficiency. To enhance the gain of OCA, several techniques have been reported. In [2], a slotted dipole antenna with a gain of -2 dBi is reported whose gain is enhanced by creating a cavity beneath the antenna in silicon dioxide layer. Similarly, in [3], a strip dipole antenna with lumped inductive-capacitive (LC) balun is presented where silicon is removed from beneath the antenna and gain is increased to 4.7 dBi

at 85 GHz. Furthermore, in [4], a Vivaldi and a monopole antenna at 130 GHz are presented in which a cavity is made in the silicon layer of the CMOS chip for improving the gain. Although above works improve the antenna gains; however, adding dielectric layers above the antenna and making cavities in silicon or silicon dioxide layers are customized fabrication steps, not offered in standard CMOS processes which not only increases the complexity of fabrication process but also increases the overall cost of the system.

Use of electromagnetic band-gap (EBG) reflective surfaces is also a popular technique for gain enhancement of OCAs. EBG surfaces are metalo-dielectric arrays of periodic structures to denote artificially realized materials with unusual transmission and reflection characteristics in a particular band of frequencies. The subset terminologies of this broader connotation include: high impedance surfaces (HIS), frequency selective surfaces (FSS), artificial magnetic conductors (AMC), Negative refractive index (NRI) materials etc. In [5], an AMC backed dipole OCA is presented in which ground plane of AMC is at M1 which is the lowest metal layer in a standard CMOS process. This approach isolates the digital circuitry of the chip completely from antenna radiation; thereby increasing the gain and minimizing the EMC issues. The gain of antenna is -1.4 dBi at 94 GHz with a 40 μm thick silicon dioxide in a back-end of line (BEOL) process. Notwithstanding, in a standard CMOS process only up-to 15 μm space is available for all metal layers which is too less for AMC operation to converge in mm-wave band. In [6], a triangular monopole antenna backed by a partially reflected surface at M1 and a PEC layer beneath the silicon layer, is presented with 0.12 dBi gain at 60 GHz and a radiation efficiency of 41%. Similarly, in [7], a circularly polarized, circular loop antenna backed by a star shaped AMC with a gain of -4.4 dBi at 60 GHz is presented. Metallic ground of AMC stack-up is placed beneath the silicon substrate and array of star shaped periodic structures is present at M1, while OCA is at the top-metal layer. Other similar works are presented in [8],[9].

In this paper, through a combination of bowtie and rhombus shaped antennas, a novel double-rhomboid bowtie (DRBT) slot antenna is proposed. Furthermore, a back-to-back E-shaped (B2BE) slot AMC is designed, taking the advantage of high reflection coefficient of E-shaped high impedance surface (HIS). Implemented in a 0.13 μm standard BiCMOS process, an array of 12×12 AMC elements are included in a $1 \times 1 \text{ mm}^2$ chip area providing gain enhancement in the W-band.

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II. AMC THEORY & DESIGN

According to duality theorem, perfect magnetic conductor (PMC) behaves as a dual of a perfect electric conductor (PEC). Unlike a PEC, PMC does not introduce a 180 degrees phase-shift to incident electric field, the property which has useful applications in making reflective surfaces for low profile antennas. PMCs are non-existent in nature and whose behavior can only be artificially realized. Originally proposed by Sievenpiper [10], AMCs are metallo-periodic arrays printed on grounded dielectric substrates. Unlike PECs, tangential electric field exists at the surface of an AMC which makes its surface impedance very high. Mathematically, surface Impedance of an AMC is given by: $Z_s = j\omega/(1 - \omega^2 LC)$ which shows that at resonance frequency, LC constant being reciprocal of ω^2 results in the surface impedance (Z_s) approaching infinity. Therefore, an AMC is also called high impedance surface (HIS) which introduces 0° phase difference to the phase of incident wave at resonance frequency. Thus, incident wave reflects back and constructively interferes with a radiating surface in a close vicinity ($\leq 15 \mu\text{m}$). Another terminology FSS, is also used for a surface which carries out this operation; however FSS are metallic array structures usually fabricated on a substrate only for support and unlike AMC, FSS does not have a ground plane below the substrate [11]. Consequently, AMC is a stack of FSS, dielectric substrate, and ground plane. In a broader connotation, all these meta-material surfaces can be called electromagnetic band-gap (EBG) surfaces. A typical simulation model of an EBG structure in a standard CMOS technology chip is shown in Fig. 1. A Wave port is placed at the position of top metal layer and the FSS structure is placed at the lowest metal layer. Usually, there are 4-5 metal layers in between the top and lowest metal layer, all embedded in silicon dioxide substrate of thickness 10-15 μm . The silicon dioxide substrate is above a silicon wafer whose thickness lies between 200-700 μm . A ground plane beneath the silicon wafer can be added in a post processing step with help of metal sputtering or similar techniques.

Fig. 1. Simulation model of an EBG surface in a silicon chip

In case of OCAs, AMC periodic array is mostly placed beneath the antenna to prevent the wave from entering into lossy silicon substrate, thus resulting into better gain & radiation efficiency. Higher magnitude of reflection coefficient (S_{11}) is desirable as it shows that little energy is transmitted beyond AMC. Furthermore, its operational phase bandwidth,

Fig. 2. Dimensions of DB, JC & B2BE AMC unit cells

in which constructive interference between an incident and reflected wave occurs, is from $+90^\circ$ to -90° .

The design is started by analysis of three AMC unit-cells. First, a Dog-bone (DB) AMC structure at lowest metal layer M1 is designed at 94 GHz. Then, a Jerusalem cross (JC) AMC unit cell is designed which can be seen as two DBs rotated at 90° with respect to each other. Finally, a B2BE AMC unit cell is designed which can be seen as three parallel DBs as shown in Fig. 2. The results in Fig. 3 show that B2BE structure has a ultra-wide phase bandwidth from 75-125 GHz and high reflection coefficient (≥ -0.05 dB) over the whole bandwidth.

Fig. 3. S_{11} phase and magnitude of DB, JC & B2BE AMC unit cells

Next, an analogous B2BE slot type AMC is designed with 3 μm thick ground plane beneath the silicon in order to couple a slot type antenna. The unit cell has S_{11} phase bandwidth from 26-168 GHz and S_{11} magnitude higher than -0.1 dB over the whole band. S_{11} phase and magnitude plot along with the unit cell dimensions is shown in Fig. 4. This B2BE slot AMC unit cell is later used to create periodic array of AMC.

Fig. 4. B2BE slot type AMC unit cell dimensions and characteristics

III. ANTENNA DESIGN

To start with, a simple bowtie slot antenna is designed at 94 GHz using the top layer (TM-2) of the BiCMOS process. A coplanar waveguide (CPW) is used for feeding purpose where the signal traces are shorted with lateral grounds in order to radiate the slot. An overall $1 \times 1 \text{ mm}^2$ chip area is maintained to include the effect of complete chip. Furthermore, a circular bondpad is included with a $125 \mu\text{m}$ pitch for on-wafer characterization. As the bond-pads introduce parasitic capacitance, an open circuit shunt stub is added to cancel the capacitive effect. As a next step, the shape of triangular slot is converted into rhomboid slot to introduce more cornered ends for better slot radiation and further extended to a double rhomboid slot for improved radiation characteristics. The dimensions of Simple Bowtie (SBT), Rhomboid Bowtie (RBT), and Double Rhomboid Bowtie (DRBT) slot antennas are shown in Fig. 5 whereas gain and S_{11} of all three antennas is shown in Fig. 6 which depicts that at 90 GHz, DRBT slot antenna has a gain of -2.31 dBi while RBT antenna has -2.47 dBi and SBT antenna has -2.55 dBi gain.

Fig. 5. Dimensions of SBT, RBT & DRBT slot antennas

Fig. 6. Simulated S_{11} and boresight Gain of SBT, RBT & DRBT slot antennas

Subsequently, the DRBT slot antenna that shows the highest gain is integrated with 12×12 B2BE slot AMC array along with some optimization in its structure for better matching. Simulation model, dimensions and fabricated OCA are shown in Fig. 7. The over-all antenna size is $988 \times 720 \mu\text{m}^2$ and thickness of Silicon is $200 \mu\text{m}$ as offered by the foundry. Dimensions of DRBT slot antenna are given in Table. I.

In order to get further insight, the gain of DRBT slot OCA backed by PMC, AMC, PEC (at M1), FSS and standalone antenna is compared in Fig. 8. In comparison to the standalone antenna, the gain boost achieved by backing the antenna by AMC and FSS is 10dB and 5dB respectively at 98 GHz.

Fig. 7. DRBT slot antenna with 12×12 B2BE slot AMC array and chip microphotograph

TABLE I
DIMENSIONS OF DRBT SLOT OCA WITH 12×12 B2BE SLOT AMC ARRAY

Description	Variable	Value (μm)
Length of bowtie slot	bl	464
Slot spacing from left/right	px	30
Slot spacing from top	py	180
Width of bowtie slot	bw	232
Slot Spacing from bottom	pz	308
length of feedline	fl	317
Width of feedline	fw	1.65
Diameter of circular pad	padl	78
Gap bw Circular pad & side ground	fg	51
Gap bw feedline & side ground	slw	50

Fig. 8. Simulated gain curves with PMC, AMC, PEC & FSS reflective surfaces compared to standalone antenna

IV. FABRICATION AND MEASUREMENTS

The antenna is fabricated in an IHP 7-layer 130 nm BiCMOS technology. In order to satisfy foundry DRC rules, dummy metalization is added for the unused M2-TM1 layers. Although, these layers are kept away from the radiating element, still about 18 % change in simulated results is observed (Fig. 11). This approach emulates the real scenario of having analog circuitry nearby unlike other reported works in which the middle layers are left un-utilized. For on-chip characterization, Orbit's 110 GHz chamber is utilized and the calibration is performed using a direct connection of the transmitter to the receiver of the probe station using a transmission line and a $125 \mu\text{m}$ pitch Cascade Microtech GSG

probe (Fig. 9). Next, a known on-chip antenna (SGCA-60-U-E by MVG-Orbit FR) is measured as a standard antenna for micro-probe antenna measurements, followed by placing the on-chip antenna and measuring its relative parameters. The chip is placed on one of the vacuum holes of the probe-station metal-chuck, the latter acting as ground for the chip. Antenna under test (AUT) is kept stationary and the reference antenna is moved in azimuth and elevation planes for recording the radiation pattern. The inset of Fig. 9 shows photograph of the probes landing on the OCA as well as dummy metallization layer patterns.

Fig. 9. OCA measurement setup with inset dummy metal layer & AUT

Measured and simulated S_{11} are compared in Fig. 10. The measured impedance bandwidth with -6 dB threshold is from 75-100 GHz and the same in simulation is from 82-96 GHz. Although the trend is similar, the difference is expected due to glass slab attached to the chip, changing the effective dielectric constant of the substrate. Similarly, the metal-chuck acting as a ground instead of deposited ground plane beneath the silicon also causes some variations.

Fig. 10. S_{11} of On-chip antenna

The gain of the OCA for both FSS and AMC case is shown in Fig. 11 and depicts a 1 dB difference between simulated and measured curves. The effective measured gain bandwidth (≥ -1.5 dBi) is from 80-90 GHz with a peak measured gain with AMC is recorded at 84 GHz. Radiation pattern comparison of measured and simulated results for gain vs. elevation angle is done at the peak frequency (84 GHz) for FSS and AMC cases as shown in Fig. 12. Calibration and de-embedding is done to compensate for the probe and cable loss. Measured boresight gain of OCA is -6.4 dBi and -0.58 dBi with respect to

Fig. 11. Measured and Simulated Gain vs. Frequency graph

FSS and AMC respectively with 2 dB and 8 dB FSS and AMC gain improvement respectively. The 2 dB reduction in gain improvement in comparison to Fig. 8 is attributed to dummy metallization layers and possible measurement uncertainty.

Fig. 12. Radiation Pattern ($\Phi=0$ deg) of OCA with FSS and AMC

DRBT slot OCA with B2BE slot AMC is compared with other state-of-the-art OCAs backed by AMCs in Table II. Benchmarks used are frequency range, size, peak bore-sight gain and AMC gain. It can be seen that the gain is higher with smaller foot-print as compared to [5],[7]. More specifically, boresight gain is 3.8 dB higher and relative size is half in one dimension and quarter in other dimension in comparison to [7]. Similarly, gain of current work is 0.8 dB higher with considerably smaller area than [5].

TABLE II
COMPARISON WITH STATE OF THE ART WORK

Reference	Freq (GHz)	Size	Gain	AMC Gain Improvement	Process
[5]	90-100	$0.63\lambda \times 0.63\lambda$	-1.4 dBi	8 dB	BEOL
[6]	54-69	$0.16\lambda \times 0.16\lambda$	1.4 dBi	2.2 dB	BiCMOS
[7]	57-67	$0.36\lambda \times 0.36\lambda$	-4.4 dBi	5 dB	BiCMOS
This work	80-90	$0.3\lambda \times 0.1\lambda$	-0.58 dBi	8 dB	BiCMOS

V. CONCLUSION

A double-rhomboid bowtie-slot on-chip antenna backed by 12×12 B2BE slot AMC array is presented. A comparison of various reflection surfaces used in combination with the on-chip antenna reveals AMC outperforming the other types. The measured peak gain of antenna is -0.58 dBi at 84 GHz with AMC and it is -6.4 dBi with FSS whereas the effective gain bandwidth is from 80-90 GHz. The presented design can be extended in form of array of rhomboid bowtie-slot antennas along with parasitic elements to get wide and multi-band response.

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