Nano-islands Based Charge Trapping Memory: A Scalability Study

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Abstract—Zinc-oxide (ZnO) and zirconia (ZrO₂) metal oxides have been studied extensively in the past few decades with several potential applications including memory devices. In this work, a scalability study, based on the ITRS roadmap, is conducted on memory devices with ZnO and ZrO₂ nano-islands charge trapping layer. Both nano-islands are deposited using atomic layer deposition (ALD), however, the different sizes, distribution and properties of the materials result in different memory performance. The results show that at the 32-nm node charge trapping memory with 127 ZrO₂ nano-islands can provide a 9.4 V memory window. However, with ZnO only 31 nano-islands can provide a window of 2.5 V. The results indicate that ZrO₂ nano-islands are more promising than ZnO in scaled down devices due to their higher density, higher-k, and absence of quantum confinement effects.

Index Terms—Charge trapping memory, atomic layer deposition, nano-islands, ZnO, ZrO₂, scalability

I. INTRODUCTION

PORTABLE electronic gadgets have been noticeable part of our daily lives since the 1990s; and the majority of these products use embedded flash memory devices. In 1967, Sze and Kahng invented the floating gate memory at Bell Labs which established the primary technology for flash memory cells [1]. In order to meet the demands of system miniaturization, the dimensional scaling of memories has evolved to increase the density of the memory devices and simultaneously improve their switching speeds. However, with aggressive scaling, the floating gate memory is expected to reach physical limitations. This is especially true with scaled tunnel oxides which can easily leak out all the stored charge in the conductive floating gate through a single leakage path, resulting in a severe reliability issue [2].

Discrete nanoparticles based memory was first invented at IBM in 1995 [3-4], and researchers were considering it to have the potential to solve the scaling problem by the early 2000s. ZnO [5-6] and ZrO₂ [7-8] have shown great potential in several applications including memory devices. In this paper, a scalability study is conducted on ZnO and ZrO₂ nano-islands

Figure 1. a. 2D AFM topography of the ZnO nano-islands, b. 3D AFM topography of the nano-islands [9].

based memory devices that have been recently demonstrated by our group [9-10].

II. DEVICE STRUCTURE AND AFM

The fabricated memory devices are based on a metal-oxide-semiconductor capacitor (MOSCap) structure because the capacitor enables the study of program/erase characteristics, along with studies of retention and endurance with reduced complexity of fabrication compared to the transistor. The tunnel oxide and blocking oxide consist of 4-nm and 10-nm Al₂O₃ layers, respectively, with the charge trapping nano-islands embedded in between the two oxides. Two nano-island materials are studied for the charge trapping layer: ZnO and ZrO₂ which are deposited by 20 cycles of the atomic layer deposition (ALD) process. More details about the fabrication of the memory and the growth of the nano-islands are explained in our recent papers [9-10]. Using an atomic force microscope, the distribution and topography of the nano-islands are extracted. Fig 1.a and Fig 1.b show the 2D and 3D images of the ZnO islands, respectively, while Fig. 2.a and Fig. 2.b show the 2D and 3D images of the ZrO₂ islands, respectively. The islands are represented by white circular/elliptical shapes in the 2D AFM images. In addition, transmission electron microscope is used to show a cross section of the ZrO₂ nano-islands (Fig. 3).

The images show that the ZnO nano-islands have a width range from 8.5-30 nm (average ~20 nm) and an average thickness of ~3 nm. The average coverage of the nano-islands

Figure 2. a. 2D AFM topography of the ZrO₂ nano-islands, b. 3D AFM topography of the nano-islands. Reused with permission from [10].

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Figure 3. TEM cross section of the ZrO₂ nano-islands

is 1/5. With ZrO₂, the average width of the islands is 10-nm with a thickness range of 4-12 nm (average ~8 nm). The coverage of the nano-islands in this case consists of 1/3 of the substrate. The exceptional feature of this growth is the shape of the nano-islands which exposes the largest cross-section (depicted in Fig. 3 with “C”) to the tunneling source (Si channel) resulting in the most effective injection condition as shown in Fig. 3.

III. DISCUSSION AND RESULTS

In our previous works, we have shown that at write/erase (W/E) voltages above 8/-8V, the threshold voltage shift (V_t shift) obtained with ZnO islands is larger than with ZrO₂ islands (shown in Fig. 4), while the shift with ZrO₂ almost saturates at high W/E voltages which indicates that the charge trap states density in ZnO could be larger than in ZrO₂. However, at low operating voltages, larger memory window is obtained with ZrO₂ which can be explained by the larger dielectric constant of the material ($k \sim 35$ as demonstrated in [10]). As a matter of fact, according to Gauss’s law across a MOScap-based memory, a high- k in the charge trapping layer results in a higher electric field across the tunnel oxide at the same W/E voltages which leads to a higher tunneling probability [11]. At higher operating W/E voltages, even though the injection field with ZrO₂ is still higher than with ZnO, however, in this case, the memory window would be limited by the available charge trap states density within the charge trapping layer.

The charge trap states density in the nano-islands at a W/E voltage of 7/-7V is calculated using the following equation:

$$N = \frac{C_t \times \Delta V t}{q} \quad (1)$$

Figure 4. Measured memory window at different Write/Erase voltages. Reused with permission from [9-10]

Figure 5. High frequency C-V characteristic of the memory a) with ZrO₂ islands b) with ZnO islands. Reused with permission from [9-10]

where C_t is the capacitance of the MOS memory per unit area and q is the elementary charge [12]. The capacitance is obtained from the measured C-V curves shown in Fig. 5a and Fig. 5b for the devices with ZrO₂ and ZnO islands, respectively, and the area of our fabricated devices is 45×45 μm². The charge trap states density in the ZnO and ZrO₂ islands is calculated taking into consideration the area coverage of the islands found to be 2.45×10¹³ cm⁻² and 1.2×10¹⁴ cm⁻², respectively.

According to the ITRS for charge trapping NOR flash memory, the physical gate length is projected to be 100-nm for the 32-nm node which is expected to be in production in the 2019-2021 years [13], and from Fig. 1a and Fig. 2a, there will definitely be several nano-islands embedded in each memory cell.

To study the scalability of the memory devices, we assume that each memory device has a square gate of area 100×100 nm², although the width of the memory devices is usually made larger than the gate length which would allow for more nano-islands to be embedded within each memory cell and therefore, leading to larger memory windows than the calculated values in this work.

The expected memory window for the scaled-down devices is calculated using equation (1). The thicknesses used for the tunnel and blocking oxides in our fabricated devices are within the projected range by the ITRS. Thus, we use the same values of the tunnel and blocking oxide thicknesses. The C_t is calculated with 4-nm Al₂O₃ tunnel oxide, 6-nm ZrO₂ and 10-nm Al₂O₃ blocking oxide for a 100×100 nm² square area. Then, again assuming that the new device has the same islands coverage of 1/3 of the total area, the V_t shift that can be obtained with this scaled device is then calculated using equation (1). In such memory devices, there would be around 127 ZrO₂ and 31 ZnO embedded nano-islands with average

width of 20-nm and 10-nm, respectively.

The following tables I and II summarize the obtained results for the 32-nm technology (100-nm physical gate length) and our fabricated devices results with ZnO and ZrO₂ nano-islands, respectively. The results show that the charge trapping memory devices with ZrO₂ nano-islands are expected to provide a very large V_t shift (9.4 V) due to the large charge trapping density, to the larger area coverage of the islands and to the high- κ of the nano-islands. It is also worth to mention that these results are based on the islands deposited by 20-ALD-cycles. However, with 30 cycles, more islands can be obtained which are smaller in size and closer to each other as demonstrated in our previous work [10]. Therefore, more islands could be embedded per memory leading to a higher memory window.

The V_t shift shown in the Table I and II are calculated with a W/E voltage of 10/-10 V. However, with different W/E voltages, V_t shift would be different. With a 7/-7 V W/E voltage, the new V_t shifts for the scaled down devices are calculated and found to be 7.7 V with ZrO₂ while 1.6 V with ZnO islands. With a 5/-5 V W/E voltage, the new V_t shifts would be 5.9 V with ZrO₂ while 0.7 V with ZnO islands. It is expected that with lower applied W/E voltages, the injection field would be lower resulting in a smaller memory window.

Table I. Scalability study on the memory with ZnO nano-islands

	Our devices	32-nm node
Physical Gate length	45-um	100-nm
Area of cell	45×45μm ²	100×100 nm ²
C _{gate-ox} (F)	39×10 ⁻¹²	3.93×10 ⁻¹⁷
N _t in ZnO (cm ⁻²)	2.45×10 ¹³	2.45×10 ¹³
Coverage of ZnO	1/5 of the total area	1/5 of the total area
V _t shift	8.5 V	2.5 V

Table II. Scalability study on the memory with ZrO₂ nano-islands

	Our devices	32-nm node
Physical Gate length	45-um	100-nm
Area of cell	45×45μm ²	100×100 nm ²
C _{gate-ox} (F)	170×10 ⁻¹²	5.12×10 ⁻¹⁷
N _t in ZrO ₂ (cm ⁻²)	1.2×10 ¹⁴	1.2×10 ¹⁴
Coverage of ZrO ₂	1/3 of the total area	1/3 of the total area
V _t shift	7.2V	9.4 V

One point that can cause reliability issues is the quantum confinement effects (QCE) in the nano-islands. In fact, we have already demonstrated that ZnO showed QCE in 1D while no such effects are obtained in the ZrO₂ islands [9-10]. Therefore, with ZnO, the performance of the memory cells will be different based on the different sizes of the islands embedded within each cell since their electronic properties will vary due to the QCE [14-17]. However, this problem is avoided with ZrO₂ islands since no QCE are shown and therefore the electronic properties of the islands are uniform and the performance of the memory will be based on the nano-

islands area coverage which is around 1/3.

Moreover, due the higher- κ of the the zirconia islands than ZnO islands, a larger electric field would be applied across the tunnel oxide under the same applied gate voltage. This might cause the breakdown of the tunnel oxide in the zirconia based memory after a smaller number of W/E cycles than in the case of the ZnO based memory. In other words, the endurance characteristic of the memory with ZnO islands could be better than the memory with ZrO₂ islands. However, we have shown in our previous work [10] that with ZrO₂, a 13.3% loss of the initial memory window is lost after 10⁵ W/E cycles which is considered as an excellent endurance characteristic

In terms of retention characteristic, leakage of the charge occurs either laterally by charge emission between the nano-islands or to the silicon channel. The former is limited by the tunneling probability between nano-islands; an Al₂O₃ oxide gap between the islands exceeding 10-nm is sufficient in making the direct tunneling current component insignificant. The latter is limited by the quiescent bias state of the device which keeps the Silicon surface in depletion. During the retention operation, without an applied gate bias, the band alignment is unfavorable for tunneling, thus, the nano-islands based memory has a long retention time as already proven in our previous works [9-10].

IV. CONCLUSION

In summary, the scalability characteristic of charge trapping memory devices with ZnO and ZrO₂ nano-islands grown by ALD is studied. The results show that although large memory devices show larger memory window with ZnO, however, scaled down devices show improved performance in terms of larger memory shift with the ZrO₂ nano-islands with a good retention characteristic. This is due to the higher density of the grown nano-islands which result in more trap states per memory, higher- κ of the material which results in a higher injection field at the same operating voltage, and the lack of quantum confinement effects.

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