DOI: 10.1002/((please add manuscript number))

Stable MoS₂ FETs using TiO₂ Interfacial Layer at Metal/MoS₂ Contact

By Woojin Park¹, Jung-Wook Min², Sohail Faizan Shaikh¹, and Muhammad Mustafa Hussain^{1}*

[*] Prof. M. M. Hussain, Dr. W. Park, S. F. Shaikh,
Integrated Nanotechnology Lab and Integrated Disruptive Electronic Applications
(IDEA) Lab
Electrical Engineering,
Computer Electrical Mathematical Science and Engineering Division
King Abdullah University of Science and Technology
Thuwal 23966-6900, Saudi Arabia
Dr. J.-W. Min
Photonics Lab
Electrical Engineering,
Computer Electrical Mathematical Science and Engineering Division
King Abdullah University of Science and Technology
Thuwal 23966-6900, Saudi Arabia
E-mail: muhammadmustafa.hussain@kaust.edu.sa

Keywords: MoS₂, TiO₂, Interfacial layer, Stability

1 The continuous scaling has been an important stimulus for the semiconductor technology
2
3 development in last several decades. As the scaling is progressed, the integration density
4
5 increases and circuit operation speed becomes faster. However, as device dimension scaling
6
7 approaches to the sub-100 nm regime, scaling limitations have been emerged because the
8
9 materials are based on atoms and the scaling approaches the atomic dimension. Due to the
10
11 several limitations such as quantum mechanical tunneling through a thin gate oxide which
12
13 causes serious leakage current problem and hence considerable power consumption through
14
15 heat dissipation, various approaches have been suggested including finding new material
16
17 candidates to replace for conventional silicon as active channel material.
18
19
20
21

22
23 Molybdenum disulfide (MoS_2), a type of atomic layer structured transition metal
24
25 dichalcogenide (TMDC) is an interesting emerging semiconducting material due to its atomic
26
27 flatness, high mobility, excellent scalability, and mechanical flexibility [1-10]. Single-layer
28
29 MoS_2 has 1.8 eV of direct band gap and multi-layer MoS_2 has 1.2~1.3 eV of indirect band
30
31 gap, hence, we can use single- and multi-layer MoS_2 as a semiconductor channel in switching
32
33 devices. Therefore, various applications have been demonstrated with MoS_2 channel
34
35 including memory devices, integrated circuits, and high sensitive sensors [11-21]. In
36
37 particular, it is well known that the most suitable application of MoS_2 is thin film transistors
38
39 (TFTs) for display applications. Mobility of usual MoS_2 field effect transistors is very similar
40
41 as that of poly-Si TFTs, which indicates that MoS_2 can be a replacement of poly-Si [22, 23].
42
43 In addition, demonstrations of flexible and transparent MoS_2 FETs with excellent mechanical
44
45 property suggest the possibility of future ultra-thin flexible display applications.
46
47
48
49
50

51
52 However, to use MoS_2 FETs for practical applications, several issues have to be
53
54 addressed: the synthesis of a high quality large area film which is an important issue on the
55
56 conventional fabrication platform, the deposition of a high quality dielectric layer with high
57
58 dielectric constant which can hold a promise of reduced leakage current maintaining same
59
60

gating efficiency, and achieving low resistance at metal-semiconductor junctions. In particular, high contact resistance at the junction is an serious obstacle to achieve high performances. Contact resistance problem can be more serious when a device is geometrically scaled as the external resistance becomes dominant component [24, 25]. In principle, MoS₂ FETs are Schottky barrier type transistors, which indicates that the operation of devices is controlled by tuning of Schottky barrier at the contact region, meaning that scaling of MoS₂ FETs would be difficult with large Schottky barrier dimension. Thus, reduction in Schottky barrier height or width can be an effective approach to achieve low contact resistance and high device performances [26]. There have been studies to reduce Schottky barrier dimension to achieve low contact resistance. To reduce Schottky barrier dimension, doping techniques (chlorine doping or molecule doping) and employing low work function contact metal (scandium) have been suggested [27-30]. Inserting a Fermi-level depinning layer between a contact metal and a MoS₂ channel was suggested as another approach to reduce Schottky barrier dimension [31]. By using a titanium dioxide (TiO₂) interfacial layer, density of interface states was reduced, achieving reduced Schottky barrier height. Study of stabilization with a TiO₂ interfacial layer was also conducted; from the low-frequency noise measurement, it was understood that more intrinsic device performance with the reduced noise level was achieved when using a TiO₂ interfacial layer by reducing interface states [32]. Over the previous studies, investigation of stabilization under a bias stress for MoS₂ FET with a TiO₂ interfacial layer is required to investigate a long term operation of devices.

Here, we conducted extensive experiments to study the stabilization of MoS₂ FETs tuned with a TiO₂ interfacial layer under gate bias stress. 20 cycle atomic layer deposition (ALD) ~3 nm TiO₂ interfacial layer was used. We choose a TiO₂ layer because a TiO₂ interfacial layer has an advantage of small band-offset with MoS₂. Increased drain current and enhanced

mobility were observed with a TiO₂ interfacial layer. The instability with the gate bias stress was also compared at room temperature and increased temperature to understand the thermal instability. Less threshold voltage (V_{TH}) shift was observed when using a TiO₂ interfacial layer and conducting electrical measurements at low temperature.

Figure 1(a) shows the Raman spectra for multi-layer MoS₂. There are two vibrational modes for MoS₂; the E_{2g}¹ mode ($\sim 384\text{ cm}^{-1}$) means in-plane vibrational motion of Mo and S atoms and the A_{1g} mode ($\sim 409\text{ cm}^{-1}$) corresponds to out-of-plane vibrational motion of Mo and S atoms. The thickness of the MoS₂ can be extracted with the frequency difference of two modes [33-35]. Single-layer MoS₂ shows a $18\sim 20\text{ cm}^{-1}$. As the number of layers increases, frequency difference increases with a redshift of the E_{2g}¹ mode and a blueshift of the A_{1g} mode. Bi-layer MoS₂ has $20\sim 22\text{ cm}^{-1}$ and multi-layer MoS₂ shows $\sim 25\text{ cm}^{-1}$. Figure 1(b) shows an atomic force microscopy (AFM) image of a MoS₂. The estimated thickness and the root mean square (RMS) are 21 nm and 2.23 nm, respectively. Figure 1(c) is the 3D schematic of a MoS₂ structure and a MoS₂ FET with an interfacial layer with a 20 cycle ALD TiO₂ interfacial layer. The MoS₂ structure shows a hexagonal close packed (HCP) lattice. 3 μm of channel length between source and drain electrode was used. TiO₂ interfacial layer thickness is estimated as $\sim 3\text{ nm}$ with a 20 cycle ALD deposition. MoS₂ transfer process and device fabrication flow is summarized in the supplementary information (Figure S1 and S2).

Figures 2(a) and 2(b) show the high resolution transmission electron microscopy (TEM) images, for Ti/MoS₂ and Ti/TiO₂/MoS₂ stack structures. MoS₂ atomic layer structure is well observed with 0.65 nm of lattice constant. In the Ti/MoS₂ stack, white native oxide like layer is observed at the boundary. TiO₂ interfacial layer is clearly shown between a Ti contact metal and a MoS₂ channel in figure 2(b). Figures 2(c) and 2(d) shows the fast Fourier transform for a MoS₂ crystal and a MoS₂/TiO₂ interface. A dot pattern is observed in the MoS₂ crystal, indicating that it has a single-crystal structure. On the other hand, mixed dot

and ring patterns are observed in the MoS₂/TiO₂ interface, meaning that TiO₂ layer has an amorphous structure [36]. Interestingly, in the Ti/MoS₂ structure, there are discontinuous layers of MoS₂ (Figure 2(e)). Theoretically, it is well known that TMDCs including MoS₂ does not have dangling bonds on the surface. This means that MoS₂ device does not need any passivation with a protective layer to avoid device performance degradation. However, evidences of dangling bonds which can react with chemical residues in ambient air have been observed from electrical and physical characteristics [37-39]. For example, impurity was detected from data of scanning tunneling microscope (STM) and inductively coupled plasma mass spectroscopy (ICPMS), showing that there are dangling bonding like binding sites and this issue can be addressed with an insulating buffer layer. From the HRTEM image in figure 2(e), it can be understood that carrier trapping binding sites can exist at the edge of the layers. As a result, clear difference of HRTEM images and FFTs between Ti/MoS₂ and Ti/TiO₂/MoS₂ stack structures is observed and it is also understood that oxide layer can cover discontinuous MoS₂ layer reducing carrier trapping sites. Energy dispersive spectroscopy (EDS) for a Ti/TiO₂/MoS₂ stack is displayed in the supplementary information (Figure S3).

Figure 3(a) is the transfer characteristics (I_{DS} - V_{BG}) of the MoS₂ FET without and with a TiO₂ interfacial layer. Gate bias was ranged from -50 V to 20 V and drain bias was applied from 0.1 V to 0.5 V with the 0.2 V step. The transfer curve shows a typical unipolar n-type behavior with a depletion mode (D-mode). I_{ON} for without and with TiO₂ interfacial layer is 2.83 μ A and 1.25 μ A at V_{DS} = 0.5 V and the field effect mobility (μ_{FE}) value for with and without TiO₂ interfacial layer is 4.42 cm²/Vs and 1.15 cm²/Vs. Our mobility values are relatively low compared to those of other studies as no capping layer was used in this study to decisively show intrinsic effects of a TiO₂ interfacial layer. Mobility value as a function of back gate bias for without and with TiO₂ layer was also compared in the supplementary document (Figure S4). The improved result of the performance in the transfer curve with

TiO₂ interfacial layer might be originated from the reduced interface states density and reduced contact resistance. The output characteristics (I_{DS} - V_{DS}) for MoS₂ FETs without and with TiO₂ interfacial layer are shown in figure 3(b). The gate bias increases from -50 V to 20 V in 10 V steps. The output characteristic contains information on series resistance. For the MoS₂ FET without TiO₂ layer, the output curve shows a unique behavior. The output curve at low drain bias region does not follow the typical linear behavior, meaning that the performance of the MoS₂ FET is suffer from the severe series resistance (R_{SD}). Indeed, serious high R_{SD} of usual MoS₂ FETs have been reported and reduction in R_{SD} has been an important challenge. On the other hand, the drain current is increased and the R_{SD} is relatively reduced for the MoS₂ FET with a TiO₂ interfacial layer. Previously, it was reported that an ALD TiO₂ layer can serve as a Fermi-level de-pinning layer or a MoS₂ doping layer, showing the reduced barrier height and the contact resistance [31, 40]. Additionally, deposition of a TiO₂ interfacial layer on the MoS₂ channel can partially contribute to the improvements of device performance with a simultaneous passivation, reducing the carrier scattering. Improved device performances with a TiO₂ layer in this study can be understood from thoes previous reports. The R_{SD} value of the MoS₂ FETs without and with a TiO₂ layer were calculated below.

To investigate the instability with a long time positive gate bias stress, stress measurements were conducted at room temperature (RT) and 80 °C and the results are summarized in Figures 4 and 5. A conventional stress-measure-stress technique was conducted with a fixed delay time. During bias stress measurements, the transfer characterization were conducted every decade (3.2s, 10s, 100s, 100s, and 10000s) by applying +10 V to the gate terminal. The drain and source voltage during the bias stress were fixed at 0 V. Total measurement time is 10000 s. The stress measurement set up schematic and the measurement sequence are shown in the supplementary information (Figure S5).

Figure 4 shows transfer curve shift of MoS₂ FETs without and with a TiO₂ interfacial layer at RT and 80 °C under increasing stress duration up to 10000s. For both cases, transfer curve parallel shifting was observed at RT and 80 °C. Transfer curve shifting was reduced by using a TiO₂ interfacial layer. Reduced drain current at 80 °C is corresponding to increased carrier scattering in the channel at high temperature.

Figures 5(a) and 5(b) show the shift of V_{TH} (ΔV_{TH}) as a function of gate bias stress time for MoS₂ FETs without and with a TiO₂ interfacial layer at RT and 80 °C. Overall, it is observed that the transfer curve shift is more severe without a TiO₂ interfacial layer at high temperature. ΔV_{TH} for MoS₂ FETs without a TiO₂ interfacial layer is 6.9 V. On the other hand, ΔV_{TH} for with a TiO₂ layer case is only ~1.5 V. At 80 °C, ΔV_{TH} is 8.2 V and 2.5 V for without and with a TiO₂ layer cases, respectively. An interface engineering with a TiO₂ layer offered a benefit of the performance stability with less ΔV_{TH} . Figures 5(c) and 5(d) show change of field effect mobility (μ_{FE}) of MoS₂ FETs without and with a TiO₂ interfacial layer at RT and 80 °C under 10000s gate bias stress measurement. At RT, μ_{FE} of MoS₂ FETs without and with a TiO₂ layer was reduced from 1.27 to 1.02 cm²/Vs and from 5.34 to 4.66 cm²/Vs, respectively. At 80 °C, μ_{FE} of MoS₂ FETs without and with a TiO₂ layer was reduced from 0.13 to 0.09 cm²/Vs and from 2.25 to 2.58 cm²/Vs, respectively. Reduction in μ_{FE} at high temperature was also observed in the conventional Si MOSFETs due to increased carrier scattering.

To explain the enhanced performances in the transfer characteristics and the stability in the gate bias stress measurements, hysteresis and the density of interface states were evaluated. First, to investigate the effects of a TiO₂ interfacial layer on the interface states, average hysteresis for the MoS₂ FETs with and without a TiO₂ interfacial layer were calculated (Figure 6(a)). The result shows that the hysteresis of the MoS₂ FET without a TiO₂ interfacial layer is more severe compared to that of the MoS₂ FET with a TiO₂ interfacial

layer. This difference of hysteresis can be explained by carrier trapping at the interface. Average hysteresis width values are 16.8 V and 6.6 V for the MoS₂ FETs with and without a TiO₂ interfacial layer, respectively. By observing hysteresis difference, we can indirectly understand the difference of reliability performance and the effects of TiO₂ interfacial layer. Second, to confirm the difference of interface states between with and without TiO₂ layer, the density of interface states was calculated. Figure 6(b) shows the density of interface states (D_{it}) for without and with TiO₂ interfacial layer FETs. A calculation technique was conducted with subthreshold swing (SS) using following equation [41].

$$SS = \frac{dV_g}{d(\log_{10} I_d)} = \ln 10 \cdot \frac{kT}{q} \left(1 + \frac{C_s + C_{it}}{C_{ox}} \right) \approx 60mV \left(1 + \frac{C_{it}}{C_{ox}} \right) \quad (1)$$

C_s is the capacitance in the MoS₂ conducting channel, C_{it} is the capacitance related to D_{it} , and C_{ox} is the oxide capacitance. The density of interface states for MoS₂ FETs without and with a TiO₂ interfacial layer were $2.63 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$ and $0.58 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$, respectively. About 78% of the density of interface states was reduced with a TiO₂ interfacial layer.

A TiO₂ interfacial layer serves as a Fermi-level de-pinning layer or a doping layer reducing interface states density at the contact region. To investigate the improvement of the contact region, series resistance (R_{SD}) was calculated. Usually, transmission line measurement (TLM) is employed with different channel length measurements to extract the contact resistance including R_{SD} . However, it is difficult to conduct TLM on a MoS₂ flake due to its limited area. Instead, we calculated R_{SD} values at the source and drain using the ratio of two linear DC, which is a previously suggested extracting approach with Si MOSFETs [42]. Figure 7 shows total resistances ($R_{TOT} = V_{DS}/I_{DS}$) at different drain biases (0.3 V and 0.5 V) and extracted R_{SD} value of a MoS₂ FET with and without a TiO₂ interfacial layer. The insets are the method of extracting series resistance by fitting the $R_{SD}-1/(V_{BG}-$

V_{TH}) curve and series resistance was extracted at drain current saturation point (high overdrive at $1/(V_{BG}-V_{TH}) \sim 0$). By using two linear transfer curves from a single MoS₂ FET, a more accurate R_{SD} was calculated at a high gate overdrive condition. Calculation technique is summarized in the supplementary. Both R_{TOT} and R_{SD} are reduced by using TiO₂ layer. Calculated R_{SD} is $\sim 139 \text{ k}\Omega\mu\text{m}$ and $\sim 300 \text{ k}\Omega\mu\text{m}$ for with and without a TiO₂ interfacial layer cases.

We can expect the transport mechanism of Ti/MoS₂ and Ti/TiO₂/MoS₂ stacks with band diagrams (Figure 8). The role of a TiO₂ interfacial layer is a buffer layer to cover dangling bonds which can alleviate Fermi-level pinning. As the effective Schottky barrier height (SBH) decreases, the electron conduction increases by overcoming the energy barrier. Effective SBH is displayed in Figure S9 in the supplementary information. Even though the details of theory of the barrier height reduction will be required, it can be understood from our results that inserting a TiO₂ interfacial layer between the contact metal and the MoS₂ channel is a promising technique to achieve more stable and higher performance MoS₂ FETs.

We investigated device stability for the MoS₂ FET with a TiO₂ interfacial layer. By using an Atomic Layer Deposition based TiO₂ interfacial layer, we observed increased I_{ON} and decreased R_{SD} . The MoS₂ FET with the TiO₂ interfacial layer showed more stable device performance with less shifted V_{TH} and μ_{FE} after 10000 s gate bias stress. This study makes a step forward toward stable 2D dichalcogenide based thin film transistors.

Experimental Section

Material analysis. MoS₂ (2D Semiconductors) was transferred onto 4 inch SiO₂ (300 nm)/Si (heavily doped) substrates by a mechanical exfoliation process. 300 nm of SiO₂ is the optimized thickness to observe MoS₂ flakes. Raman spectroscopy (ARAMIS, laser wavelength: 473 nm, 50 mW) was used to evaluate the optical characteristics of the transferred representative multi-layer MoS₂. The topological image, the root mean square (RMS) roughness, and the thickness of the multi-layer MoS₂ were observed using an AFM.

Device Fabrication. Atomic layer deposition (ALD) was used to deposit TiO₂ interfacial layer on MoS₂ using tetrakis-dimethyl-amido titanium (TDMAT) precursor. Deposition process was maintained at 200 °C. Photolithography, metal deposition, and lift-off processes were conducted to form source and drain electrodes. The distance between the source and the drain electrodes is 3 μm. E-beam evaporation was used to deposit contact metal to reduce the damage on the MoS₂ surface. Titanium (Ti) was used as a contact metal since Ti has small band offset with MoS₂. Thermal annealing was conducted in a vacuum environment at 300 °C for 1h after device fabrication.

Device Characterization. Transfer, output, and reliability measurements were done with Keithley 4200. To observe the parameter change with gate bias stress, current-voltage was measured every decade under gate bias stress, calculating threshold voltage. Reliability measurements were conducted at room temperature and 80 °C to see the behavior in the high temperature environment.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This publication is based upon work supported by the King Abdullah University of Science and Technology (KAUST) Office of Sponsored Research (OSR) under Award No. OSR-2015-Sensors-2707.

Received: ((will be filled in by the editorial staff))

Revised: ((will be filled in by the editorial staff))

Published online: ((will be filled in by the editorial staff))

References

1. Bertolazzi, S., J. Brivio, and A. Kis, *Stretching and breaking of ultrathin MoS₂*. ACS Nano, 2011. **5**(12): p. 9703-9.
2. Castellanos-Gomez, A., et al., *Elastic Properties of Freely Suspended MoS₂ Nanosheets*. Advanced Materials, 2012. **24**(6): p. 772-+.
3. Li, H., et al., *Optical identification of single- and few-layer MoS₂ sheets*. Small, 2012. **8**(5): p. 682-6.
4. Li, H., et al., *Fabrication of single- and multilayer MoS₂ film-based field-effect transistors for sensing NO at room temperature*. Small, 2012. **8**(1): p. 63-7.
5. Palummo, M., M. Bernardi, and J.C. Grossman, *Exciton radiative lifetimes in two-dimensional transition metal dichalcogenides*. Nano Lett, 2015. **15**(5): p. 2794-800.
6. Radisavljevic, B., et al., *Single-layer MoS₂ transistors*. Nat Nanotechnol, 2011. **6**(3): p. 147-50.
7. Salvatore, G.A., et al., *Fabrication and transfer of flexible few-layers MoS₂ thin film transistors to any arbitrary substrate*. ACS Nano, 2013. **7**(10): p. 8809-15.
8. Yin, Z., et al., *Single-layer MoS₂ phototransistors*. ACS Nano, 2012. **6**(1): p. 74-80.
9. Yoon, J., et al., *Highly flexible and transparent multilayer MoS₂ transistors with graphene electrodes*. Small, 2013. **9**(19): p. 3295-300.
10. Yu, W.J., et al., *Vertically stacked multi-heterostructures of layered materials for logic transistors and complementary inverters*. Nature Materials, 2013. **12**(3): p. 246-252.
11. Bertolazzi, S., D. Krasnozhan, and A. Kis, *Nonvolatile Memory Cells Based on MoS₂/Graphene Heterostructures*. Acs Nano, 2013. **7**(4): p. 3246-3252.
12. De Fazio, D., et al., *High Responsivity, Large-Area Graphene/MoS₂ Flexible Photodetectors*. Acs Nano, 2016. **10**(9): p. 8252-8262.
13. Fang, H., et al., *Degenerate n-Doping of Few-Layer Transition Metal Dichalcogenides by Potassium*. Nano Letters, 2013. **13**(5): p. 1991-1995.
14. He, G., et al., *Thermally Assisted Nonvolatile Memory in Monolayer MoS₂ Transistors*. Nano Letters, 2016. **16**(10): p. 6445-6451.
15. Lee, H.S., et al., *MoS₂ Nanosheets for Top-Gate Nonvolatile Memory Transistor Channel*. Small, 2012. **8**(20): p. 3111-3115.
16. Radisavljevic, B., M.B. Whitwick, and A. Kis, *Integrated circuits and logic operations based on single-layer MoS₂*. ACS Nano, 2011. **5**(12): p. 9934-8.
17. Roy, T., et al., *Dual-Gated MoS₂/WSe₂ van der Waals Tunnel Diodes and Transistors*. Acs Nano, 2015. **9**(2): p. 2071-2079.
18. Wang, H., et al., *Integrated Circuits Based on Bilayer MoS₂ Transistors*. Nano Letters, 2012. **12**(9): p. 4674-4680.
19. Wi, S., et al., *Enhancement of photovoltaic response in multilayer MoS₂ induced by plasma doping*. ACS Nano, 2014. **8**(5): p. 5270-81.
20. Zhang, E.Z., et al., *Tunable Charge-Trap Memory Based on Few-Layer MoS₂*. Acs Nano, 2015. **9**(1): p. 612-619.
21. Zhang, W.J., et al., *Ultrahigh-Gain Photodetectors Based on Atomically Thin Graphene-MoS₂ Heterostructures*. Scientific Reports, 2014. **4**.
22. Kim, S., et al., *High-mobility and low-power thin-film transistors based on multilayer MoS₂ crystals*. Nature Communications, 2012. **3**.
23. Kwon, J., et al., *Optically transparent thin-film transistors based on 2D multilayer MoS₂ and indium zinc oxide electrodes*. Nanotechnology, 2015. **26**(3).

24. Agrawal, A., et al., *Fermi level depinning and contact resistivity reduction using a reduced titania interlayer in n-silicon metal-insulator-semiconductor ohmic contacts*. Applied Physics Letters, 2014. **104**(11).
25. Noori, A.M., et al., *Manufacturable processes for ≤ 32 -nm-node CMOS enhancement by synchronous optimization of strain-engineered channel and external parasitic resistances*. Ieee Transactions on Electron Devices, 2008. **55**(5): p. 1259-1264.
26. Liu, H., A.T. Neal, and P.D.D. Ye, *Channel Length Scaling of MoS₂ MOSFETs*. Acs Nano, 2012. **6**(10): p. 8563-8569.
27. Das, S., et al., *High Performance Multilayer MoS₂ Transistors with Scandium Contacts*. Nano Letters, 2013. **13**(1): p. 100-105.
28. Du, Y.C., et al., *Molecular Doping of Multilayer MoS₂ Field-Effect Transistors: Reduction in Sheet and Contact Resistances*. Ieee Electron Device Letters, 2013. **34**(10): p. 1328-1330.
29. Yang, L.M., et al., *High-Performance MoS₂ Field-Effect Transistors Enabled by Chloride Doping: Record Low Contact Resistance ($0.5 \text{ k } \Omega \cdot \mu\text{m}$) and Record High Drain Current ($460 \text{ } \mu\text{A}/\mu\text{m}$)*. 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, 2014.
30. Yang, L.M., et al., *Chloride Molecular Doping Technique on 2D Materials: WS₂ and MoS₂*. Nano Letters, 2014. **14**(11): p. 6275-6280.
31. Park, W., et al., *Contact Resistance Reduction using Fermi Level De-pinning Layer for MoS₂ FETs*. 2014 Ieee International Electron Devices Meeting (Iedm), 2014.
32. Kim, Y., et al., *Reduction of low-frequency noise in multilayer MoS₂ FETs using a Fermi-level depinning layer*. Physica Status Solidi-Rapid Research Letters, 2016. **10**(8): p. 634-638.
33. Berkdemir, A., et al., *Identification of individual and few layers of WS₂ using Raman Spectroscopy*. Scientific Reports, 2013. **3**.
34. Han, S.W., et al., *Band-gap transition induced by interlayer van der Waals interaction in MoS₂*. Physical Review B, 2011. **84**(4).
35. Lee, C., et al., *Anomalous Lattice Vibrations of Single- and Few-Layer MoS₂*. Acs Nano, 2010. **4**(5): p. 2695-2700.
36. Jeong, H.Y., et al., *Role of Interface Reaction on Resistive Switching of Metal/Amorphous TiO₂/Al RRAM Devices*. Journal of the Electrochemical Society, 2011. **158**(10): p. H979-H982.
37. Addou, R., et al., *Impurities and Electronic Property Variations of Natural MoS₂ Crystal Surfaces*. Acs Nano, 2015. **9**(9): p. 9124-9133.
38. Late, D.J., et al., *Hysteresis in Single-Layer MoS₂ Field Effect Transistors*. Acs Nano, 2012. **6**(6): p. 5635-5641.
39. Rehman, A.U., et al., *n-MoS₂/p-Si Solar Cells with Al₂O₃ Passivation for Enhanced Photogeneration*. Acs Applied Materials & Interfaces, 2016. **8**(43): p. 29383-29390.
40. Kaushik, N., et al., *Interfacial n-Doping Using an Ultrathin TiO₂ Layer for Contact Resistance Reduction in MoS₂*. Acs Applied Materials & Interfaces, 2016. **8**(1): p. 256-263.
41. Najam, F., et al., *Two-dimensional (2D) transition metal dichalcogenide semiconductor field-effect transistors: the interface trap density extraction and compact model*. Semiconductor Science and Technology, 2015. **30**(7).
42. Campbell, J.P., et al., *A Simple Series Resistance Extraction Methodology for Advanced CMOS Devices*. Ieee Electron Device Letters, 2011. **32**(8): p. 1047-1049.

Figure captions

Figure 1. (a) Raman spectra for multilayer MoS₂. (b) AFM height profile for a mechanically exfoliated multilayer MoS₂. (c) 3-D schematic of a MoS₂ structure and a back-gated multilayer MoS₂ FET with a 20 cycle ALD TiO₂ interfacial layer.

Figure 2 HRTEM images for (a) Ti/MoS₂ and (b) Ti/TiO₂/MoS₂ stacks. Fast Fourier transform (FFT) for (c) MoS₂ and (d) TiO₂/MoS₂ interface. (e) A HRTEM image showing discontinuous MoS₂ layers and binding states in a stack structure.

Figure 3. (a) Transfer characteristics of MoS₂ FETs without and with a TiO₂ interfacial layer at $V_{DS} = 0.5$ V. (b) Output characteristics of MoS₂ FETs without and with a TiO₂ interfacial layer.

Figure 4. Transfer curves of MoS₂ FETs (a) without and (b) with a TiO₂ interfacial layer under 10000s gate bias stress at room temperature. Transfer curves of MoS₂ FETs (c) without and (d) with a TiO₂ interfacial layer under 10000s gate bias stress at 80°C.

Figure 5. 10000s stress time dependent ΔV_{TH} shift of MoS₂ FETs (a) without and (b) with a TiO₂ interfacial layer. 10000s stress time dependent μ_{FE} shift of MoS₂ FETs (c) without and (d) with a TiO₂ interfacial layer. ΔV_{TH} and μ_{FE} were compared at room temperature and 80 °C.

Figure 6. (a) Average hysteresis width of MoS₂ FETs without and with a TiO₂ interfacial layer. (b) Density of interface trap (D_{it}) calculated from the subthreshold swing (SS).

Figure 7. Total resistance ($R_T = V_{DS}/I_{DS}$) and extracted R_{SD} as a function of back gate overdrive for MoS₂ FETs (a) without and (b) with a TiO₂ interfacial layer. Resistance values were extracted at $V_D = 0.3$ V and $V_D = 0.5$ V. Extracted R_{SD} values at the high gate overdrive ($1/(V_{BG}-V_{TH}) \sim 0V^{-1}$) are in insets.

Figure 8. Band diagrams for (a) Ti/MoS₂ and (b) Ti/TiO₂/MoS₂. The band diagram for Ti/TiO₂/MoS₂ indicates the reduced effective Schottky barrier height (SBH) and density of interface states.

Figure 1 (Park *et al.*)

Figure 2 (Park *et al.*)

Figure 3 (Park *et al.*)

Figure 4 (Park *et al.*)

Figure 5 (Park *et al.*)

Figure 6 (Park *et al.*)

Figure 7 (Park *et al.*)

Figure 8 (Park *et al.*)

The table of contents

Unstable and low performance of MoS₂ FETs are serious issues in practical applications. We suggest an approach to achieve more stable performance of MoS₂ FETs by inserting an atomic layer deposition (ALD) titanium dioxide (TiO₂) interfacial layer. Reduced threshold voltage (V_{TH}) shift was observed after 10000s of +10 V gate bias stress.

MoS₂, TiO₂, Interfacial layer, Stability

Woojin Park, Jung-Wook Min, Sohail Faizan Shaikh, Boon. S. Ooi, and Muhammad Mustafa Hussain*

Stable MoS₂ FETs with Interface Engineering.

[Click here to access/download](#)

Supporting Information

Park-supplementary_PSSA.doc